Freescale Semiconductor - PK60FX512VLQ12 Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 48x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=pk60fx512vlq12

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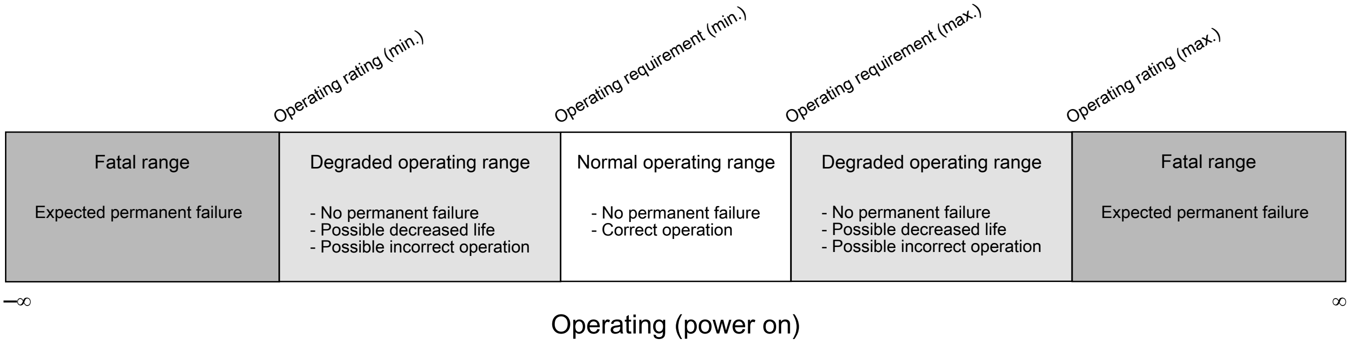
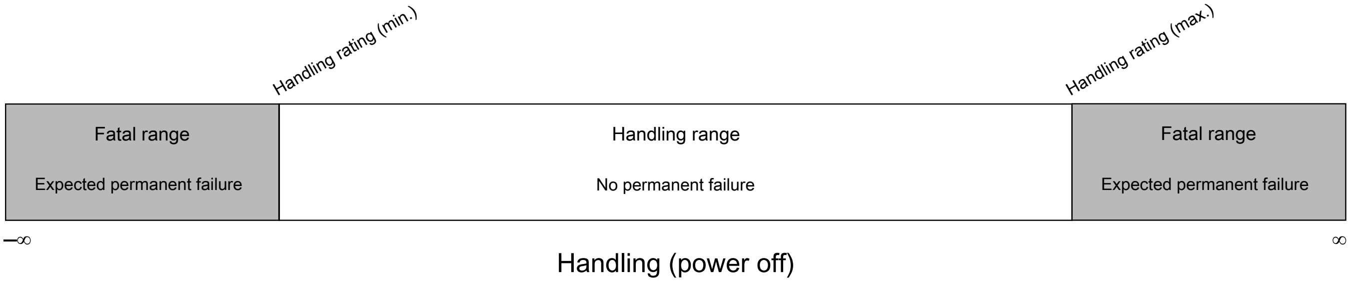
3.4 Relationship between ratings and operating requirements





3.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -9mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—	—	V	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Output high voltage — low drive strength • $2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$, $I_{OH} = -2\text{mA}$ • $1.71\text{ V} \le V_{DD} \le 2.7\text{ V}$, $I_{OH} = -0.6\text{mA}$	 $V_{DD} - 0.5$ $V_{DD} - 0.5$	 — —	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
I_{OHT_io60}	Output high current total for fast digital ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength • $2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$, $I_{OL} = 10\text{ mA}$ • $1.71\text{ V} \le V_{DD} \le 2.7\text{ V}$, $I_{OL} = 5\text{ mA}$	 — —	 — —	 0.5 0.5	 V V	
	Output low voltage — low drive strength • $2.7\text{ V} \le V_{DD} \le 3.6\text{ V}$, $I_{OL} = 2\text{ mA}$ • $1.71\text{ V} \le V_{DD} \le 2.7\text{ V}$, $I_{OL} = 1\text{ mA}$	 — —	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{OLT_io60}	Output low current total for fast digital ports	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs • $V_{SS} \le V_{IN} \le V_{DD}$ • All pins except EXTAL32, XTAL32, EXTAL, XTAL • EXTAL (PTA18) and XTAL (PTA19) • EXTAL32, XTAL32	 — — —	 0.002 0.004 0.075	 0.5 1.5 10	 µA µA µA	1, 2
I_{IND}	Input leakage current, digital pins • $V_{SS} \le V_{IN} \le V_{IL}$ • All digital pins • $V_{IN} = V_{DD}$ • All digital pins except PTD7 • PTD7	 — — —	 0.002 0.002 0.004	 0.5 0.5 1	 µA µA µA	2, 3
I_{IND}	Input leakage current, digital pins • $V_{IL} < V_{IN} < V_{DD}$ • $V_{DD} = 3.6\text{ V}$ • $V_{DD} = 3.0\text{ V}$ • $V_{DD} = 2.5\text{ V}$ • $V_{DD} = 1.7\text{ V}$	 — — — —	 18 12 8 3	 26 19 13 6	 µA µA µA µA	2, 3, 4
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5\text{ V}$	 —	 1	 50	 µA	2, 3
Z_{IND}	Input impedance examples, digital pins	 —	 —	 48	 kΩ	2, 5

Table continues on the next page...

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
		parameter, junction to package top outside center (natural convection)				

NOTES:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns

Table continues on the next page...

Table 13. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.4	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 0 0 0	 10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 50 25 12.5	 — — —	 ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.4	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 4.5	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	180	—	ps	

Table continues on the next page...

6.3.2 Oscillator electrical specifications

6.3.2.1 Oscillator DC electrical specifications

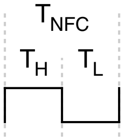
Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

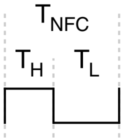
Table continues on the next page...

$$T_H = (1 - \text{SCALER} / 2) \times \frac{T_{NFC}}{2}$$

For example, if SCALER is 0.2, then $T_H = T_L = T_{NFC}/2$.



However, if SCALER is 0.667, then $T_L = 2/3 \times T_{NFC}$ and $T_H = 1/3 \times T_{NFC}$.



NOTE

The reciprocal of SCALER must be a multiple of 0.5. For example, 1, 1.5, 2, 2.5, etc.

Table 25. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns
t_{WP}	$\overline{\text{NFC\_WP}}$ pulse width	$T_L - 1$	—	ns
t_{ALS}	NFC_ALE setup time	$2T_H + T_L$	—	ns
t_{ALH}	NFC_ALE hold time	$T_H + T_L$	—	ns
t_{DS}	Data setup time	$T_L - 1$	—	ns
t_{DH}	Data hold time	$T_H - 1$	—	ns
t_{WC}	Write cycle time	$T_H + T_L - 1$	—	ns
t_{WH}	$\overline{\text{NFC\_WE}}$ hold time	$T_H - 1$	—	ns
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ low	$4T_H + 3T_L + 90$	—	ns
t_{RP}	$\overline{\text{NFC\_RE}}$ pulse width	$T_L + 1$	—	ns
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC\_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

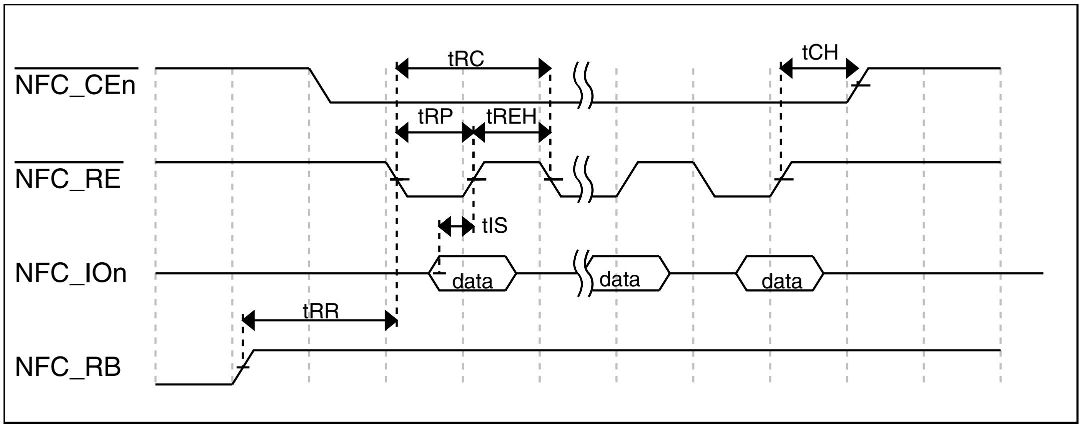


Figure 16. Read data latch cycle timing in non-fast mode

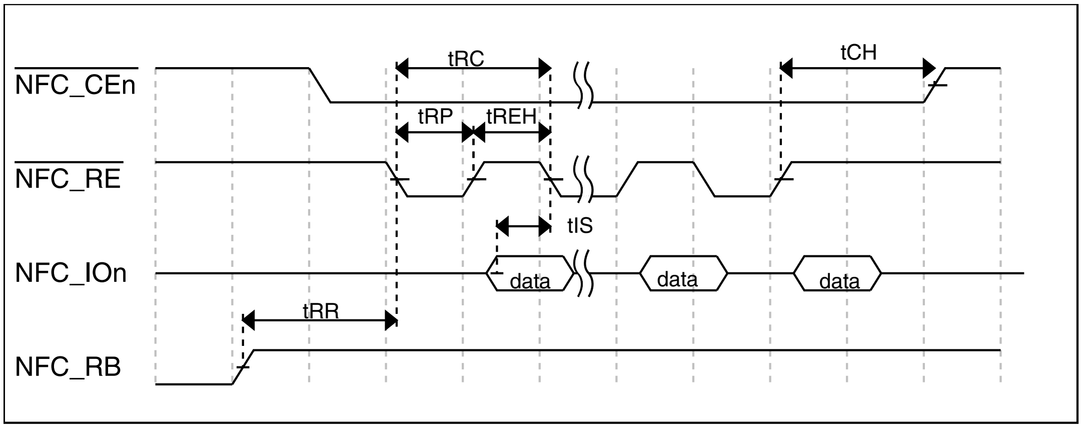


Figure 17. Read data latch cycle timing in fast mode

6.4.4 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 26. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	

Table continues on the next page...

Table 32. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

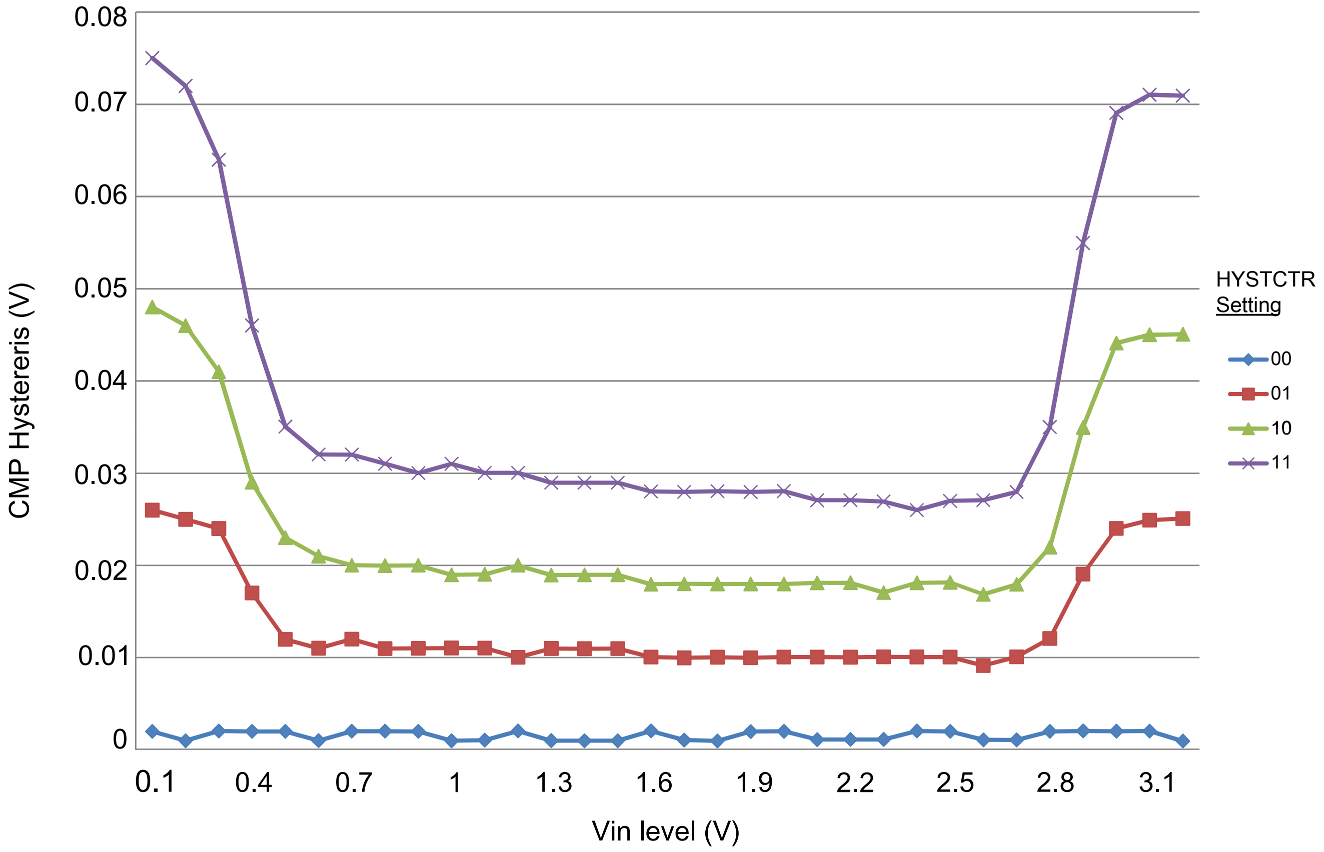


Figure 23. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

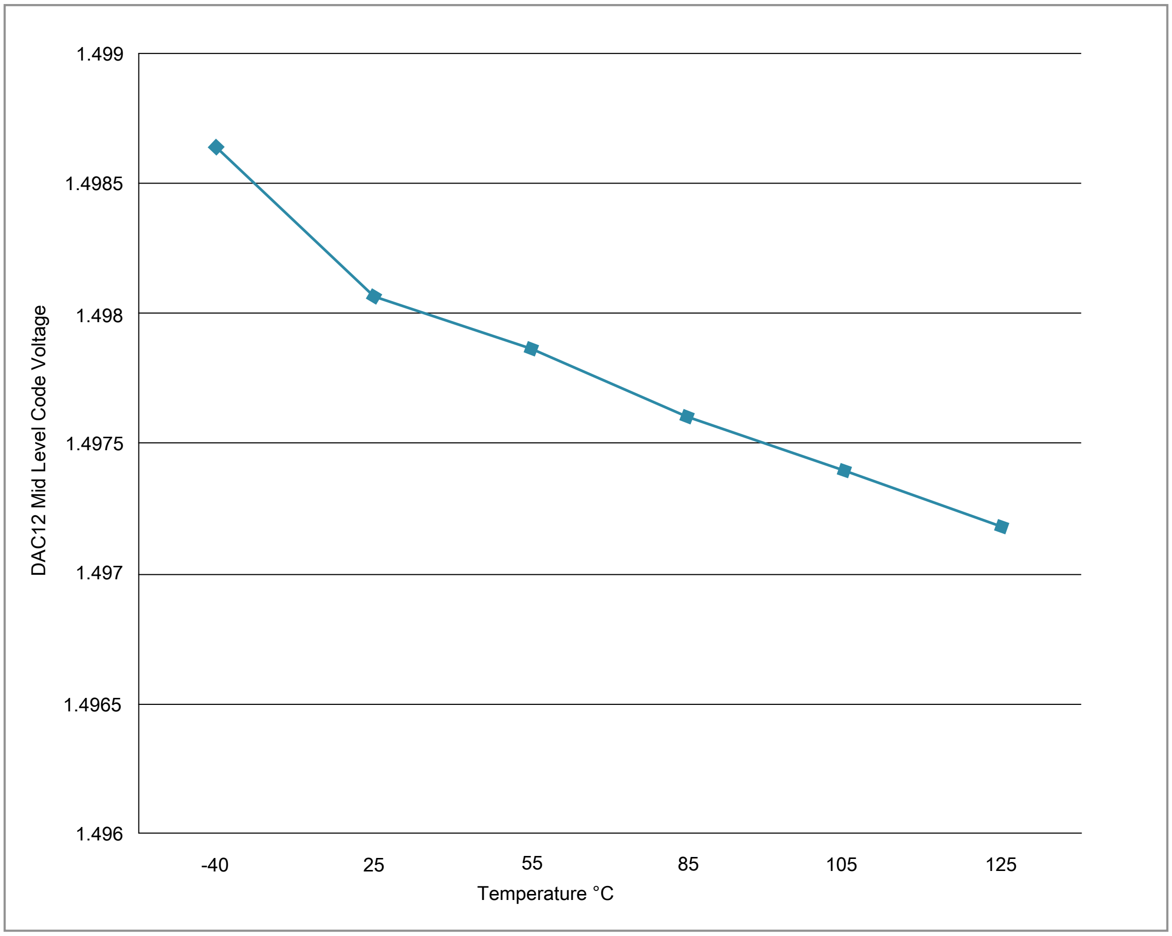


Figure 26. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 35. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

6.8.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.8.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 39. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

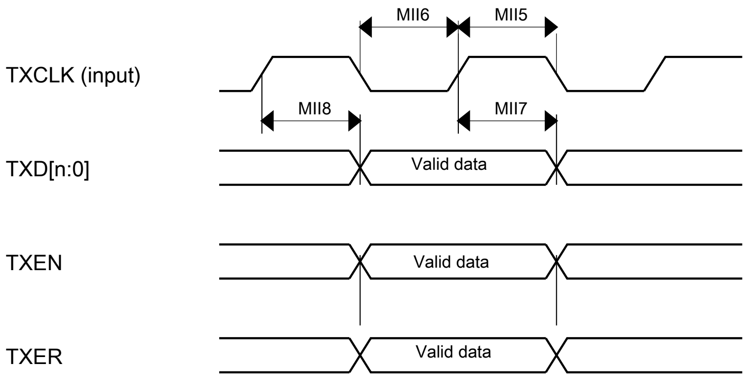


Figure 27. RMII/MII transmit signal timing diagram

Table 46. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

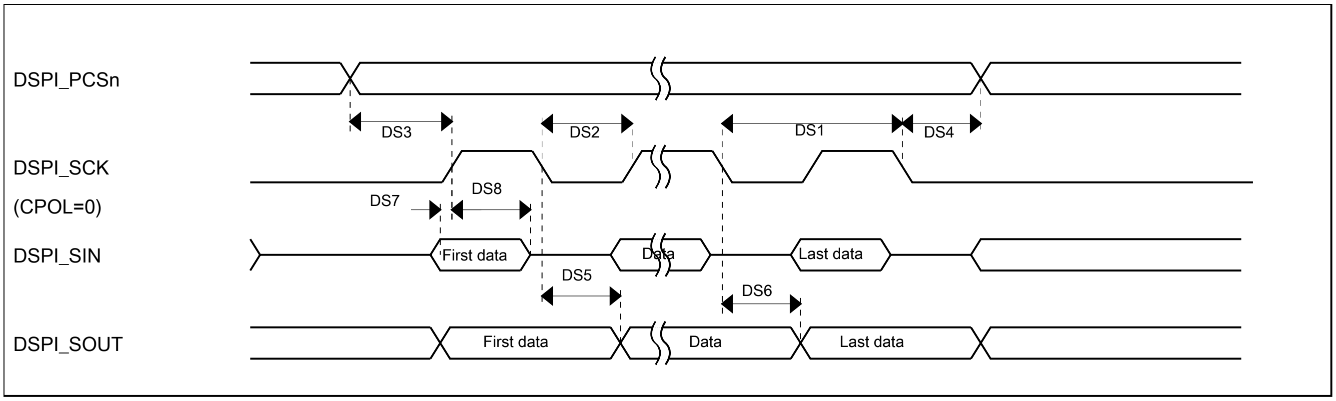


Figure 32. DSPI classic SPI timing — master mode

Table 47. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

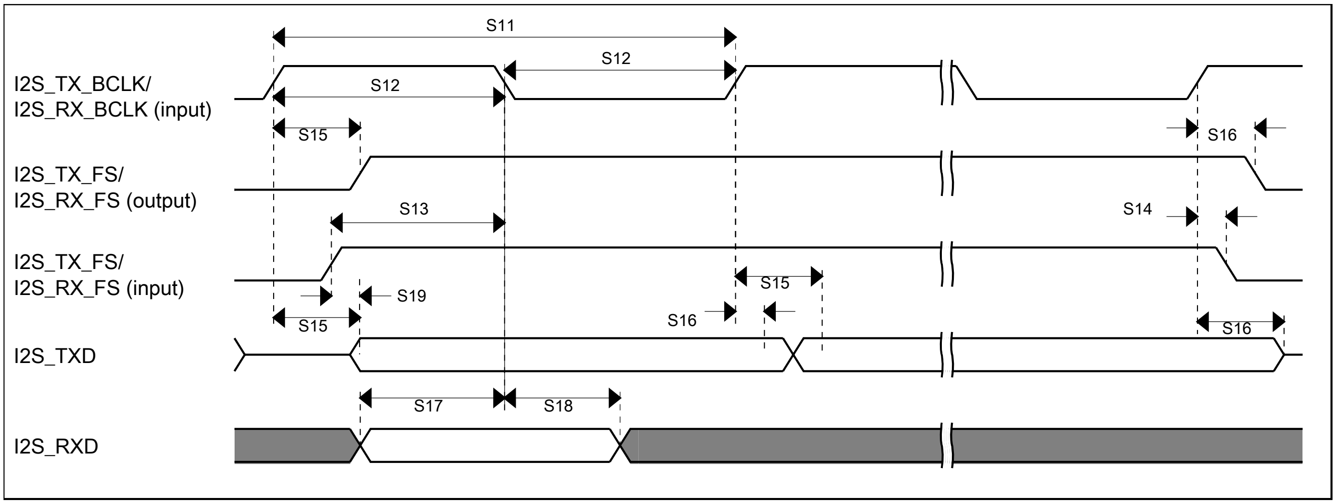


Figure 39. I2S/SAI timing — slave modes

6.8.12.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	-1.6	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

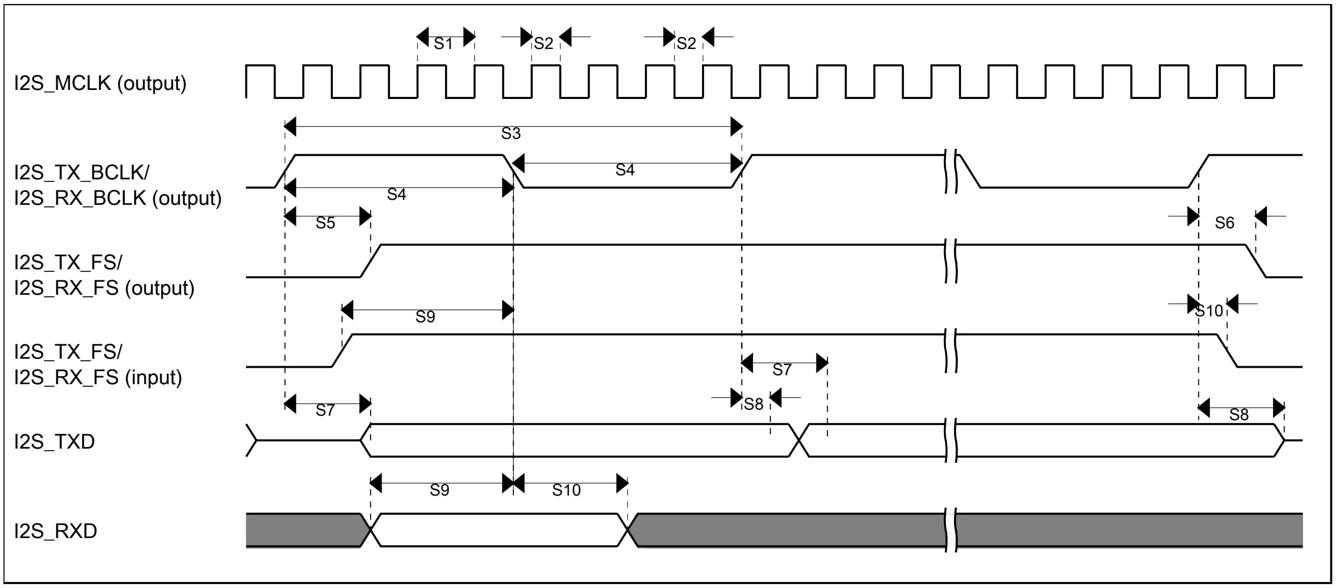


Figure 40. I2S/SAI timing — master modes

Table 56. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Table 58. Pins with active pull control after reset

Pin	Active pull direction after reset
PTA0	pulldown
PTA1	pullup
PTA3	pullup
PTA4	pullup
RESET_b	pullup

8.2 K60 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	L5	RTC_WAKEUP_B	RTC_WAKEUP_B	RTC_WAKEUP_B								
—	M5	NC	NC	NC								
—	A10	NC	NC	NC								
—	B10	NC	NC	NC								
—	C10	NC	NC	NC								
1	D3	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA	RTC_CLKOUT	
2	D2	PTE1/LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL	SPI1_SIN	
3	D1	PTE2/LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/LLWU_P1	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
4	E4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD			SPI1_SOUT	
5	E5	VDD	VDD	VDD								
6	F6	VSS	VSS	VSS								
7	E3	PTE4/LLWU_P2	DISABLED		PTE4/LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0		
9	E1	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		FTM3_CH1	USB_SOF_OUT	
10	F4	PTE7	DISABLED		PTE7		UART3_RTS_b	I2S0_RXD0		FTM3_CH2		
11	F3	PTE8	ADC2_SE16	ADC2_SE16	PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_FS		FTM3_CH3		
12	F2	PTE9	ADC2_SE17	ADC2_SE17	PTE9	I2S0_TXD1	UART5_RX	I2S0_RX_BCLK		FTM3_CH4		

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
36	J3	ADC0_SE16/CMP1_IN2/ADC0_SE21	ADC0_SE16/CMP1_IN2/ADC0_SE21	ADC0_SE16/CMP1_IN2/ADC0_SE21								
37	M3	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18	VREF_OUT/CMP1_IN5/CMP0_IN5/ADC1_SE18								
38	L3	DAC0_OUT/CMP1_IN3/ADC0_SE23	DAC0_OUT/CMP1_IN3/ADC0_SE23	DAC0_OUT/CMP1_IN3/ADC0_SE23								
39	L4	DAC1_OUT/CMP0_IN4/CMP2_IN3/ADC1_SE23	DAC1_OUT/CMP0_IN4/CMP2_IN3/ADC1_SE23	DAC1_OUT/CMP0_IN4/CMP2_IN3/ADC1_SE23								
40	M7	XTAL32	XTAL32	XTAL32								
41	M6	EXTAL32	EXTAL32	EXTAL32								
42	L6	VBAT	VBAT	VBAT								
43	—	VDD	VDD	VDD								
44	—	VSS	VSS	VSS								
45	M4	PTE24	ADC0_SE17/EXTAL1	ADC0_SE17/EXTAL1	PTE24	CAN1_TX	UART4_TX	I2S1_TX_FS		EWM_OUT_b	I2S1_RXD1	
46	K5	PTE25	ADC0_SE18/XTAL1	ADC0_SE18/XTAL1	PTE25	CAN1_RX	UART4_RX	I2S1_TX_BCLK		EWM_IN	I2S1_TXD1	
47	K4	PTE26	ADC3_SE5b	ADC3_SE5b	PTE26	ENET_1588_CLKIN	UART4_CTS_b	I2S1_TXD0		RTC_CLKOUT	USB_CLKIN	
48	J4	PTE27	ADC3_SE4b	ADC3_SE4b	PTE27		UART4_RTS_b	I2S1_MCLK				
49	H4	PTE28	ADC3_SE7a	ADC3_SE7a	PTE28							
50	J5	PTA0	JTAG_TCLK/SWD_CLK/EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_b/UART0_COL_b	FTM0_CH5				JTAG_TCLK/SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/TRACE_SWO/EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/TRACE_SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/SWD_DIO	
54	L7	PTA4/LLWU_P3	NMI_b/EZP_CS_b	TSI0_CH5	PTA4/LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2	RMII0_RXER/MII0_RXER	CMP2_OUT	I2S0_TX_BCLK	JTAG_TRST_b	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	ADC3_SE6a	ADC3_SE6a	PTA6	ULPI_CLK	FTM0_CH3	I2S1_RXD0			TRACE_CLKOUT	

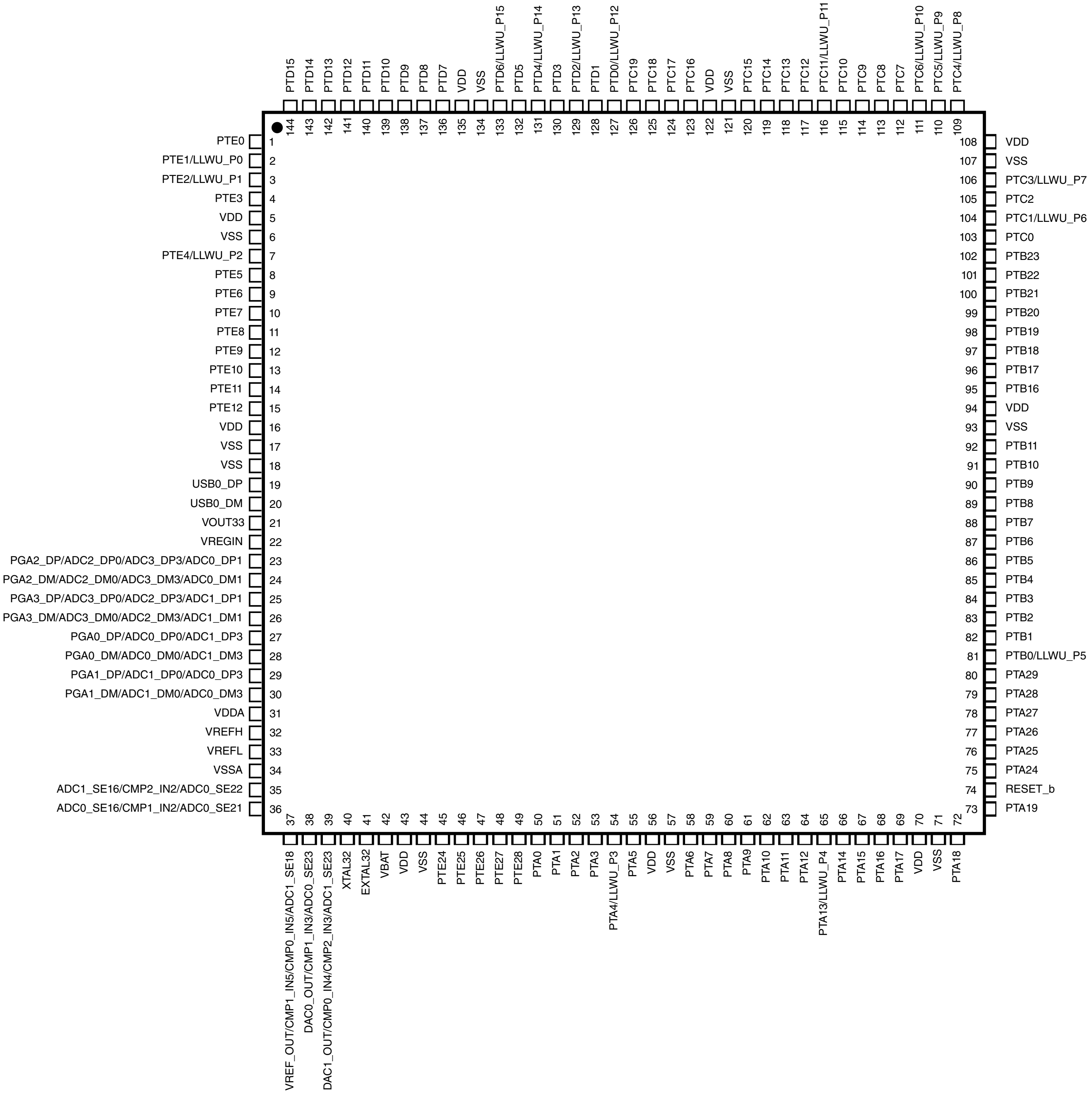


Figure 42. K60 144 LQFP Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6/ LLWU_P15	PTD5	PTD4/ LLWU_P14	PTD0/ LLWU_P12	PTC16	PTC12	PTC8	PTC4/ LLWU_P8	NC	PTC3/ LLWU_P7	PTC2	A
B	PTD12	PTD11	PTD10	PTD3	PTC19	PTC15	PTC11/ LLWU_P11	PTC7	PTD9	NC	PTC1/ LLWU_P6	PTC0	B
C	PTD15	PTD14	PTD13	PTD2/ LLWU_P13	PTC18	PTC14	PTC10	PTC6/ LLWU_P10	PTD8	NC	PTB23	PTB22	C
D	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5/ LLWU_P9	PTB21	PTB20	PTB19	PTB18	D
E	PTE6	PTE5	PTE4/ LLWU_P2	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10	PTE9	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	VOUT33	VREGIN	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	USB0_DP	USB0_DM	VSS	PTE28	VDDA	VSSA	VSS	VSS	PTB1	PTB0/ LLWU_P5	PTA29	PTA28	H
J	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	PTE27	PTA0	PTA1	PTA6	PTA7	PTA13/ LLWU_P4	PTA27	PTA26	PTA25	J
K	PGA3_DP/ ADC2_DP3/ ADC1_DP1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	PTE26	PTE25	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	RTC_ WAKEUP_B	VBAT	PTA4/ LLWU_P3	PTA9	PTA11	PTA14	PTA15	RESET_b	L
M	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	PTE24	NC	EXTAL32	XTAL32	PTA5	PTA10	VSS	PTA19	PTA18	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 43. K60 144 MAPBGA Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 59. Revision History

Rev. No.	Date	Substantial Changes
3	3/2012	Initial public release

Table continues on the next page...