**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 55MHz |
| Connectivity | CANbus, Ethernet, I²C, SPI, SSC, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 62 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 1.95V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFBGA |
| Supplier Device Package | 100-TFBGA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at91sam7x512b-cu |

### 8.5.3 Lock Regions

#### 8.5.3.1 SAM7X512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7X512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 32 NVM bits are software programmable through both of the EFC User Interfaces. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

#### 8.5.3.2 SAM7X256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7X256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

#### 8.5.3.3 SAM7X128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7X128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

### 8.5.4 Security Bit Feature

The SAM7X512/256/128 features a security bit, based on a specific NVM-Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command "Set Security Bit" of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 220 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

### 8.5.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands "Clear General-purpose NVM Bit" and "Set General-purpose NVM Bit" of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.

## 9.1 Reset Controller

- Based on one power-on reset cell and one brownout detector
- Status of the last reset, either Power-up Reset, Software Reset, User Reset, Watchdog Reset, Brownout Reset
- Controls the internal resets and the NRST pin output
- Allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

### 9.1.1 Brownout Detector and Power-on Reset

The SAM7X512/256/128 embeds one brownout detection circuit and a power-on reset cell. The power-on reset is supplied with and monitors VDDCORE.

Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the power supplies.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE and VDDFLASH levels during operation by comparing them to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE or VDDFLASH.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (Vbot18-, defined as Vbot18 - hyst/2), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (Vbot18+, defined as Vbot18 + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The VDDCORE threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of ± 2% and is factory calibrated.

When the brownout detector is enabled and VDDFLASH decreases to a value below the trigger level (Vbot33-, defined as Vbot33 - hyst/2), the brownout output is immediately activated.

When VDDFLASH increases above the trigger level (Vbot33+, defined as Vbot33 + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The VDDFLASH threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 2.80V with an accuracy of ± 3.5% and is factory calibrated.

The brownout detector is low-power, as it consumes less than 28 µA static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1µA. The deactivation is configured through the GPNVM bit 0 of the Flash.

## 10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

## 10.10 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

## 10.11 Timer Counter

- Three 16-bit Timer Counter Channels
  - Two output compare or one input capture per channel
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs

## 11.2 ARM7TDMI Processor

For further details on ARM7TDMI, refer to the following ARM documents:

ARM Architecture Reference Manual (DDI 0100E)

ARM7TDMI Technical Reference Manual (DDI 0210B)

### 11.2.1 Instruction Type

Instructions are either 32 bits long (in ARM state) or 16 bits long (in THUMB state).

### 11.2.2 Data Type

ARM7TDMI supports byte (8-bit), half-word (16-bit) and word (32-bit) data types. Words must be aligned to four-byte boundaries and half words to two-byte boundaries.

Unaligned data access behavior depends on which instruction is used where.

### 11.2.3 ARM7TDMI Operating Mode

The ARM7TDMI, based on ARM architecture v4T, supports seven processor modes:

**User**: The normal ARM program execution state

**FIQ**: Designed to support high-speed data transfer or channel process

**IRQ**: Used for general-purpose interrupt handling

**Supervisor**: Protected mode for the operating system

**Abort mode**: Implements virtual memory and/or memory protection

**System**: A privileged user mode for the operating system

**Undefined**: Supports software emulation of hardware coprocessors

Mode changes may be made under software control, or may be brought about by external interrupts or exception processing. Most application programs execute in User mode. The non-user modes, or privileged modes, are entered in order to service interrupts or exceptions, or to access protected resources.

### 11.2.4 ARM7TDMI Registers

The ARM7TDMI processor has a total of 37registers:

- 31 general-purpose 32-bit registers
- 6 status registers

These registers are not accessible at the same time. The processor state and operating mode determine which registers are available to the programmer.

At any one time 16 registers are visible to the user. The remainder are synonyms used to speed up exception processing.

Register 15 is the Program Counter (PC) and can be used in all instructions to reference data relative to the current instruction.

R14 holds the return address after a subroutine call.

R13 is used (by software convention) as a stack pointer.

Registers R0 to R7 are unbanked registers. This means that each of them refers to the same 32-bit physical register in all processor modes. They are general-purpose registers, with no special uses managed by the architecture, and can be used wherever an instruction allows a general-purpose register to be specified.

Registers R8 to R14 are banked registers. This means that each of them depends on the current mode of the processor.

**Table 11-1. ARM7TDMI ARM Modes and Registers Layout**

| User and System Mode | Supervisor Mode | Abort Mode | Undefined Mode | Interrupt Mode | Fast Interrupt Mode |
|---|---|---|---|---|---|
| R0 | R0 | R0 | R0 | R0 | R0 |
| R1 | R1 | R1 | R1 | R1 | R1 |
| R2 | R2 | R2 | R2 | R2 | R2 |
| R3 | R3 | R3 | R3 | R3 | R3 |
| R4 | R4 | R4 | R4 | R4 | R4 |
| R5 | R5 | R5 | R5 | R5 | R5 |
| R6 | R6 | R6 | R6 | R6 | R6 |
| R7 | R7 | R7 | R7 | R7 | R7 |
| R8 | R8 | R8 | R8 | R8 | R8_FIQ |
| R9 | R9 | R9 | R9 | R9 | R9_FIQ |
| R10 | R10 | R10 | R10 | R10 | R10_FIQ |
| R11 | R11 | R11 | R11 | R11 | R11_FIQ |
| R12 | R12 | R12 | R12 | R12 | R12_FIQ |
| R13 | R13_SVC | R13_ABORT | R13_UNDEF | R13_IRQ | R13_FIQ |
| R14 | R14_SVC | R14_ABORT | R14_UNDEF | R14_IRQ | R14_FIQ |
| PC | PC | PC | PC | PC | PC |
| CPSR | CPSR | CPSR | CPSR | CPSR | CPSR |
| | SPSR_SVC | SPSR_ABORT | SPSR_UNDEF | SPSR_IRQ | SPSR_FIQ |

Mode-specific banked registers

#### 11.2.4.1 Modes and Exception Handling

All exceptions have banked registers for R14 and R13.

After an exception, R14 holds the return address for exception processing. This address is used to return after the exception is processed, as well as to address the instruction that caused the exception.

R13 is banked across exception modes to provide each exception handler with a private stack pointer.

The fast interrupt mode also banks registers 8 to 12 so that interrupt processing can begin without having to save these registers.

A seventh processing mode, System Mode, does not have any banked registers. It uses the User Mode registers. System Mode runs tasks that require a privileged processor mode and allows them to invoke all classes of exceptions.

#### 11.2.4.2 Status Registers

All other processor states are held in status registers. The current operating processor status is in the Current Program Status Register (CPSR). The CPSR holds:

- four ALU flags (Negative, Zero, Carry, and Overflow)
- two interrupt disable bits (one for each type of interrupt)
- one bit to indicate ARM or Thumb execution
- five bits to encode the current processor mode

All five exception modes also have a Saved Program Status Register (SPSR) that holds the CPSR of the task immediately preceding the exception.

### 13.2.4.5 Watchdog Reset

The Watchdog Reset is entered when a watchdog fault occurs. This state lasts 3 Slow Clock cycles.

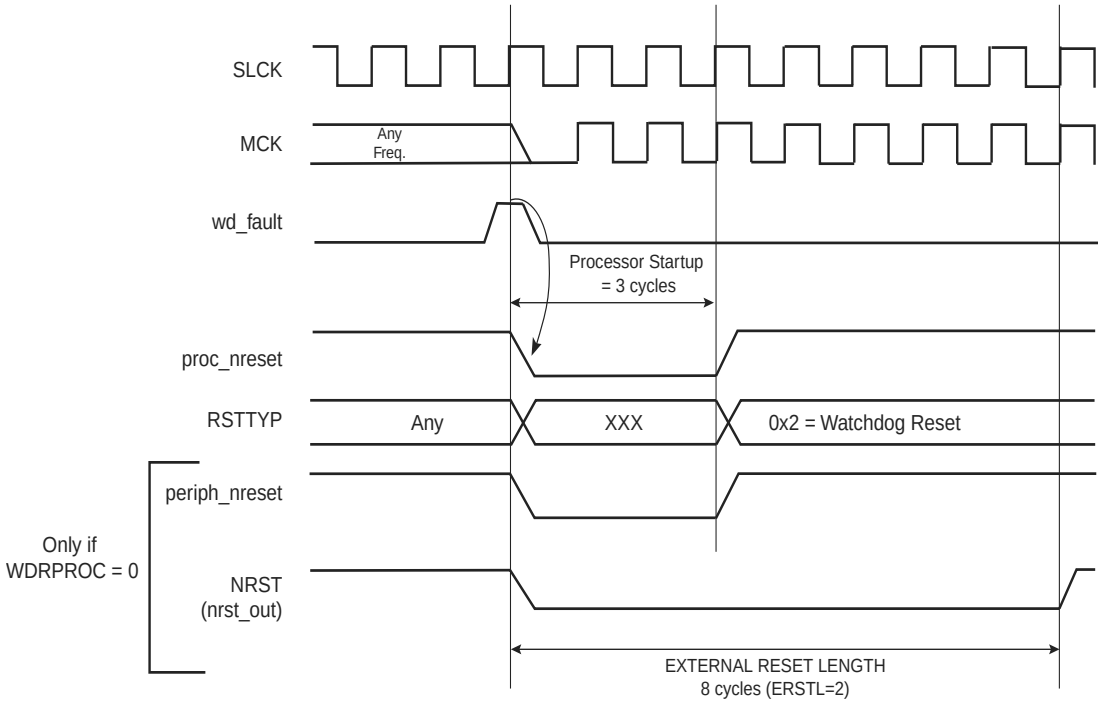
When in Watchdog Reset, assertion of the reset signals depends on the WDRPROC bit in WDT_MR:

- If WDRPROC is 0, the Processor Reset and the Peripheral Reset are asserted. The NRST line is also asserted, depending on the programming of the field ERSTL. However, the resulting low level on NRST does not result in a User Reset state.
- If WDRPROC = 1, only the processor reset is asserted.

The Watchdog Timer is reset by the proc_nreset signal. As the watchdog fault always causes a processor reset if WDRSTEN is set, the Watchdog Timer is always reset after a Watchdog Reset, and the Watchdog is enabled by default and with a period set to a maximum.

When the WDRSTEN in WDT_MR bit is reset, the watchdog fault has no impact on the reset controller.

**Figure 13-8. Watchdog Reset**



### 22.4.9 PDC Transfer Control Register

**Register Name:** PERIPH_PTCR

**Access Type:** Write-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | TXTDIS | TXTEN |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | – | – | RXTDIS | RXTEN |

- **RXTEN: Receiver Transfer Enable**

0 = No effect.

1 = Enables the receiver PDC transfer requests if RXTDIS is not set.

- **RXTDIS: Receiver Transfer Disable**

0 = No effect.

1 = Disables the receiver PDC transfer requests.

- **TXTEN: Transmitter Transfer Enable**

0 = No effect.

1 = Enables the transmitter PDC transfer requests.

- **TXTDIS: Transmitter Transfer Disable**

0 = No effect.

1 = Disables the transmitter PDC transfer requests

Moreover, like the PCK, a status bitin PMC_SR indicates that the Programmable Clock is actually what has been programmed in the Programmable Clock registers.

As the Programmable Clock Controller does not manage with glitch prevention when switching clocks, it is strongly recommended to disable the Programmable Clock before any configuration change and to re-enable it after the change is actually performed.

## 25.7 Programming Sequence

1. Enabling the Main Oscillator:

   The main oscillator is enabled by setting the MOSCEN field in the CKGR_MOR register. In some cases it may be advantageous to define a start-up time. This can be achieved by writing a value in the OSCOUNT field in the CKGR_MOR register.

   Once this register has been correctly configured, the user must wait for MOSCS field in the PMC_SR register to be set. This can be done either by polling the status register or by waiting the interrupt line to be raised if the associated interrupt to MOSCS has been enabled in the PMC_IER register.

   Code Example:

   ```
   write_register(CKGR_MOR,0x00000701)
   ```

   Start Up Time = 8 * OSCOUNT / SLCK = 56 Slow Clock Cycles.

   So, the main oscillator will be enabled (MOSCS bit set) after 56 Slow Clock Cycles.

2. Checking the Main Oscillator Frequency (Optional):

   In some situations the user may need an accurate measure of the main oscillator frequency. This measure can be accomplished via the CKGR_MCFR register.

   Once the MAINRDY field is set in CKGR_MCFR register, the user may read the MAINF field in CKGR_MCFR register. This provides the number of main clock cycles within sixteen slow clock cycles.

3. Setting PLL and divider:

   All parameters needed to configure PLL and the divider are located in the CKGR_PLLR register.

   The DIV field is used to control divider itself. A value between 0 and 255 can be programmed. Divider output is divider input divided by DIV parameter. By default DIV parameter is set to 0 which means that divider is turned off.

   The OUT field is used to select the PLL B output frequency range.

   The MUL field is the PLL multiplier factor. This parameter can be programmed between 0 and 2047. If MUL is set to 0, PLL will be turned off, otherwise the PLL output frequency is PLL input frequency multiplied by (MUL + 1).

   The PLLCOUNT field specifies the number of slow clock cycles before LOCK bit is set in the PMC_SR register after CKGR_PLLR register has been written.

   Once the PMC_PLL register has been written, the user must wait for the LOCK bit to be set in the PMC_SR register. This can be done either by polling the status register or by waiting the interrupt line to be raised if the associated interrupt to LOCK has been enabled in the PMC_IER register. All parameters in CKGR_PLLR can be programmed in a single write operation. If at some stage one of the following parameters, MUL, DIV is modified, LOCK bit will go low to indicate that PLL is not ready yet. When PLL is locked, LOCK will be set again. The user is constrained to wait for LOCK bit to be set before using the PLL output clock.

   The USBDIV field is used to control the additional divider by 1, 2 or 4, which generates the USB clock(s).

   Code Example:

### 28.7.2 SPI Mode Register

**Name:** SPI_MR

**Access Type:** Read-write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| DLYBCS | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | PCS | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LLB | – | – | MODFDIS | | PCSDEC | PS | MSTR |

- **MSTR: Master/Slave Mode**

0 = SPI is in Slave mode.

1 = SPI is in Master mode.

- **PS: Peripheral Select**

0 = Fixed Peripheral Select.

1 = Variable Peripheral Select.

- **PCSDEC: Chip Select Decode**

0 = The chip selects are directly connected to a peripheral device.

1 = The four chip select lines are connected to a 4- to 16-bit decoder.

When PCSDEC equals one, up to 15 Chip Select signals can be generated with the four lines using an external 4- to 16-bit decoder. The Chip Select Registers define the characteristics of the 15 chip selects according to the following rules:

SPI_CSR0 defines peripheral chip select signals 0 to 3.

SPI_CSR1 defines peripheral chip select signals 4 to 7.

SPI_CSR2 defines peripheral chip select signals 8 to 11.

SPI_CSR3 defines peripheral chip select signals 12 to 14.

- **MODFDIS: Mode Fault Detection**

0 = Mode fault detection is enabled.

1 = Mode fault detection is disabled.

- **LLB: Local Loopback Enable**

0 = Local loopback path disabled.

1 = Local loopback path enabled.

LLB controls the local loopback on the data serializer for testing in Master Mode only. (MISO is internally connected on MOSI.)

- **PCS: Peripheral Chip Select**

This field is only used if Fixed Peripheral Select is active (PS = 0).

If PCSDEC = 0:

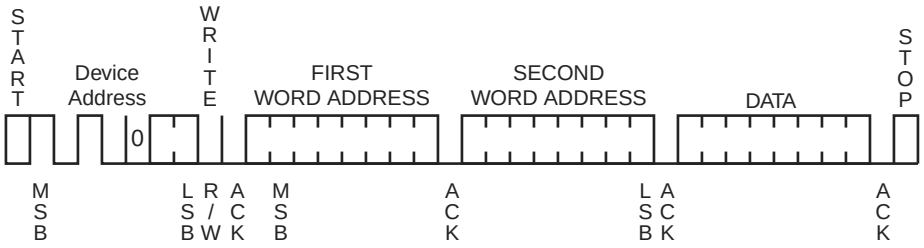
PCS = xxx0 NPCS[3:0] = 1110

PCS = xx01 NPCS[3:0] = 1101

1. Program IADRSZ = 1,
2. Program DADR with 1 1 1 1 0 b1 b2 (b1 is the MSB of the 10-bit address, b2, etc.)
3. Program TWI_IADR with b3 b4 b5 b6 b7 b8 b9 b10 (b10 is the LSB of the 10-bit address)

Figure 29-12 below shows a byte write to an Atmel AT24LC512 EEPROM. This demonstrates the use of internal addresses to access the device.

**Figure 29-12. Internal Address Usage**



### 29.6.10 TWI Transmit Holding Register

**Register Name**: TWI_THR

Access Type: Read-write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TXDATA | | | | | | | |

- **TXDATA: Transmit Holding Data**

### 32.6.9 TC Register C

**Register Name:** TC_RCx [x=0..2]

**Access Type:** Read-write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RC | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC | | | | | | | |

- **RC: Register C**

RC contains the Register C value in real time.

$$\frac{(2 \times CPRD \times DIVA)}{MCK} \text{ or } \frac{(2 \times CPRD \times DIVB)}{MCK}$$

- the ***waveform duty cycle***. This channel parameter is defined in the CDTY field of the PWM_CDTYx register. If the waveform is left aligned then:

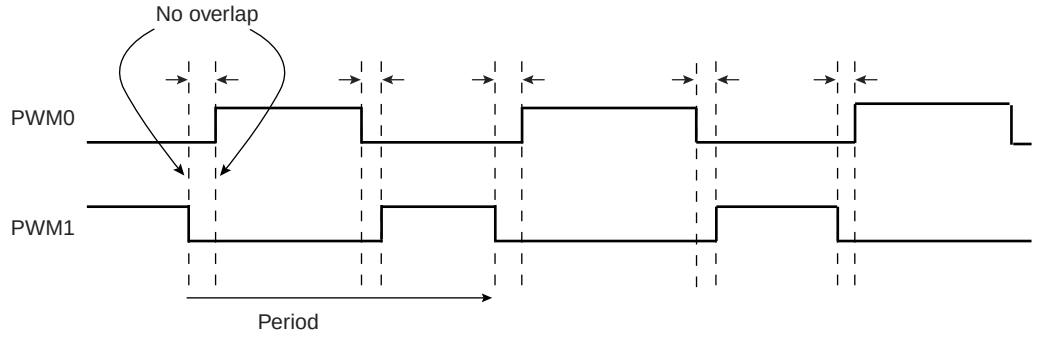
$$\text{duty cycle} = \frac{(period - 1/\text{fchannel\_x\_clock} \times CDTY)}{period}$$

If the waveform is center aligned, then:

$$\text{duty cycle} = \frac{((period/2) - 1/\text{fchannel\_x\_clock} \times CDTY))}{(period/2)}$$

- the ***waveform polarity.*** At the beginning of the period, the signal can be at high or low level. This property is defined in the CPOL field of the PWM_CMRx register. By default the signal starts by a low level.
- the ***waveform alignment***. The output waveform can be left or center aligned. Center aligned waveforms can be used to generate non overlapped waveforms. This property is defined in the CALG field of the PWM_CMRx register. The default mode is left aligned.

**Figure 33-4. Non Overlapped Center Aligned Waveforms**




Note: See Figure 33-5 on page 412 for a detailed description of center aligned waveforms.

When center aligned, the internal channel counter increases up to CPRD and.decreases down to 0. This ends the period.

When left aligned, the internal channel counter increases up to CPRD and is reset. This ends the period.

Thus, for the same CPRD value, the period for a center aligned channel is twice the period for a left aligned channel.

Waveforms are fixed at 0 when:

- CDTY = CPRD and CPOL = 0
- CDTY = 0 and CPOL = 1

Waveforms are fixed at 1 (once the channel is enabled) when:

- CDTY = 0 and CPOL = 0
- CDTY = CPRD and CPOL = 1

The waveform polarity must be set before enabling the channel. This immediately affects the channel output level. Changes on channel polarity are not taken into account while the channel is enabled.

- Configuration of the clock generator if DIVA and DIVB are required
- Selection of the clock for each channel (CPRE field in the PWM_CMRx register)
- Configuration of the waveform alignment for each channel (CALG field in the PWM_CMRx register)
- Configuration of the period for each channel (CPRD in the PWM_CPRDx register). Writing in PWM_CPRDx Register is possible while the channel is disabled. After validation of the channel, the user must use PWM_CUPDx Register to update PWM_CPRDx as explained below.
- Configuration of the duty cycle for each channel (CDTY in the PWM_CDTYx register). Writing in PWM_CDTYx Register is possible while the channel is disabled. After validation of the channel, the user must use PWM_CUPDx Register to update PWM_CDTYx as explained below.
- Configuration of the output waveform polarity for each channel (CPOL in the PWM_CMRx register)
- Enable Interrupts (Writing CHIDx in the PWM_IER register)
- Enable the PWM channel (Writing CHIDx in the PWM_ENA register)

It is possible to synchronize different channels by enabling them at the same time by means of writing simultaneously several CHIDx bits in the PWM_ENA register.

- In such a situation, all channels may have the same clock selector configuration and the same period specified.

#### 33.5.3.2 Source Clock Selection Criteria

The large number of source clocks can make selection difficult. The relationship between the value in the Period Register (PWM_CPRDx) and the Duty Cycle Register (PWM_CDTYx) can help the user in choosing. The event number written in the Period Register gives the PWM accuracy. The Duty Cycle quantum cannot be lower than *1/PWM_CPRDx* value. The higher the value of PWM_CPRDx, the greater the PWM accuracy.

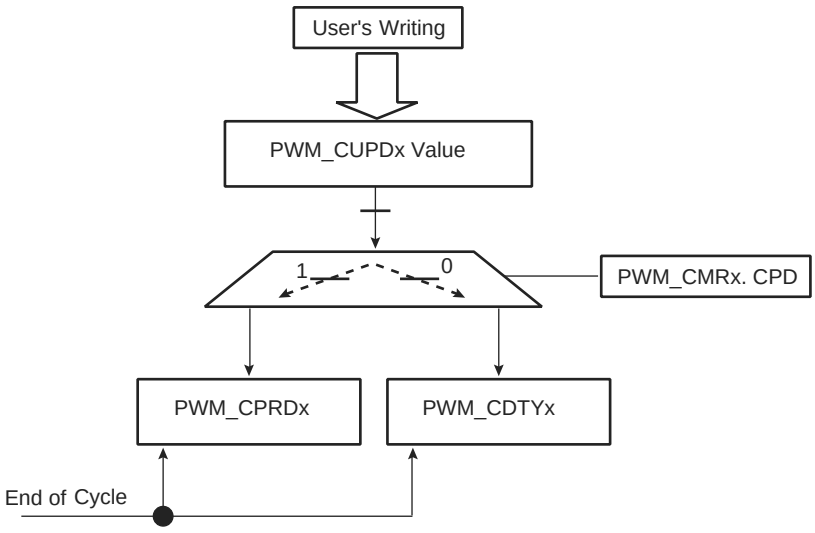
For example, if the user sets 15 (in decimal) in PWM_CPRDx, the user is able to set a value between 1 up to 14 in PWM_CDTYx Register. The resulting duty cycle quantum cannot be lower than 1/15 of the PWM period.

#### 33.5.3.3 Changing the Duty Cycle or the Period

It is possible to modulate the output waveform duty cycle or period.

To prevent unexpected output waveform, the user must use the update register (PWM_CUPDx) to change waveform parameters while the channel is still enabled. The user can write a new period value or duty cycle value in the update register (PWM_CUPDx). This register holds the new value until the end of the current cycle and updates the value for the next cycle. Depending on the CPD field in the PWM_CMRx register, PWM_CUPDx either updates PWM_CPRDx or PWM_CDTYx. Note that even if the update register is used, the period must not be smaller than the duty cycle.

**Figure 33-6. Synchronized Period or Duty Cycle Update**



A form error results from violations on one or more of the fixed form of the following bit fields:

- CRC delimiter
- ACK delimiter
- End of frame
- Error delimiter
- Overload delimiter

This flag is automatically cleared by reading CAN_SR register.

- **BERR: Bit Error**

0 = No bit error occurred during a previous transfer.

1 = A bit error occurred during a previous transfer.

A bit error is set when the bit value monitored on the line is different from the bit value sent.

This flag is automatically cleared by reading CAN_SR register.

- **RBSY: Receiver busy**

0 = CAN receiver is not receiving a frame.

1 = CAN receiver is receiving a frame.

Receiver busy. This status bit is set by hardware while CAN receiver is acquiring or monitoring a frame (remote, data, overload or error frame). It is automatically reset when CAN is not receiving.

- **TBSY: Transmitter busy**

0 = CAN transmitter is not transmitting a frame.

1 = CAN transmitter is transmitting a frame.

Transmitter busy. This status bit is set by hardware while CAN transmitter is generating a frame (remote, data, overload or error frame). It is automatically reset when CAN is not transmitting.

- **OVLSY: Overload busy**

0 = CAN transmitter is not transmitting an overload frame.

1 = CAN transmitter is transmitting a overload frame.

It is automatically reset when the bus is not transmitting an overload frame.

### 37.5.6 Transmit Buffer Queue Pointer Register

**Register Name:** EMAC_TBQP

**Access Type:** Read-write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| ADDR | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| ADDR | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ADDR | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADDR | | | | | | – | – |

This register points to the entry in the transmit buffer queue (descriptor list) currently being used. It is written with the start location of the transmit buffer descriptor list. The lower order bits increment as buffers are used up and wrap to their original values after either 1024 buffers or when the wrap bit of the entry is set. This register can only be written when bit 3 in the transmit status register is low.

As transmit buffer reads consist of bursts of two words, it is recommended that bit 2 is always written with zero to prevent a burst crossing a 1K boundary, in violation of section 3.6 of the AMBA specification.

- **ADDR: Transmit buffer queue pointer address**

Written with the address of the start of the transmit queue, reads as a pointer to the first buffer of the frame being transmitted or about to be transmitted.

# 38. SAM7X512/256/128 Electrical Characteristics

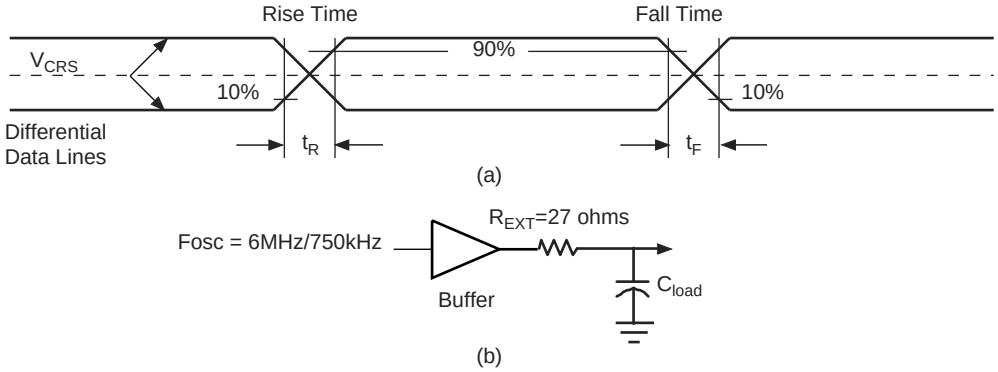
## 38.1 Absolute Maximum Ratings

**Table 38-1. Absolute Maximum Ratings***

| |
|---|
| Operating Temperature (Industrial).....-40°C to + 85°C |
| Storage Temperature.....-60°C to + 150°C |
| Voltage on Input Pins<br>with Respect to Ground.....-0.3V to + 5.5V |
| Maximum Operating Voltage<br>(VDDCORE, and VDDPLL).....2.0V |
| Maximum Operating Voltage<br>(VDDIO, VDDIN and VDDFLASH).....4.0V |
| Total DC Output Current on all I/O lines<br>100-lead LQFP package.....200 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 38-3. USB Data Signal Rise and Fall Times**



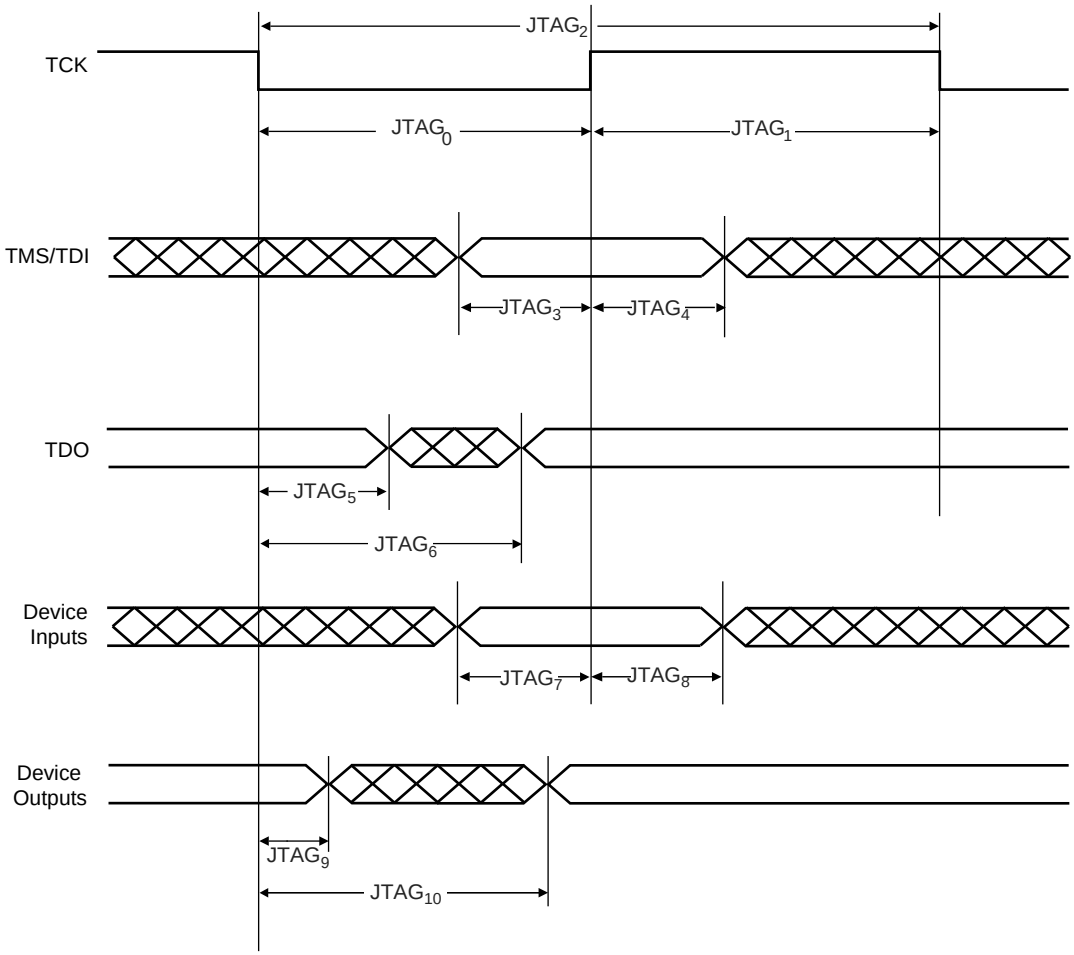
### 38.8.6.2 JTAG Interface Signals

**Table 38-28. JTAG Interface Timing specification**

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $JTAG_0$ | TCK Low Half-period | (1) | 6.5 | | ns |
| $JTAG_1$ | TCK High Half-period | (1) | 5.5 | | ns |
| $JTAG_2$ | TCK Period | (1) | 12 | | ns |
| $JTAG_3$ | TDI, TMS Setup before TCK High | (1) | 2 | | ns |
| $JTAG_4$ | TDI, TMS Hold after TCK High | (1) | 3 | | ns |
| $JTAG_5$ | TDO Hold Time | (1) | 4 | | ns |
| $JTAG_6$ | TCK Low to TDO Valid | (1) | | 16 | ns |
| $JTAG_7$ | Device Inputs Setup Time | (1) | 0 | | ns |
| $JTAG_8$ | Device Inputs Hold Time | (1) | 3 | | ns |
| $JTAG_9$ | Device Outputs Hold Time | (1) | 6 | | ns |
| $JTAG_{10}$ | TCK to Device Outputs Valid | (1) | | 18 | ns |

Note: 1. $V_{VDDIO}$ from 3.0V to 3.6V, maximum external capacitor = 40pF

**Figure 38-11. JTAG Interface Signals**



| Version 6120H | Comments | Change Request Ref. |
|---|---|---|
| | **Overview:** | |
| | Table 3-1, “Signal Description List” footnote added to JTAGSEL, ERASE and TST pin comments. | 5064 |
| | Section 6.1 ”JTAG Port Pins”, Section 6.2 ”Test Pin” and Section 6.4 ”ERASE Pin”, updated. | |
| | Section 8.4.3 ”Internal Flash”, updated: “At any time, the Flash is mapped ... if GPNVM bit 2 is set and before the Remap Command.” | 5850 |
| | Figure 9-1,”System Controller Block Diagram”, RTT is reset by power_on_reset. | 5223 |
| | ”Features”, ”Debug Unit (DBGU)”, added ”Mode for General Purpose 2-wire UART Serial Communication” | 5846 |
| | **ADC:** | |
| | Section 35.6.2 ”ADC Mode Register”, PRESCAL and STARTUP bit fields widened. | 4430 |
| | “SHTIM: Sample & Hold Time” on page 473 formula updated in bit description. | 5254 |
| | Figure 35-1,”Analog-to-Digital Converter Block Diagram”, VDDANA replaced by VDDIN. PMC added to figure. | rfo |
| | Figure 35.5.5,”Conversion Triggers”, update to the third paragraph detailing hardware trigger. | |
| | **AIC:** | |
| | Section 23.8.16 ”AIC Spurious Interrupt Vector Register”, typo fixed in bit fields. (SIQV is SIVR). | 4749 |
| | Section 23.7.5 ”Protect Mode”, writing PROT in AIC_DCR enables protection mode (3rd paragraph). | 5193 |
| | **CAN:** | |
| | Section 36.6.4.6 ”Error Interrupt Handler”, added to datasheet. | 4736 |
| | Section 36.8.5 ”CAN Status Register”, added references to the new chapter in bit descriptions, WARN, BOFF, ERRA, ERP. | |
| | **DBGU:** | |
| | Section 26.1 ”Overview”, ...” two-pin UART can be used standalone for general purpose serial communication.” | 5846 |
| | **FFPI:** | |
| | Section 20.2 ”Parallel Fast Flash Programming”, Section 20.2.1 ”Device Configuration”, added status of PIOs and Crystal Oscillator | 5989 |
| | Section 20.3 ”Serial Fast Flash Programming”, Section 20.3.1 ”Device Configuration”, added status of PIOs and Crystal Oscillator | |
| | **PMC:** | |
| | ”PMC System Clock Enable Register”, ”PMC System Clock Disable Register” and ”PMC System Clock Status Register”, bit field 11 contains PCK3. | 5722 |
| | **PWM:** | |
| | Section 33.6.12 ”PWM Channel Counter Register”, typos corrected in bit description. | 5185 |
| | **RSTC:** | |
| | Section 13.2.4.4 ”Software Reset”, PERRST must be used with PROCRST, except for debug purposes. | |
| | **SSC:** | |
| | Section 31.8.3 ”SSC Receive Clock Mode Register”, corrected bit name to STTDLY. | |