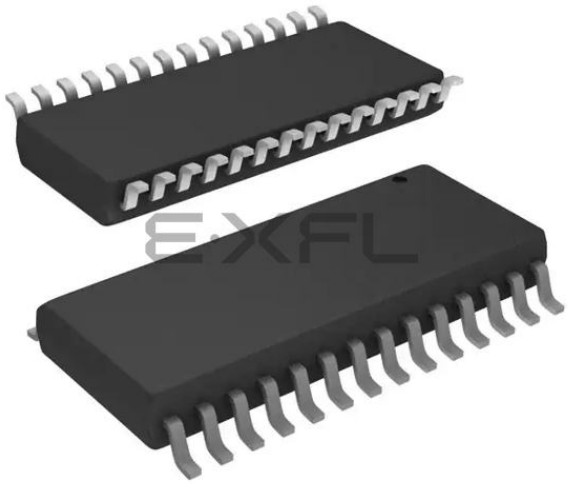


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

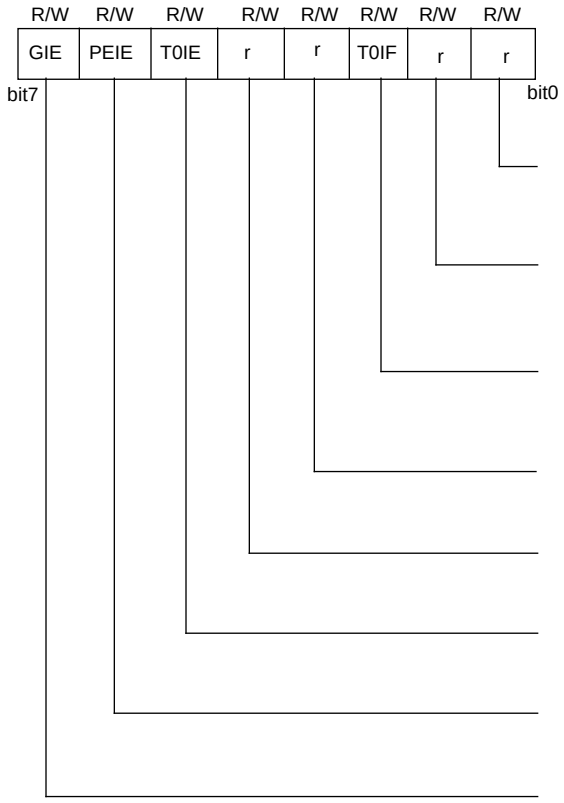
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C
Peripherals	POR, Temp Sensor, WDT
Number of I/O	20
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	Slope A/D
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic14000-04-so

4.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register which contains the various enable and flag bits for the Timer0 overflow and peripheral interrupts. Figure 4-5 shows the bits for the INTCON register.

Note:	The T0IF will be set by the specified condition even if the corresponding Interrupt Enable Bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling interrupt, clear the interrupt flag, to ensure that the program does not immediately branch to the peripheral interrupt service routine

FIGURE 4-5: INTCON REGISTER



Register:	INTCON	W:	Writable
Address:	0Bh or 8Bh	R:	Readable
POR value:	0000 000xb	U:	Unimplemented, read as '0'

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

T0IF: TMR0 overflow interrupt flag

1 = The TMR0 has overflowed
Must be cleared by software
0 = TMR0 did not overflow

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

Reserved. This bit should be programmed as '0'. Use of this bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

T0IE: TMR0 interrupt enable bit

1 = Enables T0IF interrupt
0 = Disables T0IF interrupt

PEIE: Peripheral interrupt enable bit

1 = Enables all un-masked peripheral interrupts
0 = Disables all peripheral interrupts

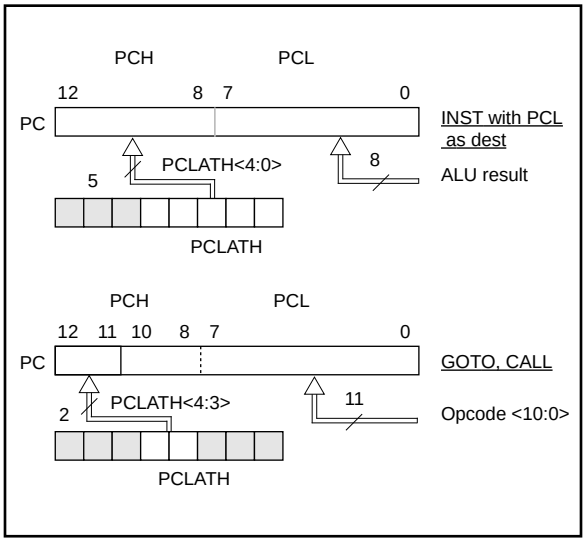
GIE: Global interrupt enable

1 = Enables all un-masked interrupts
0 = Disables all interrupts

4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte, PCL, is a readable and writable register. The high byte of the PC (PCH) is not directly readable or writable. PCLATH is a holding register for PC<12:8> where contents are transferred to the upper byte of the program counter. When PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH as shown in Figure 4-9.

FIGURE 4-9: LOADING OF PC IN DIFFERENT SITUATIONS



Note: On POR, the contents of the PCLATH register are unknown. The PCLATH should be initialized before a CALL, GOTO, or any instruction that modifies the PCL register is executed.

4.3.1 COMPUTED GOTO

When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note “Table Read Using the PIC16CXX”(AN556).

4.3.2 STACK

The PIC14000 has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed in the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a “PUSH” or a “POP” operation.

The stack operates as a circular buffer. This means that after the stack has been “PUSHed” eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no STATUS bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instruction mnemonics called PUSH nor POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, or RETFIE instructions, or the vectoring to an interrupt address

4.3.3 PROGRAM MEMORY PAGING

The PIC14000 has 4K of program memory, but the CALL and GOTO instructions only have a 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 4K program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (Figure 4-9). When doing a CALL or GOTO instruction, the user must ensure that this page bit (PCLATH<3>) is programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<3> is not required for the return instructions (which pops the PC from the stack).

Note: The PIC14000 ignores the PCLATH<4> bit, which is used for program memory pages 2 and 3 (1000h-1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0X500
BSF     PCLATH, 3 ; Select page 1 (800h-FFFh)
CALL    SUB1_P1   ; Call subroutine in
        :         ; page 1 (800h-FFFh)
        :
        :
ORG 0X900
SUB1 P1 :         ; called subroutine
        :         ; page 1 (800h-FFFh)
        :
RETURN            ; return to page 0
                  ; (000h-7FFh)
```

5.2.1 TRISC PORTC DATA DIRECTION REGISTER

This register defines each pin of PORTC as either an input or output under software control. A '1' in each location configures the corresponding port pin as an input. This register resets to all '1's, meaning all PORTC pins are initially inputs. The data register should be initialized prior to configuring the port as outputs.

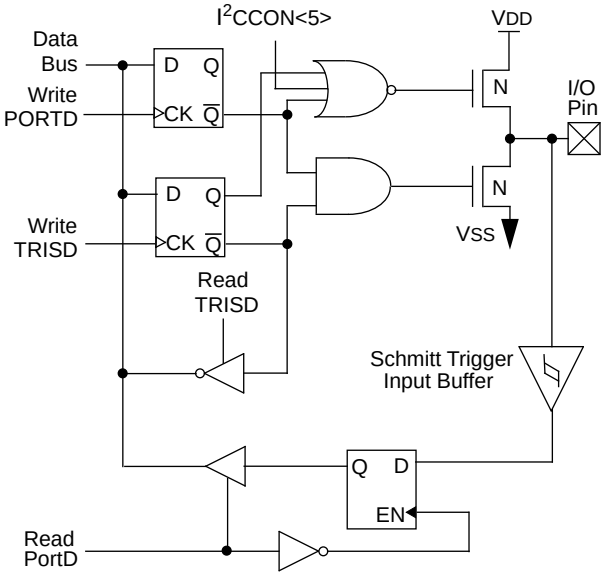
FIGURE 5-7: TRISC REGISTER

87h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value FFh	1	1	1	1	1	1	1	1

Bit	Name	Function
B7	TRISC7	Control direction on pin RC7/SDAA (has no effect if I^2C is enabled): 0 = pin is an output 1 = pin is an input
B6	TRISC6	Control direction on pin RC6/SCLA (has no effect if I^2C is enabled): 0 = pin is an output 1 = pin is an input
B5	TRISC5	Control direction on pin RC5: 0 = pin is an output 1 = pin is an input
B4	TRISC4	Control direction on pin RC4: 0 = pin is an output 1 = pin is an input
B3	TRISC3	Control direction on pin RC3: 0 = pin is an output 1 = pin is an input
B2	TRISC2	Control direction on pin RC2: 0 = pin is an output 1 = pin is an input
B1	TRISC1	Control direction on pin RC1/CMPA (has no effect if the CMAOE bit is set): 0 = pin is an output 1 = pin is an input
B0	TRISC0	Control direction on pin RC0/REFA (has no effect if the CMAOE bit is set): 0 = pin is an output 1 = pin is an input

U= unimplemented, X = unknown.

FIGURE 5-10: BLOCK DIAGRAM OF PORTD<1:0> PINS



Note: I/O pins have protection diodes to VDD and VSS. These pins do not have a P-channel pull-up.

FIGURE 5-11: PORTD DATA REGISTER

08h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTD	RD7/AN7	RD6/AN6	RD5/AN5	RD4/AN4	RD3/REFB	RD2/CMPB	RD1/SDAB	RD0/SCLB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value xxh	X	X	X	X	X	X	X	X

Bit	Name	Function
B7	RD7/AN7	GPIO or analog input. Returns value on pin RD7/AN7 when used as a digital input. When configured as an analog input, reads as '0'.
B6	RD6/AN6	GPIO or analog input. Returns value on pin RD6/AN6 when used as a digital input. When configured as an analog input, reads as '0'.
B5	RD5/AN5	GPIO or analog input. This pin can connect to a level shift network. If enabled, a +0.5V offset is added to the input voltage. When configured as an analog input, reads as '0'.
B4	RD4/AN4	GPIO or analog input. Returns value on pin RD4/AN4 when used as a digital input. When configured as an analog input, reads as '0'.
B3	RD3/REFB	This pin can serve as a GPIO, or programmable reference B output.
B2	RD2/CMPB	This pin can serve as a GPIO, or comparator B output.
B1	RD1/SDAB	Alternate synchronous serial data I/O for I^2C interface enabled by setting the I^2CSEL bit in the MISC register. This pin can also serve as a general purpose I/O. This pin has an N-channel pull-up to VDD which is disabled in I^2C mode.
B0	RD0/SCLB	Alternate synchronous serial clock for I^2C interface, enabled by setting the I^2CSEL bit in the MISC register. This pin can also serve as a general purpose I/O. This pin has an N-Channel pull-up to VDD which is disabled in I^2C mode.

Legend: U = unimplemented, read as '0', x = unknown.

If the CMBOE bit (CMCON<5>) is set, the RD3/REFB pin becomes the programmable reference B output and pin RD2/CMPB becomes the comparator B output.

Note:	Setting CMBOE changes the definition of RD3/REFB and RD2/CMPB, bypassing the PORTD data and TRISD register settings.

PORTD<1:0> also serve multiple functions. These pins act as the I^2C data and clock lines when the I^2C module is enabled.

The TRISD register controls the direction of the Port D pins. A '1' in each location configures the corresponding port pin as an input. Upon reset, this register sets to FFh, meaning all PORTD pins are initially inputs. The data register should be initialized prior to configuring the port as outputs.

Unused inputs should not be left floating to avoid leakage currents. All pins have input protection diodes to V_{DD} and V_{SS}.

EXAMPLE 5-3: INITIALIZING PORTD

```
CLRF   PORTD        ; Initialize PORTD data
                    ;    latches before setting
                    ;    the data direction
                    ;    register
BSF    STATUS, RP0  ; Select Bank1
MOVLW  0xFF         ; Value used to initialize
                    ; data direction
MOVWF  TRISD        ; Set RD<7:0> as inputs
```

5.4 I/O Programming Considerations

5.4.1 BI-DIRECTIONAL I/O PORTS

Reading the port register reads the values of the port pins. Writing to the port register writes the value to the port latch. Some instructions operate internally as read-modify-write. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation, and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTC will cause all eight bits of PORTC to be read into the CPU. Then the BSF operation takes place on bit5 and PORTC is written to the output latches. If another bit of PORTC is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

A pin actively outputting a LOW or HIGH should not be driven from external devices at the same time in order to change the level on this pin ("wire-or", "wire-and"). The resulting high output currents may damage the chip.

Example 5-4 shows the effect of two sequential read modify write instructions (ex. BCF, BSF, etc.) on an I/O Port.

EXAMPLE 5-4: READ MODIFY WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings:   PORTC<7:4> Inputs
;
;                          PORTC<3:0> Outputs
; PORTC<7:6> have external pull-up and are not
; connected to other circuitry
;
;                          PORT  latch  PORT pins
;                          ----------   ----------

   BCF  PORTC, 7          ; 01pp  pppp   11pp pppp
   BCF  PORTC, 6          ; 10pp  pppp   11pp pppp
   BSF  STATUS,RP0        ;
   BCF  TRISC, 7          ; 10pp  pppp   11pp pppp
   BCF  TRISC, 6          ; 10pp  pppp   10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused
; RC7 to be latched as the pin value (High).
```

When a master does not wish to relinquish the bus (by generating a STOP condition), a repeated START (Sr) must be generated. This condition is identical to the START (SDA goes high-to-low while SCL is high), but occurs after a data transfer acknowledge pulse (not the bus-free state). This allows a master to send "commands" to the slave and then receive the requested information or to address a different slave device. This sequence is shown in Figure 7-10.

FIGURE 7-8: MASTER - TRANSMITTER SEQUENCE

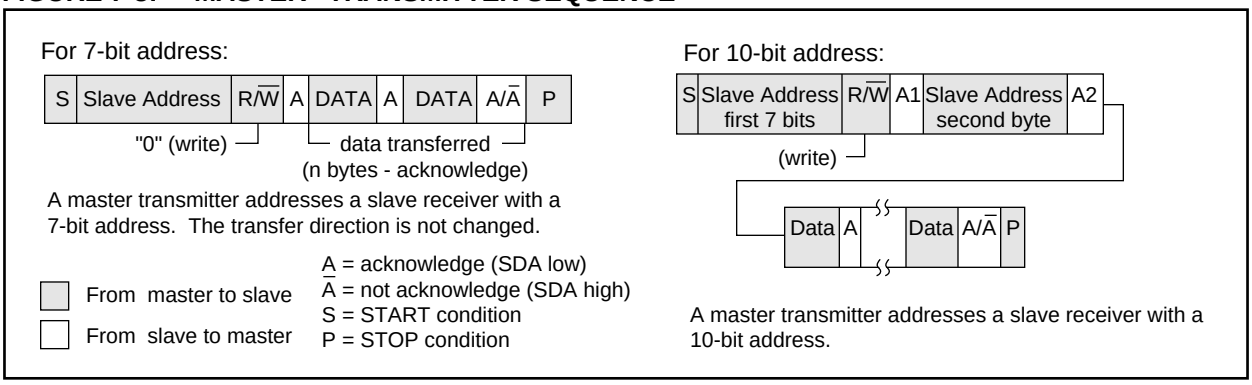


FIGURE 7-9: MASTER - RECEIVER SEQUENCE

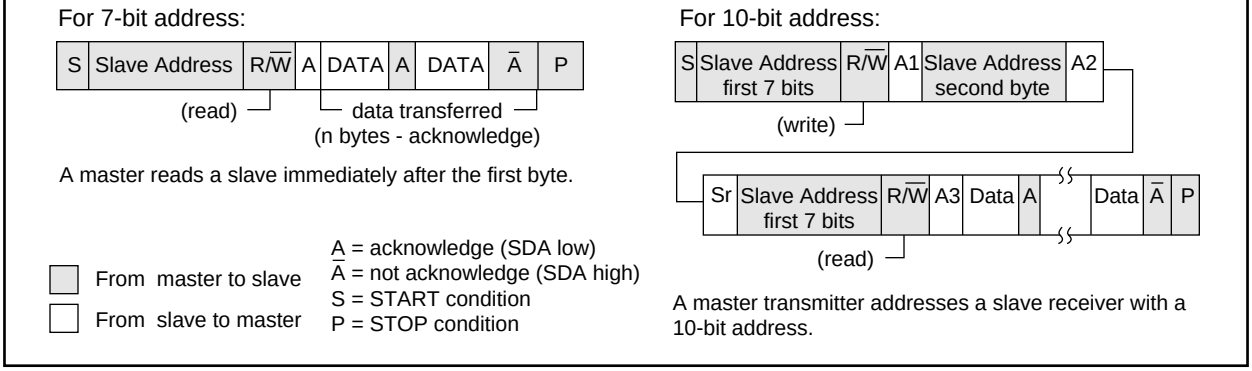
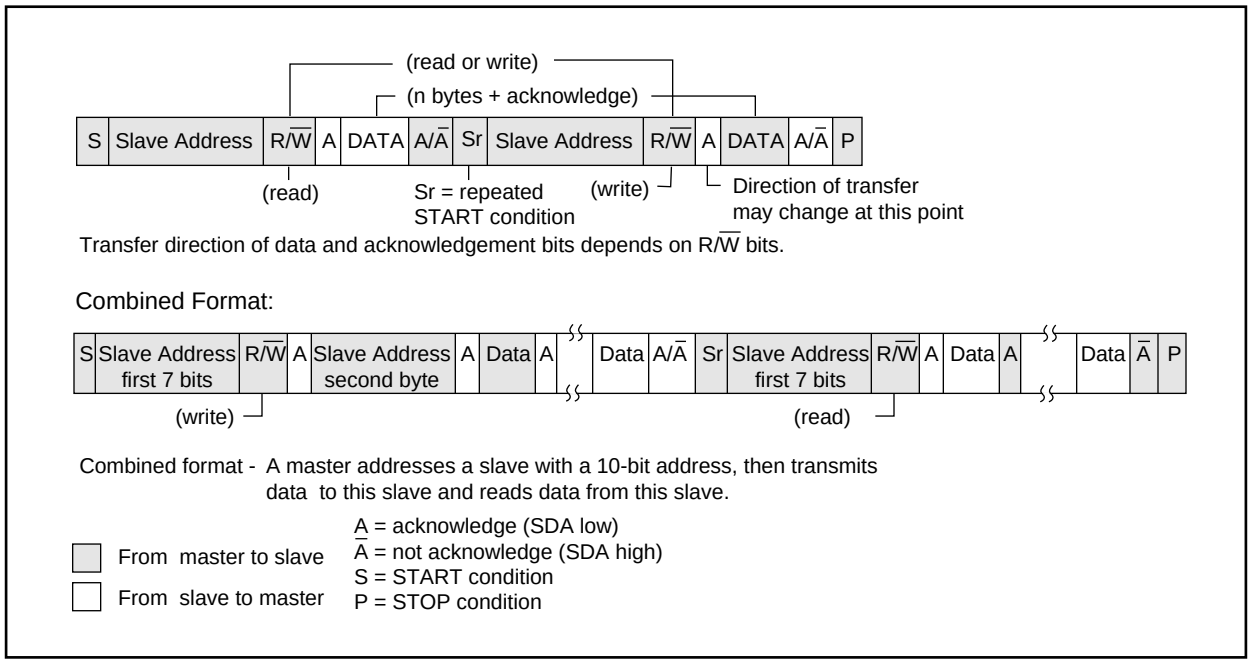


FIGURE 7-10: COMBINED FORMAT



8.6 Programmable Current Source

Four configuration bits (ADCON1<7:4>) are used to control a programmable current source for generating the ramp voltage to the A/D comparator. It allows compensation for full-scale input voltage, clock frequency and CDAC capacitor tolerance variations. The current values range from 0 to 33.75 μA (nominal) in 2.25 μA increments. The intermediate values of the current source are as follows:

TABLE 8-2: PROGRAMMABLE CURRENT SOURCE SELECTION

ADCON1<7:4>				Current Source Output
0	0	0	0	OFF - all current sources disabled
0	0	0	1	2.25 μA
0	0	1	0	4.5 μA
0	0	1	1	6.75 μA
0	1	0	0	9 μA
0	1	0	1	11.25 μA
0	1	1	0	13.5 μA
0	1	1	1	15.75 μA
1	0	0	0	18 μA
1	0	0	1	20.25 μA
1	0	1	0	22.5 μA
1	0	1	1	24.75 μA
1	1	0	0	27 μA
1	1	0	1	29.25 μA
1	1	1	0	31.5 μA
1	1	1	1	33.75 μA

The programmable current source output is tied to the CDAC pin and is used to charge an external capacitor to generate the ramp voltage for the A/D comparator. (Refer to Figure 8-1.) This capacitor should have a low voltage-coefficient as found in teflon, polypropylene, or polystyrene capacitors, for optimum results. The capacitor must be discharged at the beginning of each conversion cycle by asserting ADRST (ADCON0<1>) for at least 200 μs to allow a complete discharge. Asserting ADRST disables the current sources internally. Current flow begins when ADRST is cleared.

TABLE 8-4: A/D CONTROL AND STATUS REGISTER 1

9Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCON1	ADDAC3	ADDAC2	ADDAC1	ADDAC0	PCFG3	PCFG2	PCFG1	PCFG0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

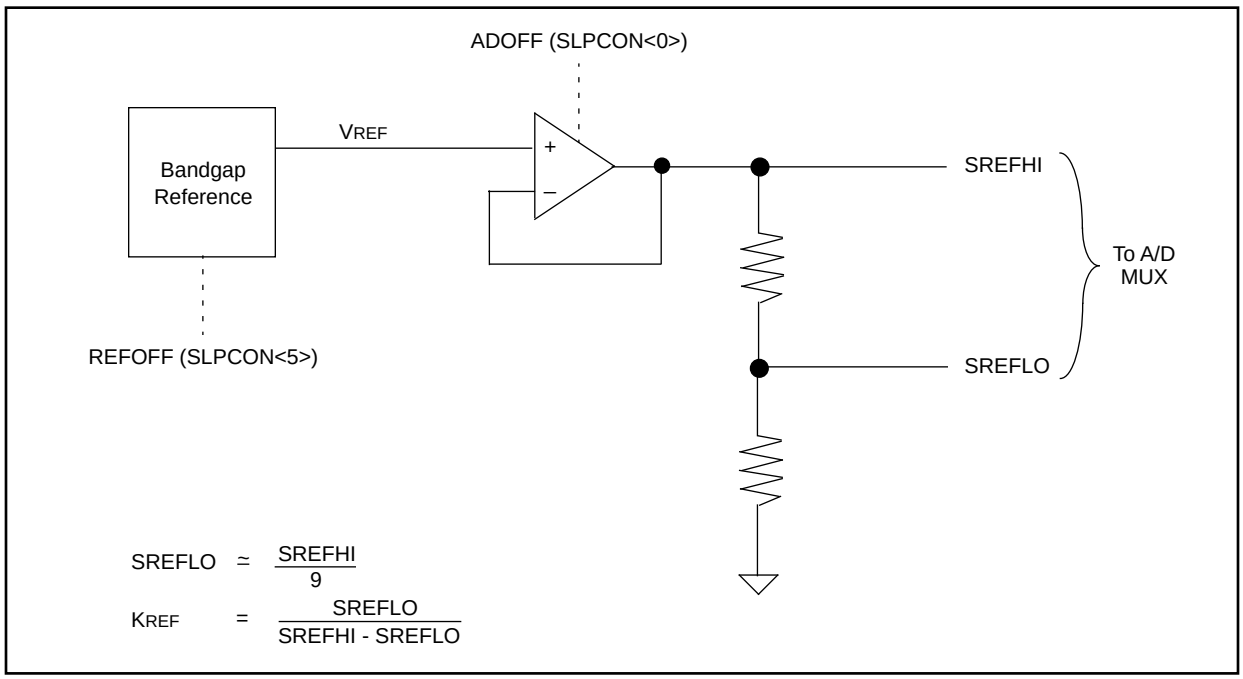
Bit	Name	Function
B7-B4	ADDAC3 ADDAC2 ADDAC1 ADDAC0	A/D Current Source Selects. Refer to Table 8-2.
B3-B2	PCFG3 PCFG2	PORTD Configuration Selects (See Table 8-5)
B1-B0	PCFG1 PCFG0	PORTA Configuration Selects (See Table 8-5)

TABLE 8-5: PORTA AND PORTD CONFIGURATION

ADCON1<1:0>	RA0/AN0	RA1/AN1	RA2/AN2	RA3/AN3
ADCON1<3:2>	**RD4/AN4**	**RD5/AN5**	**RD6/AN6**	**RD7/AN7**
0 0	A	A	A	A
0 1	A	A	A	D
1 0	A	A	D	D
1 1	D	D	D	D

Legend: A = Analog input, D = Digital I/O

FIGURE 9-2: SLOPE REFERENCE DIVIDER



9.5 Comparator and Programmable Reference Modules

9.5.1 COMPARATORS

The PIC14000 includes two independent low-power comparators for comparing the programmable reference outputs to either the RA1/AN1 or RA5/AN5 pins. The negative input of each comparator is tied to one of the reference outputs as shown in Figure 9-3. The comparator positive inputs are connected to the output of the RA1/AN1 and RA5/AN5 level-shift networks.

At reset, the RA1/AN1 level-shift output is connected to the positive inputs of both comparators. This allows a window comparison of the RA1/AN1 voltage using the two programmable references and comparators. Setting CMBOE (CMCON<5>) changes the configuration so that RA1/AN1 and RA5/AN5 may be independently monitored.

The comparator outputs can be read by the CMAOUT (CMCON<2>) and CMBOUT (CMCON<6>) bits. These are read-only bits and writes to these locations have no effect.

Either a rising or falling comparator output can generate an interrupt to the CPU as controlled by the polarity bits CPOLA (CMCON<0>) and CPOLB (CMCON<4>). The CMIF bit (PIR1<7>) interrupt flag is set whenever the exclusive-OR of the comparator output CMxOUT and the CPOLx bits equal a logic one. As with other peripheral interrupts, the corresponding enable bit CMIE (PIE1<7>) must also be set to enable the comparator interrupt. In addition, the global interrupt enable and peripheral interrupt enable bits INTCON<7:6> must also be set. This comparator interrupt is level sensitive.

The comparator outputs are visible at either RC1/CMPA or RD2/CMPB pins by setting the CMAOE (CMCON<1>) or CMBOE (CMCON<5>) bits. Setting CMxOE does not affect the comparator operation. It only enables the pin function regardless of the port TRIS register setting.

Both the references and the comparators are enabled by clearing the CMOFF (SLPCON<2>) bit.

9.5.2 PROGRAMMABLE REFERENCES

The PIC14000 includes two independent, programmable voltage references. Each reference is built using two resistor ladders, bandgap-referenced current source, and analog multiplexers. The first ladder contains 32 taps, and is divided into three ranges (upper, middle, and lower) to provide a coarse voltage adjustment. The coarse ladder includes 1k and 10k resistors yielding a step size of either 5 or 50 mV (nominal) depending on the selected range. Figure 9-8 shows the comparator and reference architecture.

A second ladder contains eight taps, and is connected across the selected coarse ladder resistor to increase resolution. This subdivides the coarse ladder step by approximately 1/8. Thus, resolutions approaching 5/8 mV are obtainable.

TABLE 10-5: RESET CONDITIONS FOR REGISTERS

Register	Address	Power-on Reset	MCLR reset during - normal operation - SLEEP WDT time-out during normal operation	Wake-up from SLEEP through interrupt Wake up from SLEEP through WDT time-out
W	-	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	-	-	-
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000h	0000h	PC + 1(2)
STATUS	03h/83h	0001 1xxx	000? ?uuu(3)	uuu? ?uuu(3)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---- xxxx	---- uuuu	---- uuuu
PORTC	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu(1)
ADTMRL	0Eh	0000 0000	0000 0000	uuuu uuuu
ADTMRH	0Fh	0000 0000	0000 0000	uuuu uuuu
I2CBUF	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
I2CCON	14h	0000 0000	0000 0000	uuuu uuuu
ADCAPL	15h	0000 0000	0000 0000	uuuu uuuu
ADCAPH	16h	0000 0000	0000 0000	uuuu uuuu
ADCON0	1Fh	0000 0010	0000 0010	uuuu uuuu
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	---- 1111	---- 1111	---- uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD	88h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PCON	8Eh	---- --0x	---- --uu	---- --uu
SLPCON	8Fh	0011 1111	0011 1111	uuuu uuuu
I2CADD	93h	0000 0000	0000 0000	uuuu uuuu
I2CSTAT	94h	--00 0000	--00 0000	--uu uuuu
PREFA	9Bh	0000 0000	0000 0000	uuuu uuuu
PREFB	9Ch	0000 0000	0000 0000	uuuu uuuu
CMCON	9Dh	0x00 0x00	0x00 0x00	uuuu uuuu
MISC	9Eh	0000 000x	0000 000x	uuuu uuuu
ADCON1	9Fh	0000 0000	0000 0000	uuuu uuuu

Legend: u=unchanged, x =unknown, - = unimplemented, reads as '0', ? = value depends on condition.

Note 1: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: See Table 10-4 for reset value for specific condition.

FIGURE 10-12: SLPCON REGISTER

8Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLPCON	HIBEN	—	REFOFF	LSOFF	OSCOFF	CMOFF	TEMPOFF	ADOFF
Read/Write	R/W	U	R/W	R/W	R/W	R/W	R/W	R/W
POR value 3Fh	0	0	1	1	1	1	1	1

Bit	Name	Function
B7	HIBEN	Hibernate Mode Select 1 = Hibernate mode enable 0 = Normal operating mode
B6	–	Unimplemented. Read as '0'
B5	REFOFF	References Power Control (bandgap reference, low voltage detector, bias generator) 1 = The references are off 0 = The references are on
B4	LSOFF	Level Shift Network Power Control 1 = The level shift network is off. The RA1/AN1, RD5/AN5 inputs can continue to function as either analog or digital. 0 = The level shift network is on. The signals at the RA1/AN1, RD5/AN5 inputs are level shifted by approximately 0.5V.
B3	OSCOFF	Main Oscillator Power Control 1 = The main oscillator is disabled during SLEEP mode 0 = The main oscillator is running during SLEEP mode for A/D conversions to continue
B2	CMOFF	Programmable Reference and Comparator Power Control 1 = The programmable reference and comparator circuits are off 0 = The programmable reference and comparator circuits are on
B1	TEMPOFF	On-chip Temperature Sensor Power Control 1 = The temperature sensor is off 0 = The temperature sensor is on
B0	ADOFF	A/D Module Power Control (comparator, programmable current source, slope reference voltage divider) 1 = The A/D module power is off 0 = The A/D module power is on

NOP — **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0xx0	0000

Description: No operation.

Words: 1

Cycles: 1

Example

```
NOP
```

RETFIE — **Return from Interrupt**

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → PC,
1 → GIE

Status Affected: None

Encoding:

00	0000	0000	1001

Description: Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
RETFIE
```

After Interrupt
PC = TOS
GIE = 1

OPTION — **Load Option Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

00	0000	0110	0010

Description: The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

RETLW — **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

11	01xx	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
        CALL TABLE      ;W contains table
                        ;offset value
        •               ;W now has table value
        •
        •
TABLE   ADDWF PC        ;W = offset
        RETLW k1        ;Begin table
        RETLW k2        ;
        •
        •
        •
        RETLW kn        ; End of table
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Encoding:

00	0000	0000	1000

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
RETURN
```

After Interrupt

PC = TOS

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

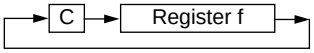
Operation: See description below

Status Affected: C

Encoding:

00	1100	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example

```
RRF             REG1,0
```

Before Instruction

```
REG1    =   1110 0110
C       =   0
```

After Instruction

```
REG1    =   1110 0110
W       =   0111 0011
C       =   0
```

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

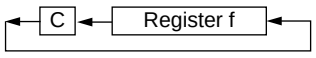
Operation: See description below

Status Affected: C

Encoding:

00	1101	dfff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example

```
RLF             REG1,0
```

Before Instruction

```
REG1    =   1110 0110
C       =   0
```

After Instruction

```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0011

Description: The power-down status bit, $\overline{PD}$ is cleared. Time-out status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See Section 10.8 for more details.

Words: 1

Cycles: 1

Example: SLEEP

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>),
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example

```
SWAPF  REG,   0
```

Before Instruction

REG1 = 0xA5

After Instruction

REG1 = 0xA5
W = 0x5A

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: $5 \le f \le 7$

Operation: (W) → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

XORLW **Exclusive OR Literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example

```
XORLW  0xAF
```

Before Instruction

W = 0xB5

After Instruction

W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example

```
XORWF  REG  1
```

Before Instruction

REG = 0xAF
W = 0xB5

After Instruction

REG = 0x1A
W = 0xB5

13.1 DC Characteristics: PIC14000

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ + 85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD = 2.7V to 6.0V				
Characteristic	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.7	—	6.0	V	IN or HS at Fosc ≤ 4 MHz
		4.5	—	5.5	V	HS at Fosc > 4 MHz
RAM Data Retention Voltage (Note 1)	VDR	—	1.5	—	V	Device in SLEEP mode
VDD start voltage to guarantee Power-On Reset	VPOR	—	VSS	—	V	See section on power-on reset for details
VDD rise rate to guarantee Power-On Reset	SVDD	0.05*	—	—	V/ms	See section on power-on reset for details
Operating Current in SLEEP Mode (Note 2)						
During A/D conversion: all analog on and internal oscillator active	IPD1	—	TBD	900	µA	VDD = 3.0V
	IPD1	—	TBD	1250	µA	VDD = 4.0V
Comparator interrupt enabled: level-shift, programmable reference, and comparator active	IPD2	—	75	100	µA	VDD = 3.0V, CMOFF = 0, LSOFF = 0, REFOFF = 0
	IPD2	—	95	125	µA	VDD = 4.0V, CMOFF = 0, LSOFF = 0, REFOFF = 0
All analog off, WDT on (Note 5)	IPD3	—	7.5	20	µA	VDD = 3.0V
	IPD3	—	10.5	28	µA	VDD = 4.0V
All analog off, WDT off (Hibernate mode) (Note 5)	IPD4	—	0.9	12	µA	VDD = 3.0V
	IPD4	—	1.5	16	µA	VDD = 4.0V
Operating Supply Current (Note 2, 4)						
Internal oscillator mode	I_{DD}	—	2.2	TBD	mA	Fosc = 4 MHz, VDD = 5.5V
		—	1.1	TBD	mA	Fosc = 4 MHz, VDD = 3.0V
HS oscillator mode		—	2.4	TBD	mA	Fosc = 4 MHz, VDD = 5.5V
		—	1.2	TBD	mA	Fosc = 4 MHz, VDD = 3.0V
		—	10	TBD	mA	Fosc = 20 MHz, VDD = 5.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD.
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Measured with all inputs at rails, no DC loads. IPD1 measured with internal oscillator active.

4: IDD values of individual analog module cannot be tested independently but are characterized.

5: Worst-case IPD conditions with all configuration bits unprogrammed. Programming configuration bits may reduce IPD.

FIGURE 13-12: TYPICAL OPERATING SUPPLY CURRENT vs FREQ (EXT CLOCK, 25°C)

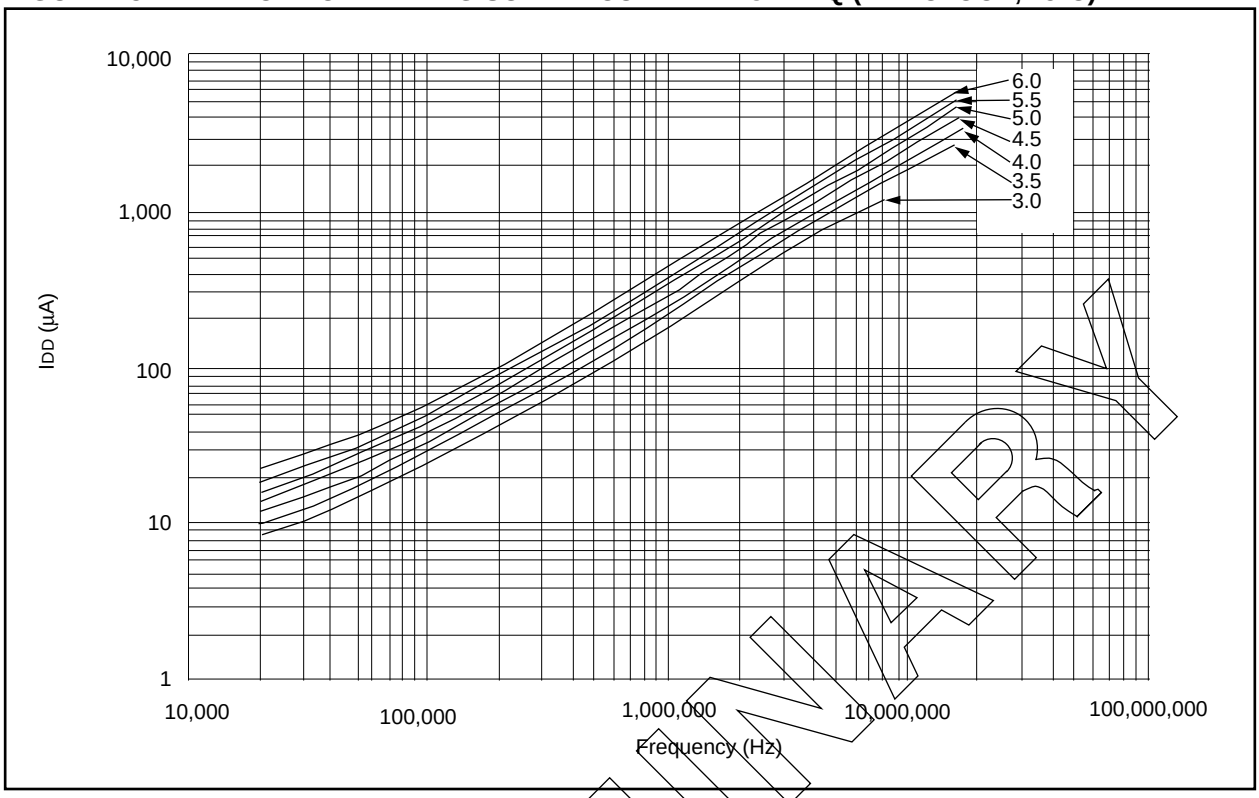


FIGURE 13-13: MAXIMUM OPERATING SUPPLY CURRENT vs FREQ (EXT CLOCK, -40° TO +85°C)

TO BE DETERMINED.

14.0 ANALOG SPECIFICATIONS: PIC14000-04 (COMMERCIAL, INDUSTRIAL)

Standard Operating Conditions (unless otherwise stated)

Operating Temperature: -40°C ≤ TA ≤ +85°C for industrial
0°C ≤ TA ≤ +70°C for commercial

VDD range: 2.7V (min) to 6.0V (max) unless otherwise stated.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions	Notes
Bandgap Voltage Reference							
Output Voltage	vo(vref)	1.14	1.19	1.24	V		
Turn-on Settling Time to < 0.1%	ton(vref)	—	1	10	ms	REFOFF bit in SLPCON register → 0	1
Temperature Coefficient	tc(vref)	—	±50	—	ppm/°C	Measured from 25°C to -40°C, +85°C	1
Temperature Coefficient	tc(vref)	—	±20	—	ppm/°C	Measured from 25°C to 0°C, +70°C	1
Supply Sensitivity	ss(vref)	—	0.04	—	%/V	From VDDmin to VDDmax	1
Operating Current (on)	idd(vref)	—	20	30	µA	REFOFF = 0	2
Operating Current (off)	idd(vref)	—	0	—	µA	REFOFF = 1	2
Programmable Current Source							
Output Current	io(cdac)					CDAC pin = 0V	3
		18.75	33.75	48.75	µA	ADCON1<7:4> = 1111b (full-scale)	
		1.25	2.25	3.25	µA	ADCON1<7:4> = 0001b (1 LSB)	
		-0.5	0	0.5	µA	ADCON1<7:4> = 0000b (zero-scale)	
Resolution	res(cdac)	1.25	2.25	3.25	µA	1 LSB	
Relative accuracy (linearity error)	racc(cdac)	-1/2		+1/2	lsb	CDAC = 0V	
Turn-on Settling Time to < 0.1% (reference start-up)	ton(cdac)	—	1	10	ms	Bias generator (reference) turn-on time (REFOFF 1 → 0)	1
Turn-on Settling Time to < 0.1% (reference already on and stable)	ton(cdac)	—	1	10	µs	REFOFF = 0 (constant), ADCON1<7:4> 0000b → 1111b	1
Temperature Coefficient	tc(cdac)	—	±0.1	—	%/°C	Measured from 25°C to Tmin, Tmax	1
Supply Sensitivity	ss(cdac)	—	0.2	—	%/V	From VDDmin to VDDmax	1
Output Voltage Sensitivity	vs(cdac)	-0.1	-0.01	–	%/V	CDAC pin voltage = 0V to VDD - 1.4V	
Output Voltage Range	vo(cdac)	0	—	VDD-1.4	V		
Operating Current (A/D on)	idd(cdac)	—	50	70	µA	ADCON1<7:4> = 1111b	2
Operating Current (A/D off)	idd(cdac)	—	0	—	µA	REFOFF = 1, ADOFF = 1	2
Temperature Sensor							
Output Voltage	vo(temp)	0.92	1.05	1.18	V	TA = 25°C	
Supply Sensitivity	ss(temp)	—	0.2	—	%/V	From VDDmin to VDDmax	1
Temperature Coefficient	KTC	3.2	3.65	4.1	mV/°C	Measured from 25°C to Tmax. Includes ± 2°C temperature calibration tolerance	

FIGURE 14-3: TEMPERATURE SENSOR OUTPUT VOLTAGE vs. TEMPERATURE (TYPICAL DEVICES SHOWN)

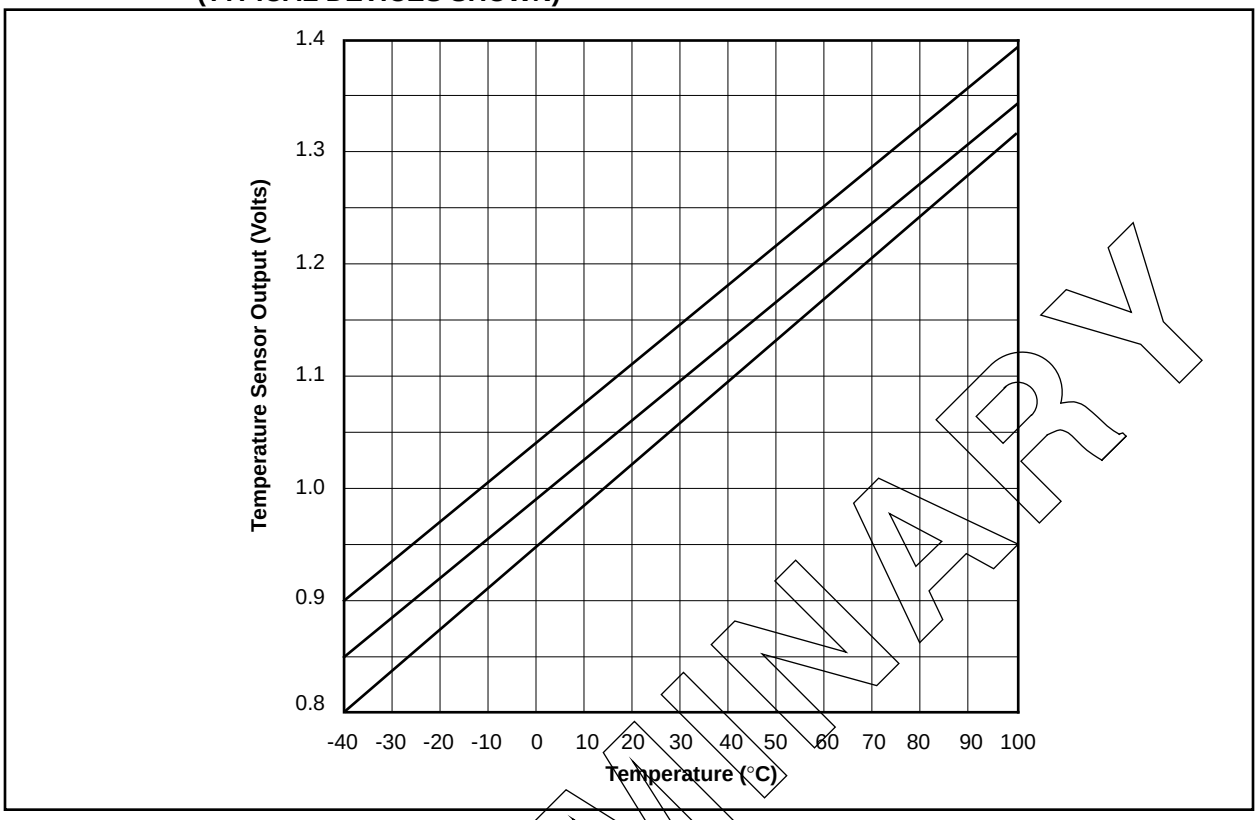
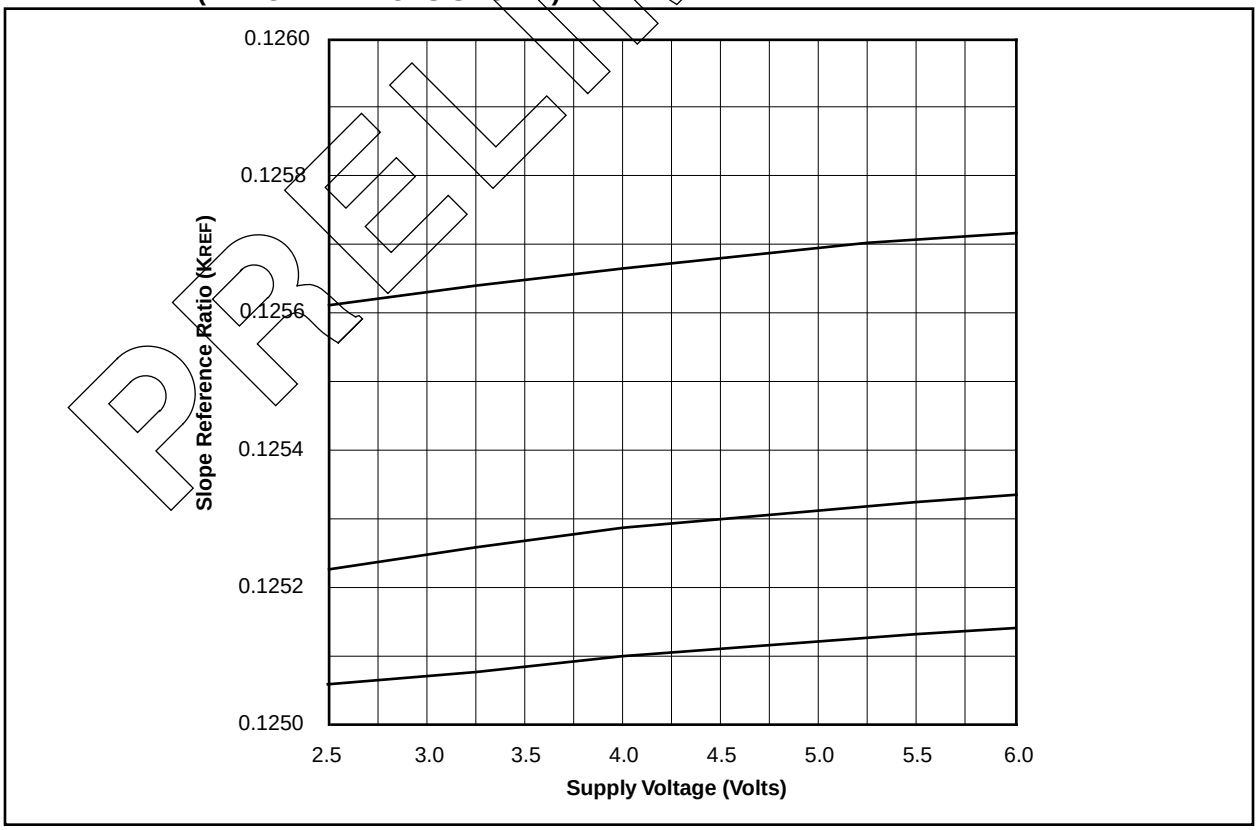


FIGURE 14-4: SLOPE REFERENCE RATIO (K_{REF}) vs. SUPPLY VOLTAGE (TYPICAL DEVICES SHOWN)



NOTES:

NOTES: