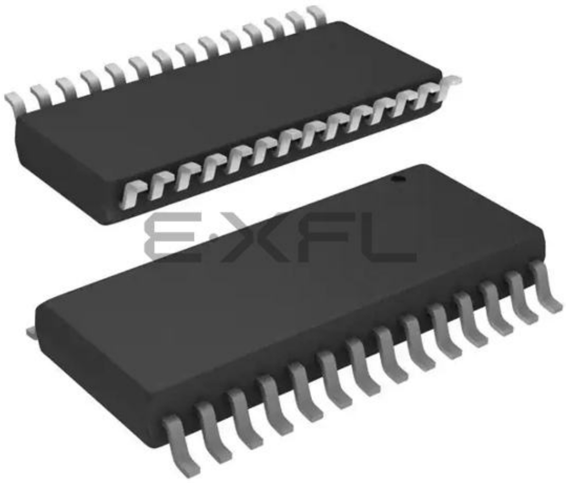

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C
Peripherals	POR, Temp Sensor, WDT
Number of I/O	20
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	Slope A/D
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic14000-04i-so

1.0 GENERAL DESCRIPTION

The PIC14000 features include medium to high resolution A/D conversion (10 to 16 bits), temperature sensing, closed loop charge control, serial communication, and low power operation.

The PIC14000 uses a RISC Harvard architecture CPU with separate 14-bit instruction and 8-bit data buses. A two-stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches, which require two cycles. A total of 35 instructions are available. Additionally, a large register set is included.

PIC16/17 microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers.

Features:

The PIC14000 is a 28-pin device with these features:

- 4K of EPROM
- 192 bytes of RAM
- 22 I/O pins

The analog peripherals include:

- 8 external analog input channels, two with level shift inputs
- 6 internal analog input channels
- 2 comparators with programmable references
- A bandgap reference
- An internal temperature sensor
- A programmable current source

In addition, the I^2C serial port through a multiplexer supports two separate I^2C channels.

A special oscillator option allows either an internal 4 MHz oscillator or an external crystal oscillator. Using the internal 4 MHz oscillator requires no external components.

The PIC14000 contains three timers, the Watchdog Timer (WDT), Timer0 (TMR0), and A/D Timer (ADTMR). The Watchdog Timer includes its own on-chip RC oscillator providing protection against software lock-up. TMR0 is a general purpose 8-bit timer/counter with an 8-bit prescaler. It may be clocked externally using the RC3/T0CKI pin. The ADTMR is intended for use with the slope A/D converter, but can also be used as a general purpose timer. It has an associated capture register which can be used to measure the time between events.

An internal low-voltage detect circuit allows for tracking of voltage levels. Upon detecting the low voltage condition, the PIC14000 can be instructed to save its operating state then enter an idle state.

The internal band-gap reference is used for calibrating the measurements of the analog peripherals. The calibration factors are stored in EPROM and can be used to achieve high measurement accuracy.

Power savings modes are available for portable applications. The SLEEP and HIBERNATE modes offer different levels of power savings. The PIC14000 can wake up from these modes through interrupts or reset.

A UV erasable CERDIP packaged version is ideal for code development, while the cost-effective One-Time Programmable (OTP) version is suitable for production in any volume.

The PIC14000 fits perfectly in applications for battery charging, capacity monitoring, and data logging. The EPROM technology makes customization of application programs (battery characteristics, feature sets, etc.) extremely fast and convenient. The small footprint packages make this microcontroller based mixed signal device perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC14000 very versatile in other applications such as temperature monitors/controllers.

1.1 Family and Upward Compatibility

Code written for PIC16C6X/7X can be easily ported to the PIC14000 (see Appendix A).

1.2 Development Support

The PIC14000 is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A “C” compiler and fuzzy logic support tools are also available.

4.2.2.2 OPTION REGISTER

The OPTION register (Address 81h) is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, TMR0, and the weak pull-ups on PORTC<5:0>. Bit 6 is reserved.

Note:	To achieve a 1:1 prescaler assignment, assign the prescaler to the WDT (PSA=1)

FIGURE 4-4: OPTION REGISTER

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
$\overline{\text{RCPU}}$	r	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

Register:	OPTION	W:	Writable
Address:	81h	R:	Readable
POR value:	FFh	U:	Unimplemented. Read as '0'

PS2:PS0

PRESCALER VALUE			TMR0 RATE	WDT RATE
PS2	**PS1**	**PS0**		
0	0	0	1 : 2	1 : 1
0	0	1	1 : 4	1 : 2
0	1	0	1 : 8	1 : 4
0	1	1	1 : 16	1 : 8
1	0	0	1 : 32	1 : 16
1	0	1	1 : 64	1 : 32
1	1	0	1 : 128	1 : 64
1	1	1	1 : 256	1 : 128

PSA: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to TMR0

T0SE: TMR0 source edge
1 = Increment on high-to-low transition on RC3/T0CKI pin
0 = Increment on low-to-high transition on RC3/T0CKI pin

T0CS: TMR0 clock source
1 = Transition on RC3/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

Reserved. This bit should be programmed as a '1'. Use of this bit as general purpose read/write is not recommended since this may affect upward compatibility with future products.

$\overline{\text{RCPU}}$: PORTC pull-up enable
1 = PORTC pull-ups are disabled overriding any port latch value (RC<5:0> only)
0 = PORTC pull-ups are enabled by individual port-latch values (RC<5:0>)

4.2.2.4 PIE1 REGISTER

This register contains the individual enable bits for the Peripheral interrupts including A/D capture event, I²C serial port, PORTC change and A/D capture timer overflow, and external push button.

Note:	INTCON<6> must be enabled to enable any interrupt in PIE1.

FIGURE 4-6: PIE1 REGISTER

R/W	R	R	R/W	R/W	R/W	R/W	R/W
CMIE	—	—	PBIE	I²CIE	RCIE	ADCIE	OVFIE
bit7							bit0

Register:	PIE1	W:	Writable
Address:	8Ch	R:	Readable
POR value:	00h	U:	Unimplemented, read as '0'

OVFIE: A/D Counter Overflow Interrupt Enable
1 = Enables A/D counter overflow interrupt
0 = Disables A/D counter overflow interrupt

ADCIE: A/D Capture Interrupt Enable
1 = A/D capture interrupt is enabled
0 = A/D capture interrupt is disabled

RCIE: PORTC Interrupt on change Enable
1 = Enables RCIF interrupt on pins, RC<7:4>
0 = Disables RCIF interrupt

I²CIE: I²C Port Interrupt Enable
1 = Enables I²CIF interrupt
0 = Disables I²CIF interrupt

PBIE: External Pushbutton Interrupt Enable
1 = Enable PBTN (pushbutton) interrupt on OSC1/PBTN.
(Note this interrupt not available in HS mode).
0 = Disable PBTN interrupt on OSC1/PBTN

Unimplemented. Read as '0'

Unimplemented. Read as '0'

CMIE: Programmable Reference Comparator Interrupt Enable
1 = Enable programmable reference comparator trip
0 = Disable programmable reference comparator trip

 Preliminary

4.2.2.5 PIR1 REGISTER

This register contains the individual flag bits for the Peripheral interrupts (Figure 4-7).

Note:	These bits will be set by the specified condition, even if the corresponding Interrupt Enable bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling an interrupt, the user may wish to clear the corresponding interrupt flag, to ensure that the program does not immediately branch to the Peripheral Interrupt service routine.

FIGURE 4-7: PIR1 REGISTER

R/W	R	R	R/W	R/W	R/W	R/W	R/W
CMIF	—	—	PBIF	I^2CIF	RCIF	ADCIF	OVFIF
bit7							bit0

Register: PIR1	W: Writable
Address: 0Ch	R: Readable
POR value: 00h	U: Unimplemented, read as '0'

OVFIF: A/D counter Overflow Interrupt Flag
1 = An A/D counter overflow has occurred. Must be cleared in software.
0 = An A/D counter overflow has not occurred

ADCIF: A/D Capture Interrupt Flag
1 = An A/D capture has occurred. Must be cleared in software.
0 = An A/D capture has not occurred

RCIF: PORTC Interrupt on Change Flag
1 = At least one RC<7:4> input changed. Must be cleared in software.
0 = None of the RC<7:4> inputs have changed

I^2CIF: I^2C Port Interrupt Flag
1 = A transmission/reception is completed. Must be cleared in software.
0 = Waiting to transmit/receive

PBIF: External Pushbutton Interrupt Flag
1 = The external pushbutton interrupt has occurred on OSC1/PBTN. Note: This interrupt is not available in HS mode.
0 = The external pushbutton interrupt did not occur

Unimplemented. Read as '0'

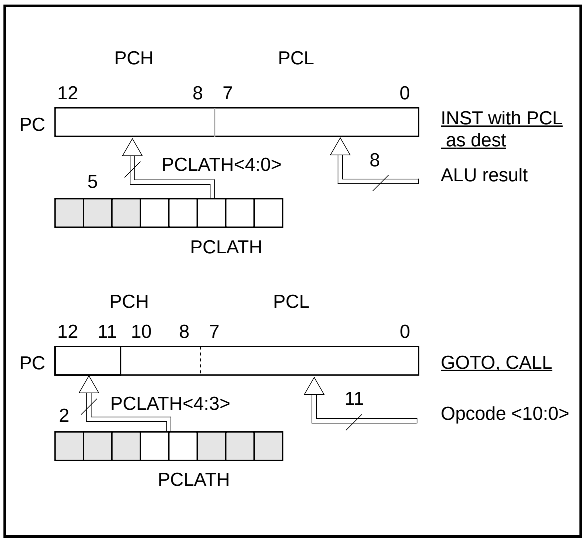
Unimplemented. Read as '0'

CMIF: Programmable Reference Comparator Interrupt Flag
1 = The comparator output has tripped. This is a level-sensitive interrupt.
0 = The interrupt did not occur

4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte, PCL, is a readable and writable register. The high byte of the PC (PCH) is not directly readable or writable. PCLATH is a holding register for PC<12:8> where contents are transferred to the upper byte of the program counter. When PC is loaded with a new value during a CALL, GOTO or a write to PCL, the high bits of PC are loaded from PCLATH as shown in Figure 4-9.

FIGURE 4-9: LOADING OF PC IN DIFFERENT SITUATIONS



Note:	On POR, the contents of the PCLATH register are unknown. The PCLATH should be initialized before a CALL, GOTO, or any instruction that modifies the PCL register is executed.

4.3.1 COMPUTED GOTO

When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note “Table Read Using the PIC16CXX”(AN556).

4.3.2 STACK

The PIC14000 has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed in the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a “PUSH” or a “POP” operation.

The stack operates as a circular buffer. This means that after the stack has been “PUSHed” eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1:	There are no STATUS bits to indicate stack overflow or stack underflow conditions.
Note 2:	There are no instruction mnemonics called PUSH nor POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, or RETFIE instructions, or the vectoring to an interrupt address

4.3.3 PROGRAM MEMORY PAGING

The PIC14000 has 4K of program memory, but the CALL and GOTO instructions only have a 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 4K program memory address range, there must be another bit to specify the program memory page. This paging bit comes from the PCLATH<3> bit (Figure 4-9). When doing a CALL or GOTO instruction, the user must ensure that this page bit (PCLATH<3>) is programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<3> is not required for the return instructions (which pops the PC from the stack).

Note:	The PIC14000 ignores the PCLATH<4> bit, which is used for program memory pages 2 and 3 (1000h-1FFFh). The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

Example 4-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that the PCLATH is saved and restored by the interrupt service routine (if interrupts are used).

EXAMPLE 4-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
ORG 0X500
BSF     PCLATH,  3 ; Select page 1 (800h-FFFh)
CALL    SUB1_P1    ; Call subroutine in
        :          ; page 1 (800h-FFFh)
        :
        :
ORG 0X900
SUB1 P1 :          ; called subroutine
        :          ; page 1 (800h-FFFh)
        :
RETURN             ; return to page 0
                   ; (000h-7FFh)
```

FIGURE 7-2: I^2CSTAT: I^2C PORT STATUS REGISTER

U	U	R	R	R	R	R	R
–	–	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit7							bit0

Register: I^2CSTAT Address: 94h POR value: 00h	W: Writable bit R: Readable bit U: Unimplemented, read as ‘0’

BF: Buffer full

Receive
1 = Receive complete, I^2CBUF is full
0 = Receive not complete, I^2CBUF is empty

Transmit
1 = Transmit in progress, I^2CBUF is full
0 = Transmit complete, I^2CBUF is empty

UA: Update Address (10-bit I^2C slave mode only)
1 = Indicate that the user needs to update the address in the I^2CADD register.
0 = Address does not need to be updated

R/$\overline{W}$: Read/write bit information
This bit holds the R/$\overline{W}$ bit information received following the last address match. This bit is only valid during the transmission.
The user may use this bit in software to determine whether transmission or reception is in progress.
1 = Read
0 = Write

S: Start bit
This bit is cleared when the I^2C module is disabled (I^2CEN is cleared)
1 = Indicates that a start bit has been detected last. This bit is 0 on reset.
0 = Start bit was not detected last

P: Stop bit
This bit is cleared when the I^2C module is disabled (I^2CEN is cleared)
1 = Indicates that a stop bit has been detected last.
0 = Stop bit was not detected last

D/$\overline{A}$: Data/$\overline{\text{Address}}$ bit
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was address

Unimplemented: read as ‘0’

 Preliminary

FIGURE 7-3: I^2CCON: I^2C PORT CONTROL REGISTER

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
WCOL	I^2COV	I^2CEN	CKP	I^2CM3	I^2CM2	I^2CM1	I^2CM0
bit7							bit0

Register: I^2CCON Address: 14h POR value: 00h	W: Writable bit R: Readable bit U: Unimplemented, read as ‘0’

I^2CM<3:0>: I^2C mode select

0110 = I^2C slave mode, 7-bit address
0111 = I^2C slave mode, 10-bit address
1011 = I^2C firmware controlled master mode (slave idle)
1110 = I^2C slave mode, 7-bit address with start and stop bit interrupts enabled
1111 = I^2C slave mode, 10-bit address with start and stop bit interrupts enabled

Any other combinations of I^2CM<3:0> are illegal and should NEVER be used.

CKP: Clock polarity select

SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch)
Note: Used to ensure data setup time

I^2CEN: I^2C enable

1 = Enables the serial port and configures SDA and SCL pins as serial port pins. When enabled, these pins must be configured as input or output.
0 = Disables serial port and configures these pins as I/O port pins

I^2COV: Receive overflow flag

1 = A byte is received while the I^2CBUF is still holding the previous byte. I^2COV is a don't care in transmit mode. I^2COV must be cleared in software.
0 = No overflow

WCOL: Write collision detect

1 = the I^2CBUF register is written while it is still transmitting the previous word. Must be cleared in software.
0 = No collision

7.5.1.3 TRANSMISSION

When the R/$\overline{W}$ bit of the address byte is set and an address match occurs, the R/$\overline{W}$ bit of the I^{2}CSTAT register is set. The received address is loaded into the I^{2}CBUF The $\overline{ACK}$ pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the I^{2}CBUF register, which also loads the I^{2}CSR register. Then the SCL pin should be enabled by setting the CKP bit (I^{2}CCON<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 7-15).

A I^{2}CIF interrupt is generated for each data transfer byte. The I^{2}CIF bit must be cleared in software, and the I^{2}CSTAT register is used to determine the status of the byte. The I^{2}CIF bit is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. The slave then monitors for another occurrence of the START bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the I^{2}CBUF register, which also loads the I^{2}CSR register. Then the SCL pin should be enabled by setting the CKP bit (I^{2}CCON<4>).

FIGURE 7-15: I^{2}C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)

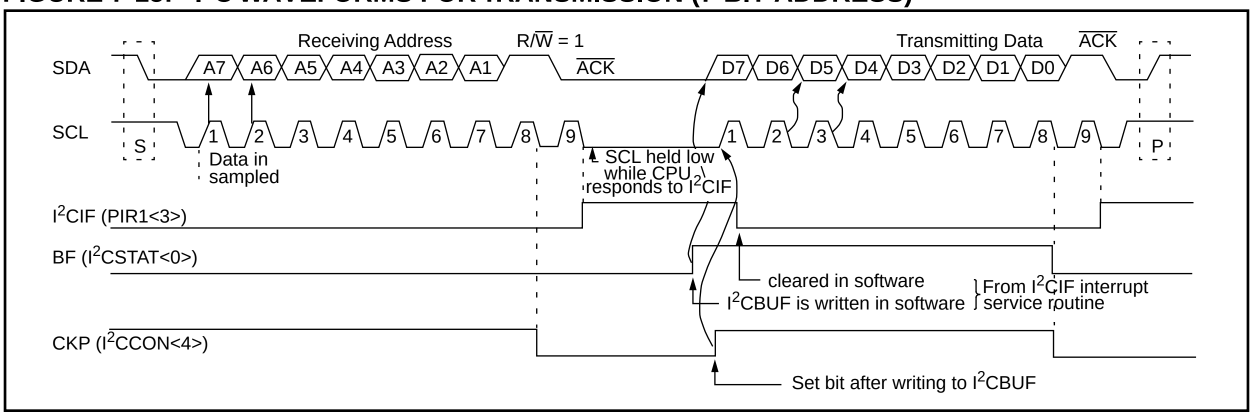


FIGURE 8-2: EXAMPLE A/D CONVERSION CYCLE

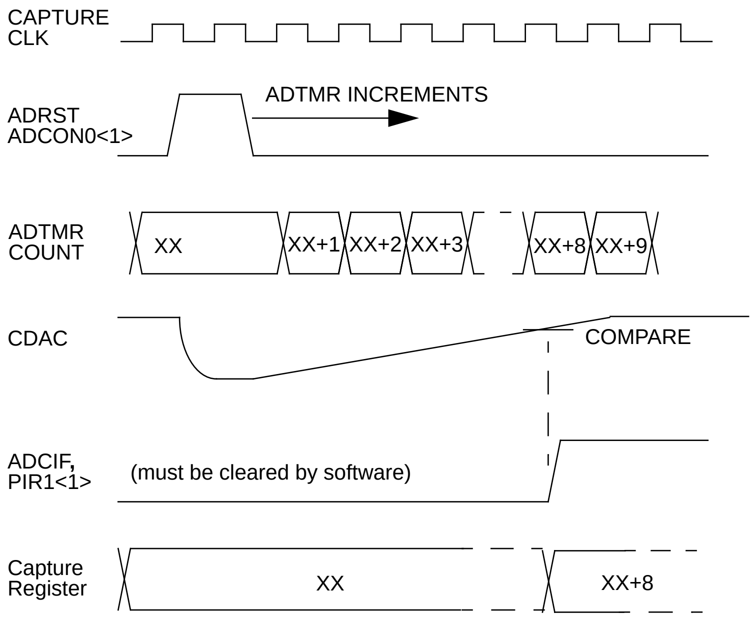


FIGURE 8-3: A/D CAPTURE TIMER (LOW BYTE)

0Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTMRL	b7	b6	b5	b4	b3	b2	b1	b0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

FIGURE 8-4: A/D CAPTURE TIMER (HIGH BYTE)

0Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTMRH	b15	b14	b13	b12	b11	b10	b9	b8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

FIGURE 8-5: A/D CAPTURE REGISTER (LOW BYTE)

15h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCAPL	b7	b6	b5	b4	b3	b2	b1	b0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

FIGURE 8-6: A/D CAPTURE REGISTER (HIGH BYTE)

16h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCAPH	b15	b14	b13	b12	b11	b10	b9	b8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Legend: U= unimplemented, X = unknown.

8.4 A/D Comparator

The PIC14000 includes a high gain comparator for A/D conversions. The positive input terminal of the A/D comparator is connected to the output of an analog mux through an RC low-pass filter. The nominal time-constant for the RC filter is 3.5 μs. The negative input terminal is connected to the external 0.1 μF (nominal) ramp capacitor.

8.5 Analog Mux

A total of 16 channels are internally multiplexed to the single A/D comparator positive input. Four configuration bits (ADCON0<7:4>) select the channel to be converted. Refer to Table 8-1 for channel assignments.

TABLE 8-1: A/D CHANNEL ASSIGNMENT

ADCON0(7:4)				A/D Channel
0	0	0	0	RA0/AN0 pin
0	0	0	1	RA1/AN1 pin
0	0	1	0	RA2/AN2 pin
0	0	1	1	RA3/AN3 pin
0	1	0	0	Bandgap reference voltage
0	1	0	1	Slope reference SREFHI
0	1	1	0	Slope reference SREFLO
0	1	1	1	Internal temperature sensor
1	0	0	0	Programmable reference A output
1	0	0	1	Programmable reference B output
1	0	1	0	RD4/AN4 pin
1	0	1	1	RD5/AN5 pin
1	1	0	0	RD6/AN6 pin
1	1	0	1	RD7/AN7 pin
1	1	1	0	Reserved
1	1	1	1	Reserved

TABLE 8-4: A/D CONTROL AND STATUS REGISTER 1

9Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCON1	ADDAC3	ADDAC2	ADDAC1	ADDAC0	PCFG3	PCFG2	PCFG1	PCFG0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B4	ADDAC3 ADDAC2 ADDAC1 ADDAC0	A/D Current Source Selects. Refer to Table 8-2.
B3-B2	PCFG3 PCFG2	PORTD Configuration Selects (See Table 8-5)
B1-B0	PCFG1 PCFG0	PORTA Configuration Selects (See Table 8-5)

TABLE 8-5: PORTA AND PORTD CONFIGURATION

ADCON1<1:0>	RA0/AN0	RA1/AN1	RA2/AN2	RA3/AN3
ADCON1<3:2>	**RD4/AN4**	**RD5/AN5**	**RD6/AN6**	**RD7/AN7**
0 0	A	A	A	A
0 1	A	A	A	D
1 0	A	A	D	D
1 1	D	D	D	D

Legend: A = Analog input, D = Digital I/O

FIGURE 9-6: PREFA REGISTER

9Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREFA	PRA7	PRA6	PRA5	PRA4	PRA3	PRA2	PRA1	PRA0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B0	PRA7 PRA6 PRA5 PRA4 PRA3 PRA2 PRA1 PRA0	Programmable Reference A Voltage Select Bits. See Table 9-1 and Table 9-2 for decoding.

FIGURE 9-7: PREFB REGISTER

9Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREFB	PRB7	PRB6	PRB5	PRB4	PRB3	PRB2	PRB1	PRB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B0	PRB7 PRB6 PRB5 PRB4 PRB3 PRB2 PRB1 PRB0	Programmable Reference B Voltage Select Bits. See Table 9-1 and Table 9-2 for decoding.

10.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, V_{DD} and process variations (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION registers. Thus, time-out periods up to 2.3 seconds can be realized. The `CLRWDT` and `SLEEP` instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{\text{TO}}$ bit in the status register will be cleared upon a watchdog timer time-out. The WDT time-out period (no prescaler) is measured and stored in calibration space at location 0FD2h.

10.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst-case conditions (minimum VDD, maximum temperature, maximum WDT prescaler) it may take several seconds before a WDT time-out occurs. Refer to Section 6.3 for prescaler switching considerations.

10.8 Power Management Options

The PIC14000 has several power management options to prolong battery lifetime. The `SLEEP` instruction halts the CPU and can turn off the on-chip oscillators. The CPU can be in SLEEP mode, yet the A/D converter can continue to run. Several bits are included in the SLPCON register (8Fh) to control power to analog modules.

TABLE 10-6: SUMMARY OF POWER MANAGEMENT OPTIONS

Function	Summary
CPU Clock	OFF during SLEEP/HIBERNATE mode, ON otherwise
Main Oscillator	ON if NOT in SLEEP mode. In SLEEP mode, controlled by OSCOFF bit, SLPCON<3>.
Watchdog Timer	Controlled by WDTE, 2007h<2> and HIBEN, SLPCON<7>
Temperature Sensor	Controlled by TEMPOFF, SLPCON<1>
Low-voltage Detector	Controlled by REFOFF, SLPCON<5>
Comparator and Programmable References	Controlled by CMOFF, SLPCON<2>
A/D Comparator	Controlled by ADOFF, SLPCON<0>
Programmable Current Source	Controlled by ADOFF, SLPCON<0> and ADCON1<7:4>
Slope Reference Voltage Divider	Controlled by ADOFF, SLPCON<0>
Level Shift Networks	Controlled by LSOFF, SLPCON<4>
Bandgap Reference	Controlled by REFOFF, SLPCON<5>
Voltage Regulator Control	Always ON. Does not consume power if unconnected.
Power On Reset	Always ON, except in SLEEP/HIBERNATE mode

Note: Refer to analog specs for individual peripheral operating currents.

CLRWDT — Clear Watchdog Timer

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT
0 → WDT prescaler,
1 → $\overline{\text{TO}}$
1 → $\overline{\text{PD}}$

Status Affected: $\overline{\text{TO}}$, $\overline{\text{PD}}$

Encoding:

00	0000	0110	0100

Description: `CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{\text{TO}}$ and $\overline{\text{PD}}$ are set.

Words: 1

Cycles: 1

Example

```
CLRWDT
```

Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescaler = 0
$\overline{\text{TO}}$ = 1
$\overline{\text{PD}}$ = 1

COMF — Complement f

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow$ (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example

```
COMF        REG1,0
```

Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

DECF — Decrement f

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - 1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example

```
DECF     CNT,  1
```

Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

DECFSZ — Decrement f, Skip if 0

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - 1 → (dest); skip if result = 0

Status Affected: None

Encoding:

00	1011	dfff	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example

```
HERE       DECFSZ   CNT, 1
           GOTO     LOOP
CONTINUE   •
           •
           •
```

Before Instruction
PC = address `HERE`
After Instruction
CNT = CNT - 1
if CNT = 0,
PC = address `CONTINUE`
if CNT ≠ 0,
PC = address `HERE+1`

SWAPF — Swap Nibbles in f

Syntax: [*label*] SWAPF f,d

Operands: $0 \leq f \leq 127$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>),
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

00	1110	dfff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example

```
SWAPF  REG,    0
```

Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0x5A

TRIS — Load TRIS Register

Syntax: [*label*] TRIS f

Operands: $5 \leq f \leq 7$

Operation: (W) → TRIS register f;

Status Affected: None

Encoding:

00	0000	0110	0fff

Description: The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.

Words: 1

Cycles: 1

Example

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

XORLW — Exclusive OR Literal with W

Syntax: [*label*] XORLW k

Operands: $0 \leq k \leq 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

11	1010	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:

```
XORLW    0xAF
```

Before Instruction
W = 0xB5

After Instruction
W = 0x1A

XORWF — Exclusive OR W with f

Syntax: [*label*] XORWF f,d

Operands: $0 \leq f \leq 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

00	0110	dfff	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example

```
XORWF     REG   1
```

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

13.0 ELECTRICAL CHARACTERISTICS FOR PIC14000 ABSOLUTE MAXIMUM RATINGS †

Ambient temperature under bias .... -55°C to+ 125°C
Storage Temperature .... -65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) .... -0.5V to V_{DD} +0.6V
Voltage on V_{DD} with respect to V_{SS} .... 0 to +6.0 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2) .... 0 to +14 V
Total power Dissipation (Note 1) .... 1.0 W
Maximum Current out of V_{SS} pin 300mA
Maximum Current into V_{DD} pin 250mA
Input clamp current, I_{IK} (V_I <0 or V_I> V_{DD}) .... ±20mA
Output clamp current, I_{OK} (V_O <0 or V_O>V_{DD}) .... ±20mA
Maximum Output Current sunk by any I/O pin 25mA
Maximum Output Current sourced by any I/O pin 25mA
Maximum Current sunk by PORTA, PORTC, and PORTD(combined) 200mA
Maximum Current sourced by PORTA, PORTC, and PORTE (combined) 200mA
Maximum Current sunk by PORTC and PORTD (combined) 200mA
Maximum Current sourced by PORTC and PORTD (combined) 200mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.2 DC Characteristics: PIC14000

DC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ + 85°C for industrial and 0°C ≤ T_A ≤ +70°C for commercial Operating voltage V_{DD} range as described in Section 13.1.					
Characteristic	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
Input Low Voltage						
I/O ports	V_{IL}					
Schmitt Trigger mode		V_{SS}	—	$0.2V_{DD}$	V	
SMBus mode (RC7, RC6, RD0, RD1)		V_{SS}	—	0.6	V	SMBus bit, MISC<3> = 1
$\overline{MCLR}$, OSC1 (in IN mode)		Vss	—	$0.2V_{DD}$	V	
OSC1 (in HS mode)		Vss	—	$0.3V_{DD}$	V	
Input High Voltage						
I/O ports	V_{IH}		—			
Schmitt Trigger mode		0.85 V_{DD}	—	V_{DD}	V	
SMBus mode (RC7, RC6, RD0, RD1)		1.4V	—	V_{DD}	V	SMBus bit, MISC<3> = 1
PORTC<5:0> weak pull-up current	I_{PURC}	50	200	†400	μA	V_{DD} = 5V, V_{PIN} = V_{SS}
Input Leakage Current (Notes 1,2)						
I/O ports, CDAC	I_{IL}			±1	μA	Vss ≤ V_{PIN} ≤ V_{DD}, Pin at hi-impedance
$\overline{MCLR}$				±5	μA	Vss ≤ V_{PIN} ≤ V_{DD}
OSC1				±5	μA	Vss ≤ V_{PIN} ≤ V_{DD}
Output Low Voltage						
I/O ports	V_{OL}	—	—	0.6	V	I_{OL} = 8.5mA, V_{DD}-4.5V, -40°C to +85°C
OSC2		—	—	0.6	V	I_{OL} = 1.6mA, V_{DD}-4.5V, -40°C to +85°C
Output High Voltage						
I/O ports (Note 2)	V_{OH}	V_{DD}-0.7	—	—	V	I_{OH} = -3.0mA, V_{DD}=4.5V, -40°C to +85°C
RC6, RC7, RD0, RD1 (except I^2C mode)		2.4	—	—	V	I_{OH} = -2.0mA, V_{DD}=4.5V, -40°C to +85°C
OSC2		V_{DD}-0.7	—	—	V	I_{OH} = -1.3mA, V_{DD}=4.5V, -40°C to +85°C
Capacitive Loading Specs on Output Pins						
OSC2 pin	C_{OSC2}			15	pF	
All I/O pins except OSC2 (in IN mode)	C_{IO}			50	pF	
SCL, SDA in I^2C mode	Cb			400	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as coming out of the pin.

ON-LINE SUPPORT

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Use Microchip's Bulletin Board Service (BBS) to get current information and help about Microchip products. Microchip provides the BBS communication channel for you to use in extending your technical staff with microcontroller and memory experts.

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www.microchip.com

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You can telnet or ftp to the Microchip BBS at the address:

mchipbbs.microchip.com

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When using the BBS via the Compuserve Network, in most cases, a local call is your only expense. The Microchip BBS connection does not use CompuServe membership services, therefore you do not need CompuServe membership to join Microchip's BBS. There is no charge for connecting to the Microchip BBS.

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The following connect procedure applies in most locations.

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe access number.
3. Depress the <Enter> key and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type +, depress the <Enter> key and “Host Name:” will appear.
5. Type MCHIPBBS, depress the <Enter> key and you will be connected to the Microchip BBS.

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For voice information (or calling from overseas), you may call (614) 723-1550 for your local CompuServe number.

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Device: **PIC14000** Literature Number: **DS40122B**

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PIC14000 PRODUCT IDENTIFICATION SYSTEM

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NO. -XX X /XX XXX

Pattern:	3-Digit Pattern Code for QTP (blank otherwise)		
Package:	SP	=	300 mil PDIP
	SO	=	300 mil SOIC (Gull Wing, 300 mil body)
	SS	=	209 mil SSOP
	JW	=	Windowed CERDIP
Temperature Range:	-	=	0˚C to +70˚C
	I	=	-40˚C to +85˚C
Frequency Range:	04	=	4 MHz
	20	=	20 MHz
Device:	PIC14000: V_{DD} range 2.7V to 6.0V		
	PIC14000T: V_{DD} range 2.7V to 6.0V (Tape & Reel)		