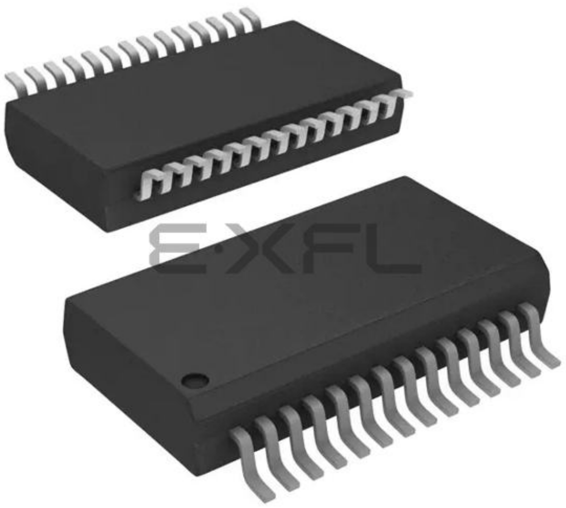

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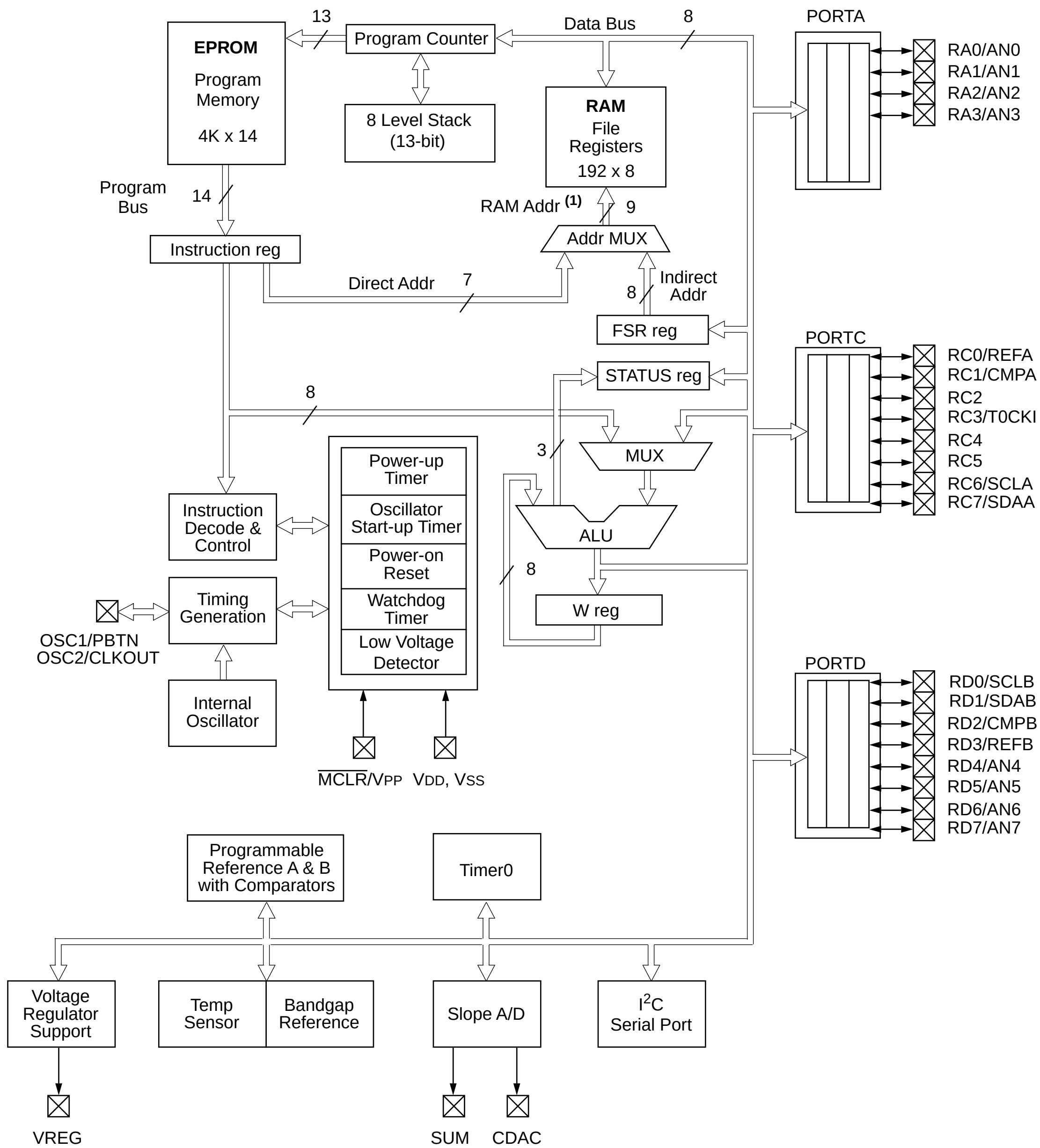
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C
Peripherals	POR, Temp Sensor, WDT
Number of I/O	20
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	Slope A/D
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic14000-04i-ss

FIGURE 3-1: PIC14000 BLOCK DIAGRAM



Note 1: Higher order bits are from the STATUS register.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Pin Name	Pin No.	I/O	Pin Type Input	Output	Description
RD3/REFB	3	I/O-PU	AN/ST	CMOS	General purpose I/O or programmable reference B output.
RD4/AN4	26	I/O	AN/ST	CMOS	Analog input channel 4. This pin can also serve as a GPIO.
RD5/AN5	25	I/O	AN/ST	CMOS	Analog input channel 5. This pin can connect to a level shift network. If enabled, a +0.5V offset is added to the input voltage. This pin can also serve as a GPIO.
RD6/AN6	24	I/O	AN/ST	CMOS	Analog input channel 6. This pin can also serve as a GPIO.
RD7/AN7	23	I/O	AN/ST	CMOS	Analog input channel 7. This pin can also serve as a GPIO.
VREG	10	O	—	AN	This pin is an output to control the gate of an external N-FET for voltage regulation.
OSC1/PBTN	8	I-PU	ST	—	IN Mode: Input with weak pull-up resistor, can be used to generate an interrupt. HS Mode: External oscillator input.
OSC2/ CLKOUT	7	O	—	CMOS	IN Mode: General purpose output. HS Mode: External oscillator/clock output.
$\overline{MCLR}$/VPP	14	I/PWR	ST		Master clear (reset) input / programming voltage input. This pin is an active low reset to the device.
V_{DD}	9	PWR			Positive supply connection
V_{SS}	20	GND			Return supply connection

Legend:

Type:	**Definition:**
TTL	TTL-compatible input
CMOS	CMOS-compatible input or output
ST	Schmitt Trigger input, with CMOS levels
SM	SMBus compatible input
OD	Open-drain output. An external pull-up resistor is required if this pin is used as an output.
NPU	N-channel pull-up. This pin will pull-up to approximately V_{DD} - 1.0V when outputting a logical ‘1’.
PU	Weak internal pull-up (10K-50K ohms)
No-P diode	No P-diode to V_{DD}. This pin may be pulled above the supply rail (to 6.0V maximum).
AN	Analog input or output

4.2.2.5 PIR1 REGISTER

This register contains the individual flag bits for the Peripheral interrupts (Figure 4-7).

Note:	These bits will be set by the specified condition, even if the corresponding Interrupt Enable bit is cleared (interrupt disabled) or the GIE bit is cleared (all interrupts disabled). Before enabling an interrupt, the user may wish to clear the corresponding interrupt flag, to ensure that the program does not immediately branch to the Peripheral Interrupt service routine.

FIGURE 4-7: PIR1 REGISTER

R/W	R	R	R/W	R/W	R/W	R/W	R/W
CMIF	—	—	PBIF	I^2CIF	RCIF	ADCIF	OVFIF
bit7							bit0

Register: PIR1	W: Writable
Address: 0Ch	R: Readable
POR value: 00h	U: Unimplemented, read as ‘0’

OVFIF: A/D counter Overflow Interrupt Flag
1 = An A/D counter overflow has occurred. Must be cleared in software.
0 = An A/D counter overflow has not occurred

ADCIF: A/D Capture Interrupt Flag
1 = An A/D capture has occurred. Must be cleared in software.
0 = An A/D capture has not occurred

RCIF: PORTC Interrupt on Change Flag
1 = At least one RC<7:4> input changed. Must be cleared in software.
0 = None of the RC<7:4> inputs have changed

I^2CIF: I^2C Port Interrupt Flag
1 = A transmission/reception is completed. Must be cleared in software.
0 = Waiting to transmit/receive

PBIF: External Pushbutton Interrupt Flag
1 = The external pushbutton interrupt has occurred on OSC1/PBTN. Note: This interrupt is not available in HS mode.
0 = The external pushbutton interrupt did not occur

Unimplemented. Read as ‘0’

Unimplemented. Read as ‘0’

CMIF: Programmable Reference Comparator Interrupt Flag
1 = The comparator output has tripped. This is a level-sensitive interrupt.
0 = The interrupt did not occur

4.2.2.6 PCON REGISTER

The Power Control (PCON) register status contains 2 flag bits to allow differentiation between a Power-on Reset, an external $\overline{\text{MCLR}}$ reset, WDT reset, or low-voltage condition (Figure 4-8).

These bits are cleared on POR. The user must set these bits following POR. On a subsequent reset if POR is cleared, this is an indication that the reset was due to a power-on reset condition.

Note: $\overline{\text{LVD}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{\text{LVD}}$ is cleared, indicating a low voltage condition has occurred.

FIGURE 4-8: PCON REGISTER

R/W	U	U	U	U	U	R/W	R/W
r	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{LVD}}$
bit7							bit0

Register: PCON Address: 8Eh POR value: 0000_000xb	W: Writable R: Readable U: Unimplemented, read as ‘0’

$\overline{\text{LVD}}$: Low Voltage Detect Flag
1 = A low-voltage detect condition has not occurred.
0 = A low-voltage detect condition has occurred. Software must set this bit after a power-on-reset condition has occurred.

$\overline{\text{POR}}$: Power on Reset Flag
1 = A power on reset condition has not occurred. Reset must be due to some other source (WDT, $\overline{\text{MCLR}}$).
0 = A power on reset condition has occurred. Software must set this bit after a power-on-reset condition has occurred.

Unimplemented. Read as ‘0’

Unimplemented. Read as ‘0’

Unimplemented. Read as ‘0’

Unimplemented. Read as ‘0’

Unimplemented. Read as ‘0’

Reserved. Bit 7 is reserved. This bit should be programmed as ‘0’ .

4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

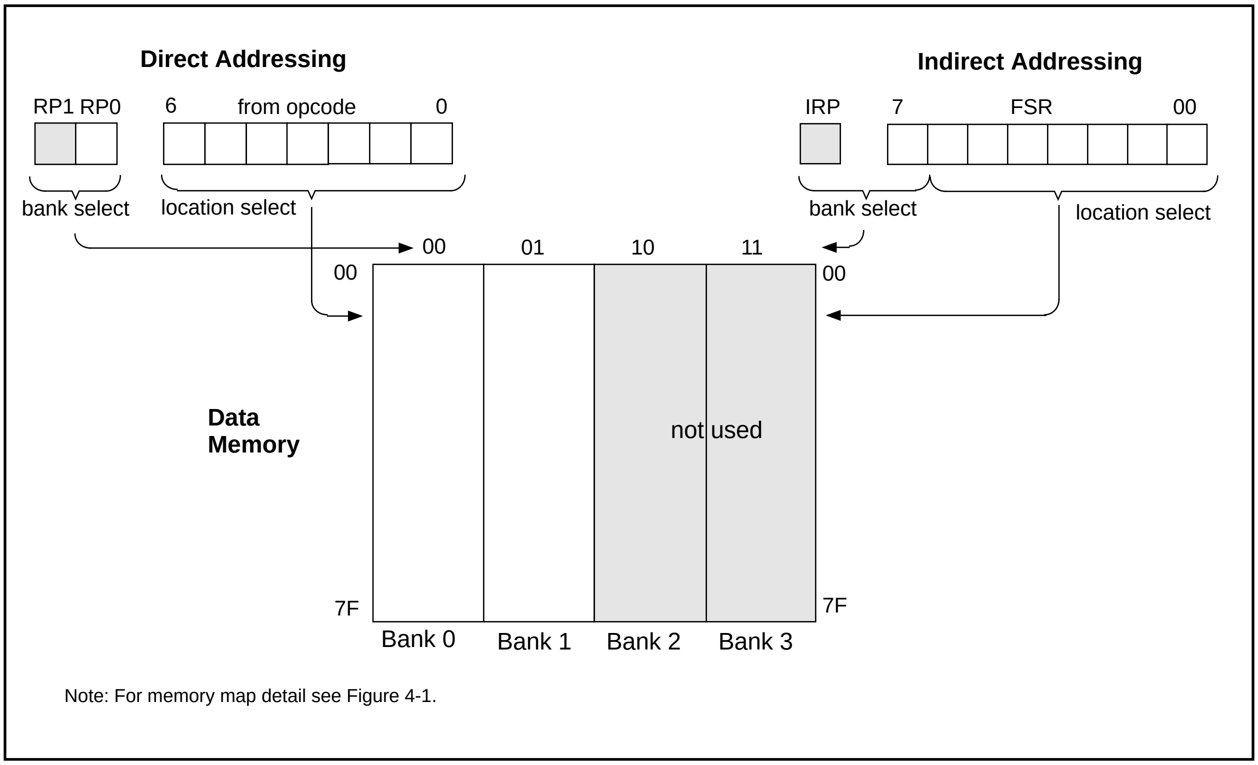
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the file select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-10. However, IRP is not used in the PIC14000.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: INDIRECT ADDRESSING

```
          movlw   0x20     ;initialize pointer
          movf    FSR      ;to RAM
NEXT      clrf    INDF     ;clear INDF register
          incf    FSR      ;inc pointer
          btfss   FSR,4    ;all done?
          goto    NEXT     ;no clear next
                           ;yes continue
CONTINUE:
```

FIGURE 4-10: INDIRECT/INDIRECT ADDRESSING

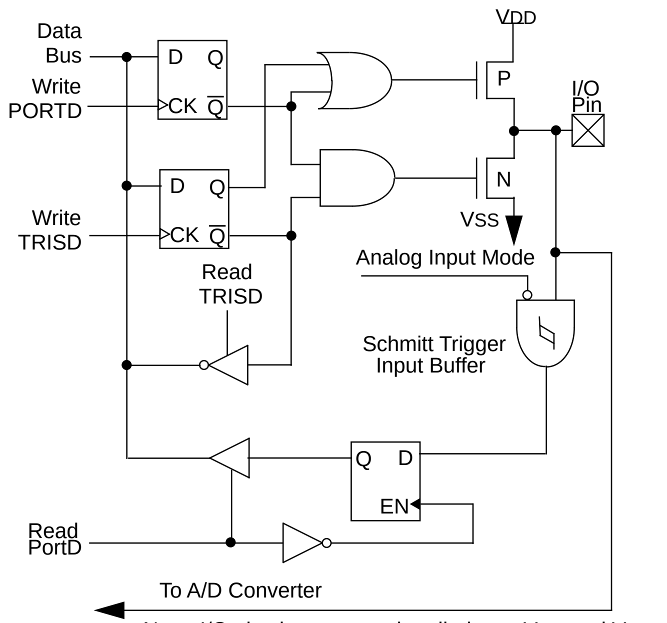


 Preliminary

5.3 PORTD and TRISD

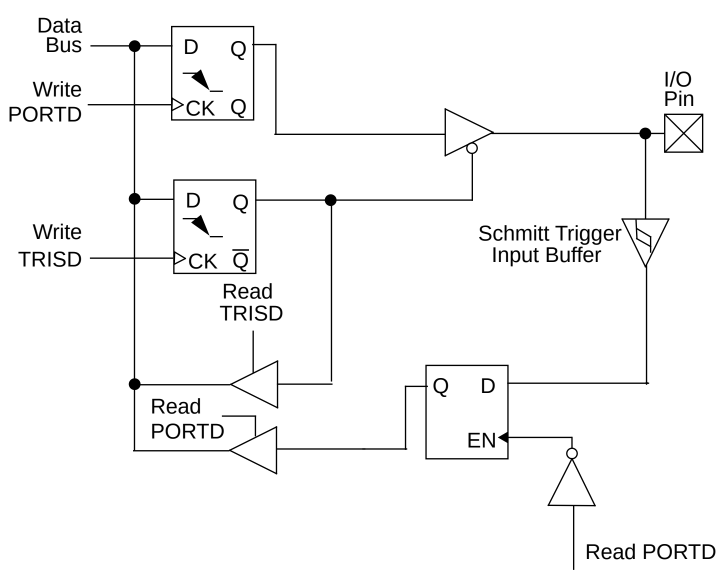
PORTD is an 8-bit port that may be used for general purpose I/O. Four pins can be configured as analog inputs.

FIGURE 5-8: BLOCK DIAGRAM OF PORTD<7:4> PINS



Note: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-9: BLOCK DIAGRAM OF PORTD<3:2> PINS



1. I/O pins have protection diodes to VDD and VSS.
2. If CMBOE (CMCON<5>) is set to '1', RD2 becomes CMPB, RD3 becomes REFB, ignoring the PORTD<3:2> data and TRISD<3:2> register settings.

7.5.2 MASTER MODE

Master mode operation is supported by interrupt generation on the detection of the START and STOP. The STOP(P) and START(S) bits are cleared from a reset or when the I^{2}C module is disabled. Control of the I^{2}C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are cleared.

In master mode, the SCL and SDA lines are manipulated by changing the corresponding TRISC<7:6> or TRISD<1:0> bits to an output (cleared). The output level is always low, regardless of the value(s) in PORTC<7:6> or PORTD<1:0>. So when transmitting data, a “1” data bit must have the TRISC<7> or TRISD<1> bit set (input) and a “0” data bit must have the TRISC<7> or TRISD<1> bit cleared (output). The same scenario is true for the SCL line with the TRISC<6> or TRISD<0> bit.

The following events will cause the I^{2}C interrupt Flag (I^{2}CIF) to be set (I^{2}C interrupt if enabled):

- START
- STOP
- Data transfer byte transmitted/received

Master mode of operation can be done with either the slave mode idle (I^{2}CM3...I^{2}CM0 = 1011b) or with the slave active. When both master and slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

7.5.3 MULTI-MASTER MODE

In multi-master mode, the interrupt generation on the detection of the START and STOP allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the I^{2}C module is disabled. Control of the I^{2}C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are cleared. When the bus is busy, enabling the I^{2}C interrupt will generate the interrupt when the STOP occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and low level is present, the device needs to release the SDA and SCL lines (set TRISC<7:6>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, the device may being addressed. If addressed an $\overline{\text{ACK}}$ pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

TABLE 7-3: REGISTERS ASSOCIATED WITH I^{2}C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B/8Bh	INTCON	GIE	PEIE	T0IE	r	r	T0IF	r	r
0Ch	PIR1	CMIF	—	—	PBIF	I^{2}CIF	RCIF	ADCIF	OVFIF
8Ch	PIE1	CMIE	—	—	PBIE	I^{2}CIE	RCIE	ADCIE	OVFIE
13h	I^{2}CBUF	I^{2}C Serial Port Receive Buffer/Transmit Register							
93h	I^{2}CADD	I^{2}C mode Synchronous Serial Port (I^{2}C mode) Address Register							
14h	I^{2}CCON	WCOL	I^{2}CON	I^{2}CEN	CKP	I^{2}CM3	I^{2}CM2	I^{2}CM1	I^{2}CM0
94h	I^{2}CSTAT	—	—	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF
9Eh	MISC	SMHOG	SPGNDB	SPGNDA	I^{2}CSEL	SMBUS	INCLKEN	OSC2	OSC1
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
88h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0

Legend: — = Unimplemented location, read as ‘0’
r = reserved locations, default is POR value and **should not be overwritten with any value**

Note: Shaded boxes are not used by the I^{2}C module.

FIGURE 7-16: MISC REGISTER

9Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MISC	SMHOG	SPGNDB	SPGNDA	I^2CSEL	SMBUS	INCLKEN	OSC2	OSC1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
POR value 00h	0	0	0	0	0	0	0	X

Bit	Name	Function
B7	SMHOG	SMHOG enable 1 = Stretch I^2C CLK signal (hold low) when receive data buffer is full (refer to Section 7.5.4). For pausing I^2C transfers while preventing interruptions of A/D conversions. 0 = Disable I^2C CLK stretch.
B6	SPGNDB	Serial Port Ground Select 1 = PORTD<1:0> ground reference is the RD5/AN5 pin. 0 = PORTD<1:0> ground reference is Vss.
B5	SPGNDA	Serial Port Ground Select 1 = PORTC<7:6> ground reference is the RA1/AN1 pin. 0 = PORTC<7:6> ground reference is Vss.
B4	I^2CSEL	I^2C Port select Bit. 1 = PORTD<1:0> are used as the I^2C clock and data lines. 0 = PORTC<7:6> are used as the I^2C clock and data lines.
B3	SMBus	SMBus-Compatibility Select 1 = SMBus compatibility mode is enabled. PORTC<7:6> and PORTD<1:0> have SMBus-compatible input thresholds. 0 = SMBus-compatibility is disabled. PORTC<7:6> and PORTD<1:0> have Schmitt Trigger input thresholds.
B2	INCLKEN	Oscillator Output Select (available in IN mode only). 1 = Output IN oscillator signal divided by four on OSC2 pin. 0 = Disconnect IN oscillator signal from OSC2 pin.
B1	OSC2	OSC2 output port bit (available in IN mode only). Writes to this location affect the OSC2 pin in IN mode. Reads return the value of the output latch.
B0	OSC1	OSC1 input port bit (available in IN mode only). Reads from this location return the status of the OSC1 pin in IN mode. Writes have no effect.

Caution:	Reading or writing the ADTMR register during an A/D conversion cycle can produce unpredictable results and is not recommended.

Note:	The correct sequence for writing the ADTMR register is HI byte followed by LO byte. Reversing this order will prevent the A/D timer from running.

During conversion one or both of the following events will occur:

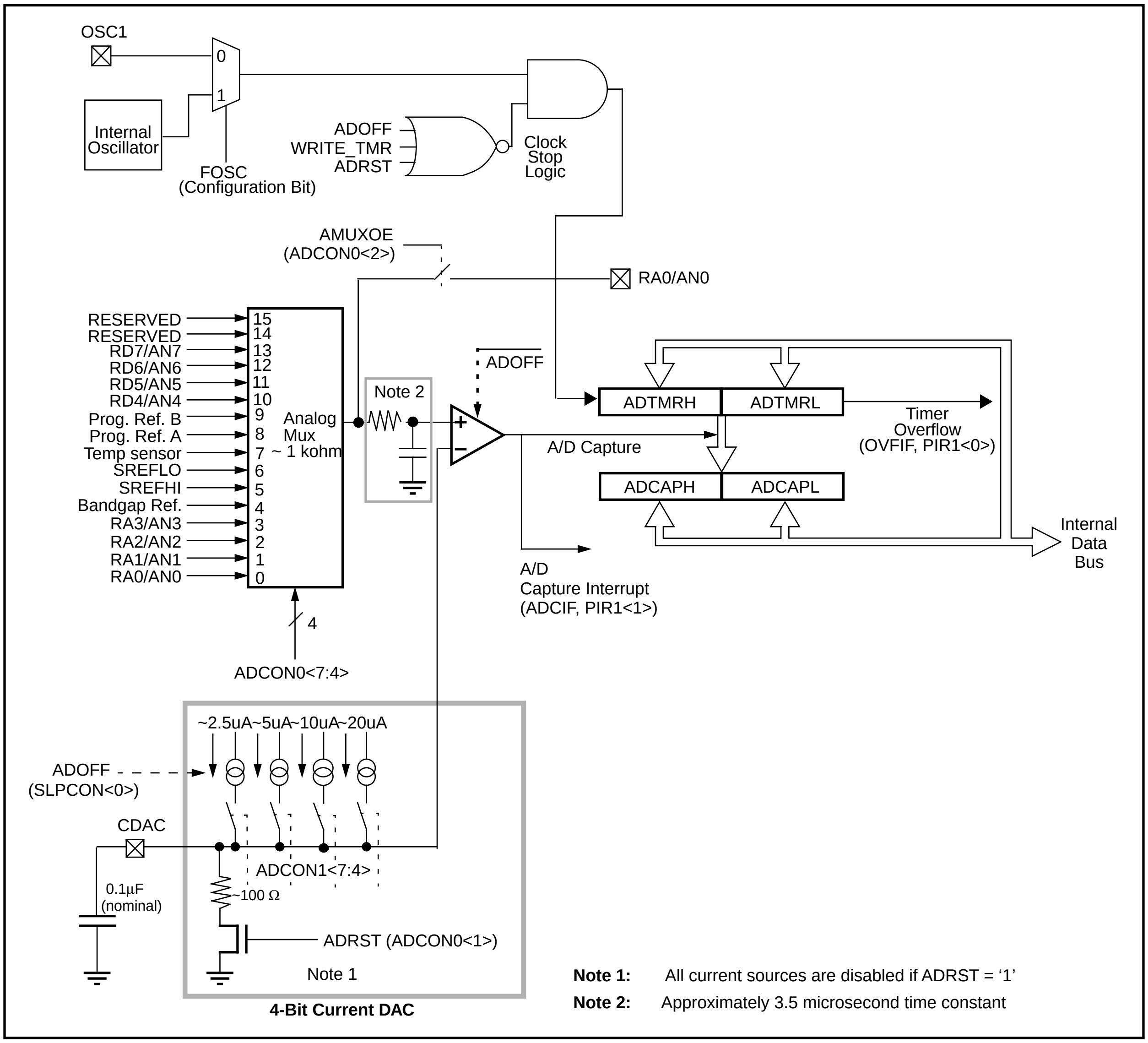
1. capture event
2. timer overflow

In a capture event, the comparator trips when the slope voltage on the CDAC output exceeds the input voltage, causing the comparator output to transition from high to low. This causes a transfer of the current timer count to the capture register and sets the ADCIF flag (PIR1<1>).

A CPU interrupt will be generated if bit ADCIE (PIE1<1>) is set to ‘1’ (interrupt enabled). In addition, the Global Interrupt Enable and Peripheral Interrupt Enables (INTCON<7,6>) must also be set. Software is responsible for clearing the ADCIF flag prior to the next conversion cycle. Note that this interrupt can only occur once per conversion cycle.

In a timer overflow condition, the timer rolls over from FFFFh to 0000h, and a capture overflow flag (OVFIF) is asserted (PIR1<0>). The timer continues to increment following a timer overflow. A CPU interrupt can be generated if bit OVFIE (PIE1<0>) is set (interrupt enabled). In addition, the Global Interrupt Enable and Peripheral Interrupt Enables (INTCON<7,6>) must also be set. Software is responsible for clearing the OVFIF flag prior to the next conversion cycle.

FIGURE 8-1: A/D BLOCK DIAGRAM



9.0 OTHER ANALOG MODULES

The PIC14000 has additional analog modules for mixed signal applications. These include:

- bandgap voltage reference
- comparators with programmable references
- internal temperature sensor
- voltage regulator control

9.1 Bandgap Voltage Reference

The bandgap reference circuit is used to generate a 1.2V nominal stable voltage reference for the A/D and the low-voltage detector. The bandgap reference is channel 4 of the analog mux. The bandgap reference voltage is stored in the calibration space EPROM (See Table 4-2). To enable the bandgap reference REFOFF (SLPCON<5>) must be cleared.

9.2 Level-Shift Networks

The RA1/AN1 and RA5/AN5 pins have an internal level-shift network. A current source and resistor are used to bias the pin voltage by about +0.5V into a range usable by the A/D converter. The nominal value of bias current source is 5 µA and the resistor is 100 kohms.

The level-shift function can be turned on by clearing the LSOFF bit (SLPCON<4>) to '0'.

Note:	The minimum voltage permissible at the RA1/AN1 and RA5/AN5 pins is -0.3V. The input protection diodes will begin to turn on beyond -0.3V, introducing significant errors in the A/D readings. Under no conditions should the pin voltage fall below -0.5V.

9.2.1 ZEROING/FILTERING SWITCHES

The RA1/AN1 and RA5/AN5 inputs also have a matched pair of pass gates useful for current-measurement applications. One gate is connected between the pin and the level-shift network. The second pass gate is connected to ground as shown in Figure 9-1. By setting the ADZERO bit (ADCON0<0>), a zero-current condition is simulated. Subsequent A/D readings are calculated relative to this zero count from the A/D. This zeroing of the current provides very high accuracies at low current values where it is most needed.

For additional noise filtering or for capturing short duration periodic pulses, an optional filter capacitor may be connected from the SUM pin to ground (this feature is available for RA1/AN1 only). This forms an RC network with the internal 100 kohm (nominal) bias resistor to act as a low pass filter. The capacitor size can be adjusted for the desired time constant.

A switch is included between the output from the RA1/AN1 level-shift network and the SUM pin. This switch is closed during A/D sampling periods and is automatically opened during a zeroing operation (if ADZERO = '1'). If not required in the system, this pin should be left floating (not connected).

Setting the LSOFF bit (SLPCON<4>) disables the level-shift networks, so the RA1/AN1 and RA5/AN5 pins can continue to be used as general-purpose analog inputs.

FIGURE 9-5: COMPARATOR CONTROL REGISTER

9Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMCON	U	CMBOUT	CMBOE	CPOLB	U	CMAOUT	CMAOE	CPOLA
Read/Write	—	R	R/W	R/W	—	R	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7	—	Unimplemented. Read as ‘0’.
B6	CMBOUT	Comparator B Output Reading this bit returns the status of the comparator B output. Writes to this bit have no effect.
B5	CMBOE	Comparator B Output Enable 1 = Comparator B output is available on RD2/CMPB pin and Reference B output is available on RD3/REFB pin. 0 = RD2/CMPB and RD3/REFB assume normal PORTD function.
B4	CPOLB	Comparator B Polarity Bit 1 = Invert the output of comparator B. 0 = Do not invert the output of comparator B.
B3	—	Unimplemented. Read as ‘0’.
B2	CMAOUT	Comparator A Output Reading this bit returns the status of the comparator A output. Writes to this bit have no effect.
B1	CMAOE	Comparator A Output Enable 1 = Comparator A output is available on RC1/CMPA pin and Reference A output is available on RC0/REFA pin. 0 = RC0/REFA and RC1/CMPA assume normal PORTC function.
B0	CPOLA	Comparator A Polarity Bit 1 = Invert the output of comparator A. 0 = Do not invert the output of comparator A.

FIGURE 9-6: PREFA REGISTER

9Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREFA	PRA7	PRA6	PRA5	PRA4	PRA3	PRA2	PRA1	PRA0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B0	PRA7 PRA6 PRA5 PRA4 PRA3 PRA2 PRA1 PRA0	Programmable Reference A Voltage Select Bits. See Table 9-1 and Table 9-2 for decoding.

FIGURE 9-7: PREFB REGISTER

9Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PREFB	PRB7	PRB6	PRB5	PRB4	PRB3	PRB2	PRB1	PRB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR value 00h	0	0	0	0	0	0	0	0

Bit	Name	Function
B7-B0	PRB7 PRB6 PRB5 PRB4 PRB3 PRB2 PRB1 PRB0	Programmable Reference B Voltage Select Bits. See Table 9-1 and Table 9-2 for decoding.

10.2 Oscillator Configurations

The PIC14000 can be operated with two different oscillator options. The user can program a configuration word (CONFIG<0>) to select one of these:

- HS High Speed Crystal/Ceramic Resonator (CONFIG<0> =‘0’)
- IN Internal oscillator (CONFIG<0> =‘1’) (Default)

10.2.1 INTERNAL OSCILLATOR CIRCUIT

The PIC14000 includes an internal oscillator option that offers additional cost and board-space savings. No external components are required. The nominal operating frequency is 4 MHz. The frequency is measured and stored into the calibration space in EPROM.

By selecting IN mode OSC1/PBTN becomes a digital input (with weak internal pull-up resistor) and can be read via bit MISC<0>. Writes to this location have no effect. The OSC1/PBTN input is capable of generating an interrupt to the CPU if enabled (Section 10.6). Also, the OSC2 pin becomes a digital output for general purpose use and is accessed via MISC<1>. Writes to this bit directly affect the OSC2 pin. Reading this bit returns the contents of the output latch. The MISC register format is shown in Figure 10-2.

The OSC2 pin can also output the IN oscillator frequency, divided-by-four, by setting INCLKEN (MISC<2>).

Note: The OSC2 output buffer provides less drive than standard I/O.

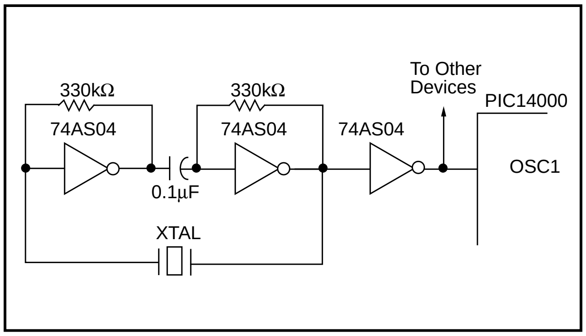
FIGURE 10-2: MISC REGISTER

9Eh	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
MISC	SMHOG	SPGNDB	SPGNDA	I^2CSEL	SMBUS	INCLKEN	OSC2	OSC1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
POR value 00h	0	0	0	0	0	0	0	X

Bit	Name	Function
B7	SMHOG	SMHOG enable 1 = Stretch I^2C CLK signal (hold low) when receive data buffer is full (refer to Section 7.5.4). For pausing I^2C transfers while preventing interruptions of A/D conversions. 0 = Disable I^2C CLK stretch.
B6	SPGNDB	Serial Port Ground Select 1 = PORTD<1:0> ground reference is the RD5/AN5 pin. 0 = PORTD<1:0> ground reference is Vss.
B5	SPGNDA	Serial Port Ground Select 1 = PORTC<7:6> ground reference is the RA1/AN1 pin. 0 = PORTC<7:6> ground reference is Vss.
B4	I^2CSEL	I^2C Port select Bit. 1 = PORTD<1:0> are used as the I^2C clock and data lines. 0 = PORTC<7:6> are used as the I^2C clock and data lines.
B3	SMBus	SMBus-Compatibility Select 1 = SMBus compatibility mode is enabled. PORTC<7:6> and PORTD<1:0> have SMBus-compatible input thresholds. 0 = SMBus-compatibility is disabled. PORTC<7:6> and PORTD<1:0> have Schmitt Trigger input thresholds.
B2	INCLKEN	Oscillator Output Select (available in IN mode only). 1 = Output IN oscillator signal divided by four on OSC2 pin. 0 = Disconnect IN oscillator signal from OSC2 pin.
B1	OSC2	OSC2 output port bit (available in IN mode only). Writes to this location affect the OSC2 pin in IN mode. Reads return the value of the output latch.
B0	OSC1	OSC1 input port bit (available in IN mode only). Reads from this location return the status of the OSC1 pin in IN mode. Writes have no effect.

Figure 10-6 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 10-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



10.3 Reset

The PIC14000 differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during SLEEP
- WDT Reset (normal operation)

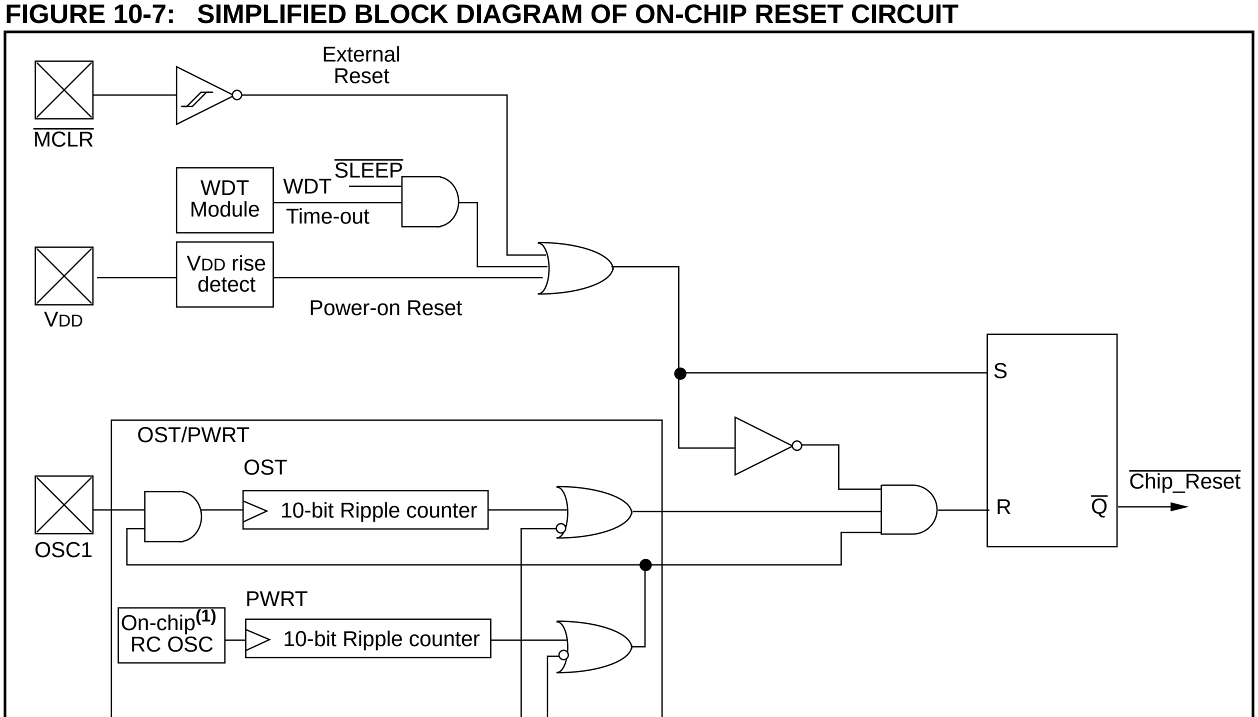
Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), on the $\overline{\text{MCLR}}$ and WDT Reset, and on $\overline{\text{MCLR}}$ Reset during SLEEP. They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different reset situations as indicated in Table 10-3. These bits are used in software to determine the nature of the reset. See Table 10-5 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 10-7.

The devices all have a $\overline{\text{MCLR}}$ noise filter in the $\overline{\text{MCLR}}$ reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

FIGURE 10-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.

10.6.2 TIMER0 INTERRUPT

An overflow (FFh → 00h) in Timer0 will set the T0IF (INTCON<2>) flag. Setting T0IE (INTCON<5>) enables the interrupt.

10.6.3 PORTC INTERRUPT ON CHANGE

An input change on PORTC<7:4> sets RCIF (PIR1<2>). Setting RCIE (PIE1<2>) enables the interrupt. For operation of PORTC, refer to Section 5.2.

> **Note:** If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RCIF interrupt flag may not be set.

10.6.4 CONTEXT SWITCHING DURING INTERRUPTS

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, for example, W register and Status register. Example 10-1 is an example that shows saving registers in RAM.

EXAMPLE 10-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF    W_TEMP           ;Copy W to TEMP register, could be any bank
SWAPF    STATUS,W         ;Swap status to be saved into W
BCF      STATUS,RP1       ;Change to bank zero, regardless of current bank
BCF      STATUS,RP0       ;
MOVWF    STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF    STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                          ;(sets bank to original state)
MOVWF    STATUS           ;Move W into STATUS register
SWAPF    W_TEMP,F         ;Swap W_TEMP
SWAPF    W_TEMP,W         ;Swap W_TEMP into W
```


MPASM allows full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PIC16/17. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

12.11 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16/17 series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

12.12 C Compiler (MPLAB-C)

The MPLAB-C Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC16/17 family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display (PICMASTER emulator software versions 1.13 and later).

12.13 Fuzzy Logic Development System (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, edition for implementing more complex systems.

Both versions include Microchip's *fuzzy*LAB™ demonstration board for hands-on experience with fuzzy logic systems implementation.

12.14 MP-DriveWay™ – Application Code Generator

MP-DriveWay is an easy-to-use Windows-based Application Code Generator. With MP-DriveWay you can visually configure all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language. The output is fully compatible with Microchip's MPLAB-C C compiler. The code produced is highly modular and allows easy integration of your own code. MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

12.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

12.16 TrueGauge® Intelligent Battery Management

The TrueGauge development tool supports system development with the MTA11200B TrueGauge Intelligent Battery Management IC. System design verification can be accomplished before hardware prototypes are built. User interface is graphically-oriented and measured data can be saved in a file for exporting to Microsoft Excel.

12.17 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

13.0 ELECTRICAL CHARACTERISTICS FOR PIC14000 ABSOLUTE MAXIMUM RATINGS †

Ambient temperature under bias	-55°C to+ 125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$)	-0.5V to V_{DD} +0.6V
Voltage on V_{DD} with respect to V_{SS}	0 to +6.0 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (Note 2)	0 to +14 V
Total power Dissipation (Note 1)	1.0 W
Maximum Current out of V_{SS} pin	300mA
Maximum Current into V_{DD} pin	250mA
Input clamp current, I_{IK} (V_I <0 or V_I> V_{DD})	±20mA
Output clamp current, I_{OK} (V_O <0 or V_O>V_{DD})	±20mA
Maximum Output Current sunk by any I/O pin	25mA
Maximum Output Current sourced by any I/O pin	25mA
Maximum Current sunk by PORTA, PORTC, and PORTD(combined)	200mA
Maximum Current sourced by PORTA, PORTC, and PORTE (combined)	200mA
Maximum Current sunk by PORTC and PORTD (combined)	200mA
Maximum Current sourced by PORTC and PORTD (combined)	200mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.5 DC and AC Characteristics Graphs and Tables for PIC14000

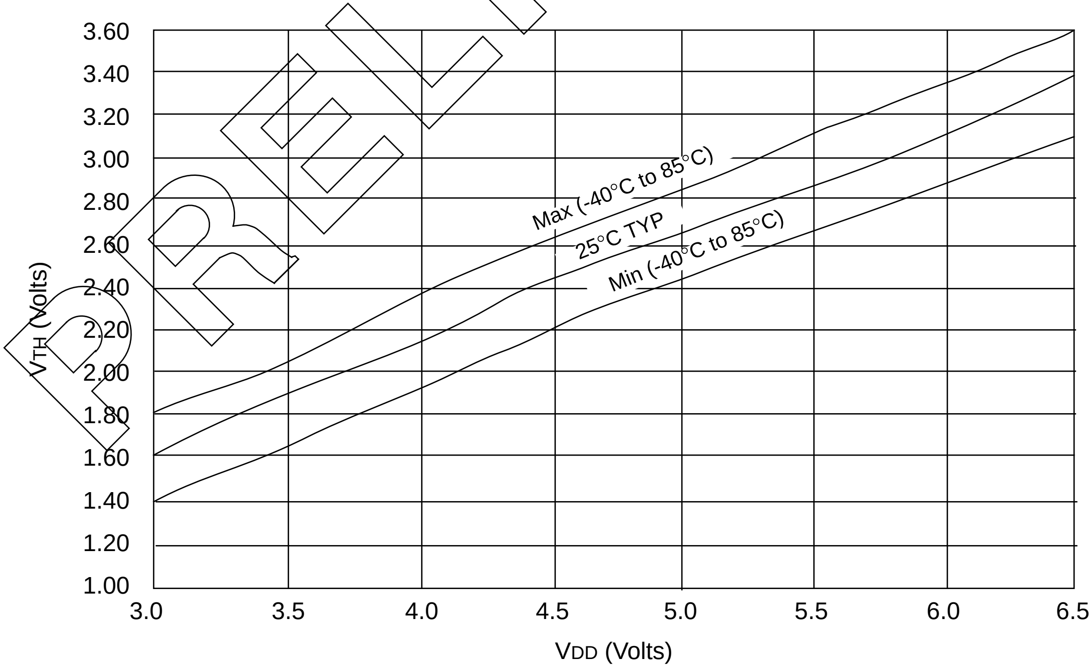
FIGURE 13-9: TYPICAL I_{PD4} vs V_{DD} AT 25°C

TO BE DETERMINED.

FIGURE 13-10: TYPICAL I_{PD3} vs V_{DD} AT 25°C

TO BE DETERMINED.

FIGURE 13-11: V_{TH} (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN HS MODE) vs V_{DD}



Standard Operating Conditions (unless otherwise stated)

Operating Temperature: -40°C ≤ T_A ≤ +85°C for industrial
0°C ≤ T_A ≤ +70°C for commercial

V_{DD} range: 2.7V (min) to 6.0V (max) unless otherwise stated.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions	Notes
Programmable Reference(s) (continued)							
Lower Range Output Voltage	vo(pref)	0.304	0.384	0.464	V	T_A = 25°C PREFx<7:0> = D7h (215 decimal), max	
		0.114	0.144	0.174	V	PREFx<7:0> = F8h (248 decimal), min	
Coarse Resolution	resc(pref)	38.0	48.0	58.0	mV	PREFx<2:0> = constant	
Fine Resolution	resf(pref)	4.0	5.0	6.0	mV	PREFx<7:3> = constant	
Relative accuracy (linearity error)	racc(pref)	–1/2	—	+1/2	lsb	lsb = resolution within selected range	
Settling Time to < ±1/2 LSB	ts(pref)	—	1	10	µS	PREFx<7:0> transition from 7Fh to FFh	1
Temperature Coefficient	tc(pref)	—	0.39	—	%/°C	From Tmin to Tmax	1
Supply Sensitivity	ss(pref)	—	0.2	—	%/V	From VDDmin to VDDmax	1
Operating Current (on)	idd(pref)	—	5	10	µA	CMOFF = 0	2
Operating Current (off)	idd(pref)	—	0	—	µA	CMOFF = 1	2
Low-Voltage Detector							
Detect Voltage	v-(lvd)	2.43	2.55	2.67	V	Decreasing VDD	
Release Voltage	v+(lvd)	2.48	2.60	2.72	V	Increasing VDD	
Hysteresis	vhys(lvd)	35	55	75	mV	Between detect and release trip points	
Operating Current (on)	idd(lvd)	—	15	25	µA	REFOFF = 0	2
Operating Current (off)	idd(lvd)	—	0	—	µA	REFOFF = 1	2
Internal Oscillator							
Frequency Range	fosc(in)	3.0	4.0	5.0	MHz		
Temperature Coefficient	tc(in)	—	-0.04	—	%/°C	From Tmin to Tmax	1
Supply Sensitivity	ss(in)	—	0.8	—	%/V	From VDDmin to VDDmax	1
Jitter	jit(in)	—	100	—	ppm	±3 sigma from mean	1
Start-up Time	tsu(in)	—	8	—	Tcycs	At Power-On Reset and exit from SLEEP	4
Operating Current (oscillator on)	idd(in)	—	300	500	µA		2
Operating Current (oscillator off)	idd(in)	—	0	—	µA	SLEEP mode, OSCOFF = 1	2
Voltage Regulator Control Output							
Regulation Voltage	vo(reg)	5.2	5.9	6.6	V	Measured with Ivreg = 10µA at T_A = 25°C	
Temperature Coefficient	tc(vreg)	—	-0.2	—	%/°C	From Tmin to Tmax	1
Operating Current (Recommended)	idd(vreg)	1	–	10	µA	Determined by external components	
Operating Current		—	0	—		If VREG pin is open	

A.2 PIC16C5X Family of Devices

	Clock	Memory			Peripherals		Features		
	Maximum Frequency of Operation (MHz)	Program Memory (x12 words) EPROM	Program Memory (x12 words) ROM	RAM Data Memory (bytes)	Timer Module(s)	I/O Pins	Voltage Range (Volts)	Number of Instructions	Packages
PIC16C52	4	384	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC
PIC16C54	20	512	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C54A	20	512	—	25	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR54A	20	—	512	25	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C55	20	512	—	24	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C56	20	1K	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C57	20	2K	—	72	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16CR57B	20	—	2K	72	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C58A	20	2K	—	73	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR58A	20	—	2K	73	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

