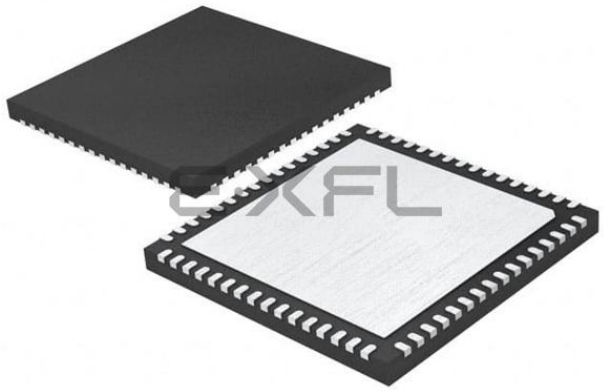


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65k22-i-mr

TABLE 1-3: PIC18F6XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	QFN/TQFP			
				PORTD is a bidirectional I/O port.
RD0/PSP0/CTPLS	58			
RD0		I/O	ST	Digital I/O.
PSP0		I/O	TTL	Parallel Slave Port data.
CTPLS		O	—	CTMU pulse generator output.
RD1/PSP1/T5CKI/T7G	55			
RD1		I/O	ST	Digital I/O.
PSP1		I/O	TTL	Parallel Slave Port.
T5CKI		I	ST	Timer5 clock input.
T7G		I	ST	Timer7 external clock gate input.
RD2/PSP2	54			
RD2		I/O	ST	Digital I/O.
PSP2		O	TTL	Parallel Slave Port.
RD3/PSP3	53			
RD3		I/O	ST	Digital I/O.
PSP3		I/O	TTL	Parallel Slave Port.
RD4/PSP4/SDO2	52			
RD4		I/O	ST	Digital I/O.
PSP4		I/O	TTL	Parallel Slave Port.
SDO2		O	—	SPI data out.
RD5/PSP5/SDI2/SDA2	51			
RD5		I/O	ST	Digital I/O.
PSP5		I/O	TTL	Parallel Slave Port.
SDI2		I	ST	SPI data in.
SDA2		I/O	I^2C	I^2C™ data I/O.
RD6/PSP6/SCK2/SCL2	50			
RD6		I/O	ST	Digital I/O.
PSP6		I/O	TTL	Parallel Slave Port.
SCK2		I/O	ST	Synchronous serial clock.
SCL2(4)		I/O	I^2C	Synchronous serial clock I/O for I^2C mode.
RD7/PSP7/$\overline{SS2}$	49			
RD7		I/O	ST	Digital I/O.
PSP7		I/O	TTL	Parallel Slave Port.
$\overline{SS2}$		I	TTL	SPI slave select input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C = I^2C™/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K22 and PIC18F85K22 devices.

4: The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

TABLE 1-4: PIC18F8XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTH is a bidirectional I/O port.
RH0/AN23/A16	79			
RH0		I/O	ST	Digital I/O.
AN23		I	Analog	Analog Input 23.
A16		I/O	TTL	External Memory Address/Data 16.
RH1/AN22/A17	80			
RH1		I/O	ST	Digital I/O.
AN22		I	Analog	Analog Input 22.
A17		I/O	TTL	External Address/Data 17.
RH2/AN21/A18	1			
RH2		I/O	ST	Digital I/O.
AN21		I	Analog	Analog Input 21.
A18		I/O	TTL	External Address/Data 18.
RH3/AN20/A19	2			
RH3		I/O	ST	Digital I/O.
AN20		I	Analog	Analog Input 20.
A19		I/O	TTL	External Address/Data 19.
RH4/CCP9/P3C/AN12/C2INC	22			
RH4		I/O	ST	Digital I/O.
CCP9(3,5)		I/O	ST	Capture 9 input/Compare 9 output/PWM9 output.
P3C		O	—	ECCP3 PWM Output C.
AN12		I	Analog	Analog Input 12.
C2INC		I	Analog	Comparator 2 Input C.
RH5/CCP8/P3B/AN13/C2IND	21			
RH5		I/O	ST	Digital I/O.
CCP8(5)		I/O	ST	Capture 8 input/Compare 8 output/PWM8 output.
P3B		O	—	ECCP3 PWM Output B.
AN13		I	Analog	Analog Input 13.
C2IND		I	Analog	Comparator 1 Input D.
RH6/CCP7/P1C/AN14/C1INC	20			
RH6		I/O	ST	Digital I/O.
CCP7(5)		I/O	ST	Capture 7 input/Compare 7 output/PWM7 output.
P1C		O	—	ECCP1 PWM Output C.
AN14		I	Analog	Analog Input 14.
C1INC		I	Analog	Comparator 1 Input C.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C = I^2C™/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K22 and PIC18F85K22 devices.

4: PSP is available only in Microcontroller mode.

5: The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

TABLE 1-4: PIC18F8XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTJ is a bidirectional I/O port.
RJ0/ALE	62			
RJ0		I/O	ST	Digital I/O.
ALE		O	—	External memory address latch enable.
RJ1/$\overline{OE}$	61			
RJ1		I/O	ST	Digital I/O.
$\overline{OE}$		O	—	External memory output enable.
RJ2/$\overline{WRL}$	60			
RJ2		I/O	ST	Digital I/O.
$\overline{WRL}$		O	—	External memory write low control.
RJ3/$\overline{WRH}$	59			
RJ3		I/O	ST	Digital I/O.
$\overline{WRH}$		O	—	External memory high control.
RJ4/BA0	39			
RJ4		I/O	ST	Digital I/O.
BA0		O	—	External Memory Byte Address 0 control
RJ5/$\overline{CE}$	40			
RJ5		I/O	ST	Digital I/O
$\overline{CE}$		O	—	External memory chip enable control.
RJ6/$\overline{LB}$	41			
RJ6		I/O	ST	Digital I/O.
$\overline{LB}$		O	—	External memory low byte control.
RJ7/$\overline{UB}$	42			
RJ7		I/O	ST	Digital I/O.
$\overline{UB}$		O	—	External memory high byte control.
VSS	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVSS	26	P	—	Ground reference for analog modules.
AVDD	25	P	—	Positive supply for analog modules.
ENVREG	24	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP	12			Core logic power or external filter capacitor connection.
VDDCORE				
VCAP		P	—	External filter capacitor connection (regulator enabled/disabled).

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); I^2C = I^2C™/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

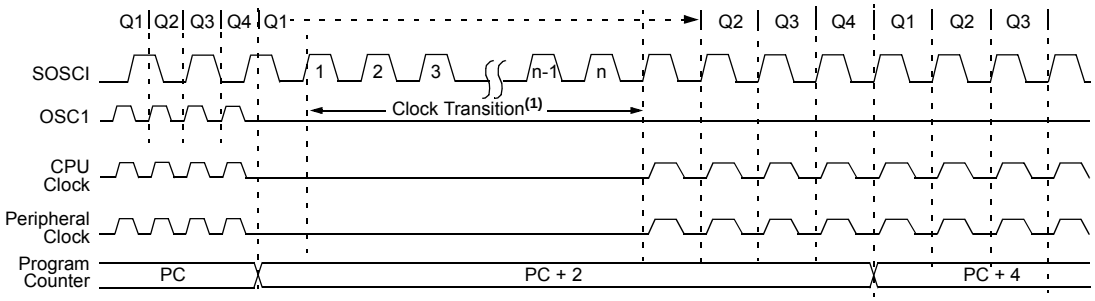
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K22 and PIC18F85K22 devices.

4: PSP is available only in Microcontroller mode.

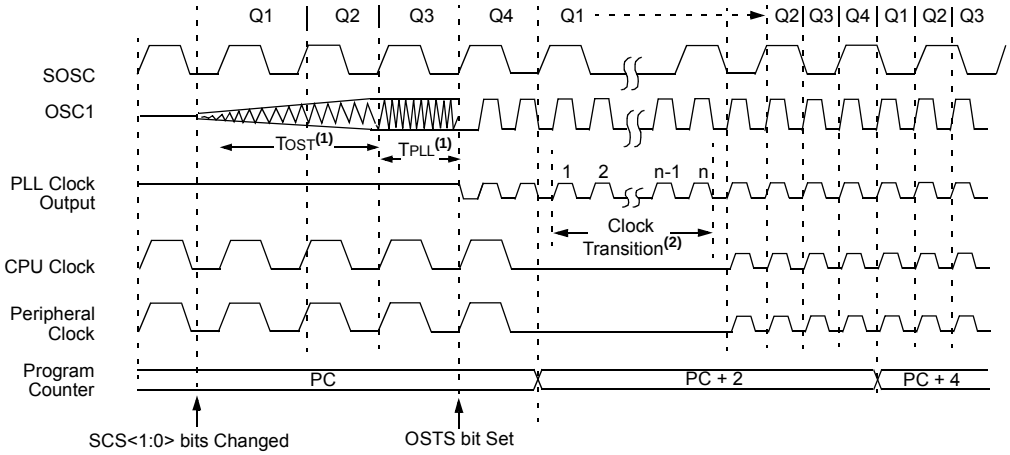
5: The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

FIGURE 4-1: TRANSITION TIMING FOR ENTRY TO SEC_RUN MODE



Note 1: Clock transition typically occurs within 2-4 TOSC.

FIGURE 4-2: TRANSITION TIMING FROM SEC_RUN MODE TO PRI_RUN MODE (HSPLL)



Note 1: TOST = 1024 TOSC; TPLL = 2 ms (approx). These intervals are not shown to scale.

2: Clock transition typically occurs within 2-4 TOSC.

6.1.3.2 Return Stack Pointer (STKPTR)

The STKPTR register (Register 6-1) contains the Stack Pointer value, the STKFUL (Stack Full) status bit and the STKUNF (Stack Underflow) status bits. The value of the Stack Pointer can be 0 through 31. The Stack Pointer increments before values are pushed onto the stack and decrements after values are popped off the stack. On Reset, the Stack Pointer value will be zero.

The user may read and write the Stack Pointer value. This feature can be used by a Real-Time Operating System (RTOS) for return stack maintenance.

After the PC is pushed onto the stack 31 times (without popping any values off the stack), the STKFUL bit is set. The STKFUL bit is cleared by software or by a POR.

What happens when the stack becomes full depends on the state of the STVREN (Stack Overflow Reset Enable) Configuration bit. (For a description of the device Configuration bits, see **Section 28.1 "Configuration Bits"**.) If STVREN is set (default), the 31st push will push the (PC + 2) value onto the stack, set the STKFUL bit and reset the device. The STKFUL bit will remain set and the Stack Pointer will be set to zero.

If STVREN is cleared, the STKFUL bit will be set on the 31st push and the Stack Pointer will increment to 31. Any additional pushes will not overwrite the 31st push and the STKPTR will remain at 31.

When the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC and set the STKUNF bit while the Stack Pointer remains at zero. The STKUNF bit will remain set until cleared by software or until a POR occurs.

Note:	Returning a value of zero to the PC on an underflow has the effect of vectoring the program to the Reset vector, where the stack conditions can be verified and appropriate actions can be taken. This is not the same as a Reset as the contents of the SFRs are not affected.

6.1.3.3 PUSH and POP Instructions

Since the Top-of-Stack (TOS) is readable and writable, the ability to push values onto the stack and pull values off of the stack, without disturbing normal program execution, is a desirable feature. The PIC18 instruction set includes two instructions, PUSH and POP, that permit the TOS to be manipulated under software control. TOSU, TOSH and TOSL can be modified to place data or a return address on the stack.

The PUSH instruction places the current PC value onto the stack. This increments the Stack Pointer and loads the current PC value onto the stack.

The POP instruction discards the current TOS by decrementing the Stack Pointer. The previous value pushed onto the stack then becomes the TOS value.

REGISTER 6-1: STKPTR: STACK POINTER REGISTER

R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKFUL(1)	STKUNF(1)	—	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **STKFUL:** Stack Full Flag bit(1)
1 = Stack has become full or overflowed
0 = Stack has not become full or overflowed

bit 6 **STKUNF:** Stack Underflow Flag bit(1)
1 = Stack underflow has occurred
0 = Stack underflow did not occur

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **SP<4:0>:** Stack Pointer Location bits

Note 1: Bit 7 and bit 6 are cleared by user software or by a POR.

TABLE 6-2: PIC18F87K22 FAMILY REGISTER FILE SUMMARY (CONTINUED)

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
F86h	PORTG	—	—	RG5(1)	RG4	RG3	RG2	RG1	RG0	--xx xxxx
F85h	PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—	xxxx xxx-
F84h	PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx xxxx
F83h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx
F82h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx
F81h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx
F80h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx
F7Fh	EECON1	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD	xx-0 x000
F7Eh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----
F7Dh	TMR5H	Timer5 Register High Byte								xxxx xxxx
F7Ch	TMR5L	Timer5 Register Low Byte								xxxx xxxx
F7Bh	T5CON	TMR5CS1	TMR5CS0	T5CKPS1	T5CKPS0	SOSCEN	$\overline{\text{T5SYNC}}$	RD16	TMR5ON	0000 0000
F7Ah	T5GCON	TMR5GE	T5GPOL	T5GTM	T5GSPM	$\overline{\text{T5GGO}}$/$\overline{\text{T5DONE}}$	T5GVAL	T5GSS1	T5GSS0	0000 0x00
F79h	CCPR4H	Capture/Compare/PWM Register 4 High Byte								xxxx xxxx
F78h	CCPR4L	Capture/Compare/PWM Register 4 Low Byte								xxxx xxxx
F77h	CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	--00 0000
F76h	CCPR5H	Capture/Compare/PWM Register 5 High Byte								xxxx xxxx
F75h	CCPR5L	Capture/Compare/PWM Register 5 Low Byte								xxxx xxxx
F74h	CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	--00 0000
F73h	CCPR6H	Capture/Compare/PWM Register 6 High Byte								xxxx xxxx
F72h	CCPR6L	Capture/Compare/PWM Register 6 Low Byte								xxxx xxxx
F71h	CCP6CON	—	—	DC6B1	DC6B0	CCP6M3	CCP6M2	CCP6M1	CCP6M0	--00 0000
F70h	CCPR7H	Capture/Compare/PWM Register 7 High Byte								xxxx xxxx
F6Fh	CCPR7L	Capture/Compare/PWM Register 7 Low Byte								xxxx xxxx
F6Eh	CCP7CON	—	—	DC7B1	DC7B0	CCP7M3	CCP7M2	CCP7M1	CCP7M0	--00 0000
F6Dh	TMR4	Timer4 Register								xxxx xxxx
F6Ch	PR4	Timer4 Period Register								1111 1111
F6Bh	T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-111 1111
F6Ah	SSP2BUF	MSSP Receive Buffer/Transmit Register								xxxx xxxx
F69h	SSP2ADD	MSSP Address Register in I^2C™ Slave Mode. MSSP1 Baud Rate Reload Register in I^2C Master Mode.								0000 0000
F68h	SSP2STAT	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	0000 0000
F67h	SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000
F66h	SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0100 0000
F65h	BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	0100 0-00
F64h	OSCCON2	—	SOSCRUN	—	—	SOSCGO	—	MFIOFS	MFIOSEL	-0-- 0-x0
F63h	EEADRH	EEPROM Address Register High Byte								0000 0000
F62h	EEADR	EEPROM Address Register Low Byte								0000 0000
F61h	EEDATA	EEPROM Data Register								0000 0000
F60h	PIE6	—	—	—	EEIE	—	CMP3IE	CMP2IE	CMP1IE	---0 -000
F5Fh	RTCCFG	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	0-00 0000
F5Eh	RTCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	0000 0000
F5Dh	RTCVALH	RTCC Value High Register Window Based on RTCPTR<1:0>								xxxx xxxx

Note 1: This bit is available when Master Clear is disabled (MCLRE = 0). When MCLRE is set, the bit is unimplemented.
2: Unimplemented on 64-pin devices (PIC18F6XK22), read as '0'.
3: Unimplemented on devices with a program memory of 32 Kbytes (PIC18FX5K22).

7.5.1 FLASH PROGRAM MEMORY WRITE SEQUENCE

The sequence of events for programming an internal program memory location should be:

1. Read the 64 or 128 bytes into RAM.
2. Update the data values in RAM as necessary.
3. Load the Table Pointer register with the address being erased.
4. Execute the row erase procedure.
5. Load the Table Pointer register with the address of the first byte being written.
6. Write the 64 or 128 bytes into the holding registers with auto-increment.
7. Set the EECON1 register for the write operation:
   - Set the EEPGD bit to point to program memory
   - Clear the CFGS bit to access program memory
   - Set the WREN to enable byte writes
8. Disable the interrupts.
9. Write 0x55 to EECON2.
10. Write 0xAA to EECON2.
11. Set the WR bit. This will begin the write cycle. The CPU will stall for duration of the write for TIW (see Parameter D133A).
12. Re-enable the interrupts.
13. Verify the memory (table read).

An example of the required code is shown in Example 7-3.

Note:	Before setting the WR bit, the Table Pointer address needs to be within the intended address range of the 64 or 128 bytes in the holding register.

Note:	Self-write execution to Flash and EEPROM memory cannot be done while running in LP Oscillator mode (Low-Power mode). Therefore, executing a self-write will put the device into High-Power mode.

REGISTER 11-5: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIF	—	SSP2IF	BCL2IF	BCL1IF	HLVDIF	TMR3IF	TMR3GIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **OSCFIF:** Oscillator Fail Interrupt Flag bit
1 = Device oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = Device clock is operating

bit 6 **Unimplemented:** Read as '0'

bit 5 **SSP2IF:** Master Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception has been completed (must be cleared in software)
0 = Waiting to transmit/receive

bit 4 **BCL2IF:** Bus Collision Interrupt Flag bit
1 = A bus collision occurred (must be cleared in software)
0 = No bus collision occurred

bit 3 **BCL1IF:** Bus Collision Interrupt Flag bit
1 = A bus collision occurred (must be cleared in software)
0 = No bus collision occurred

bit 2 **HLVDIF:** High/Low-Voltage Detect Interrupt Flag bit
1 = A low-voltage condition occurred (must be cleared in software)
0 = The device voltage is above the regulator's low-voltage trip point

bit 1 **TMR3IF:** TMR3 Overflow Interrupt Flag bit
1 = TMR3 register overflowed (must be cleared in software)
0 = TMR3 register did not overflow

bit 0 **TMR3GIF:** TMR3 Gate Interrupt Flag bit
1 = Timer gate interrupt occurred (must be cleared in software)
0 = No timer gate interrupt occurred

23.4 Selecting and Configuring Automatic Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/$\overline{\text{DONE}}$ bit is set.

When the GO/$\overline{\text{DONE}}$ bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/$\overline{\text{DONE}}$ bit.

This occurs when the ACQT<2:0> bits (ADCON2<5:3>) remain in their Reset state ('000'), which is compatible with devices that do not offer programmable acquisition times.

If desired, the ACQTx bits can be set to select a programmable acquisition time for the A/D module. When the GO/$\overline{\text{DONE}}$ bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/$\overline{\text{DONE}}$ bit.

In either case, when the conversion is completed, the GO/$\overline{\text{DONE}}$ bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

23.5 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 14 TAD per 12-bit conversion. The source of the A/D conversion clock is software-selectable.

The possible options for TAD are:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Using the internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD. (For more information, see Parameter 130 in Table 31-28.)

Table 23-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 23-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS<2:0>	
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	64.00 MHz
RC(2)	x11	1.00 MHz(1)

Note 1: The RC source has a typical TAD time of 4 μs.

2: For device frequencies above 1 MHz, the device must be in Sleep mode for the entire conversion or the A/D accuracy may be out of specification.

23.6 Configuring Analog Port Pins

The ANCON0, ANCON1, ANCON2, TRISA, TRISF, TRISG and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRISx bits set (input). If the TRISx bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRISx bits.

Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will be accurately converted.

2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

The module is enabled by setting the HLVDEN bit (HLVDCON<4>). Each time the HLVD module is enabled, the circuitry requires some time to stabilize. The IRVST bit (HLVDCON<5>) is a read-only bit used to indicate when the circuit is stable. The module can only generate an interrupt after the circuit is stable and IRVST is set.

The VDIRMAG bit (HLVDCON<7>) determines the overall operation of the module. When VDIRMAG is cleared, the module monitors for drops in VDD below a predetermined set point. When the bit is set, the module monitors for rises in VDD above the set point.

26.1 Operation

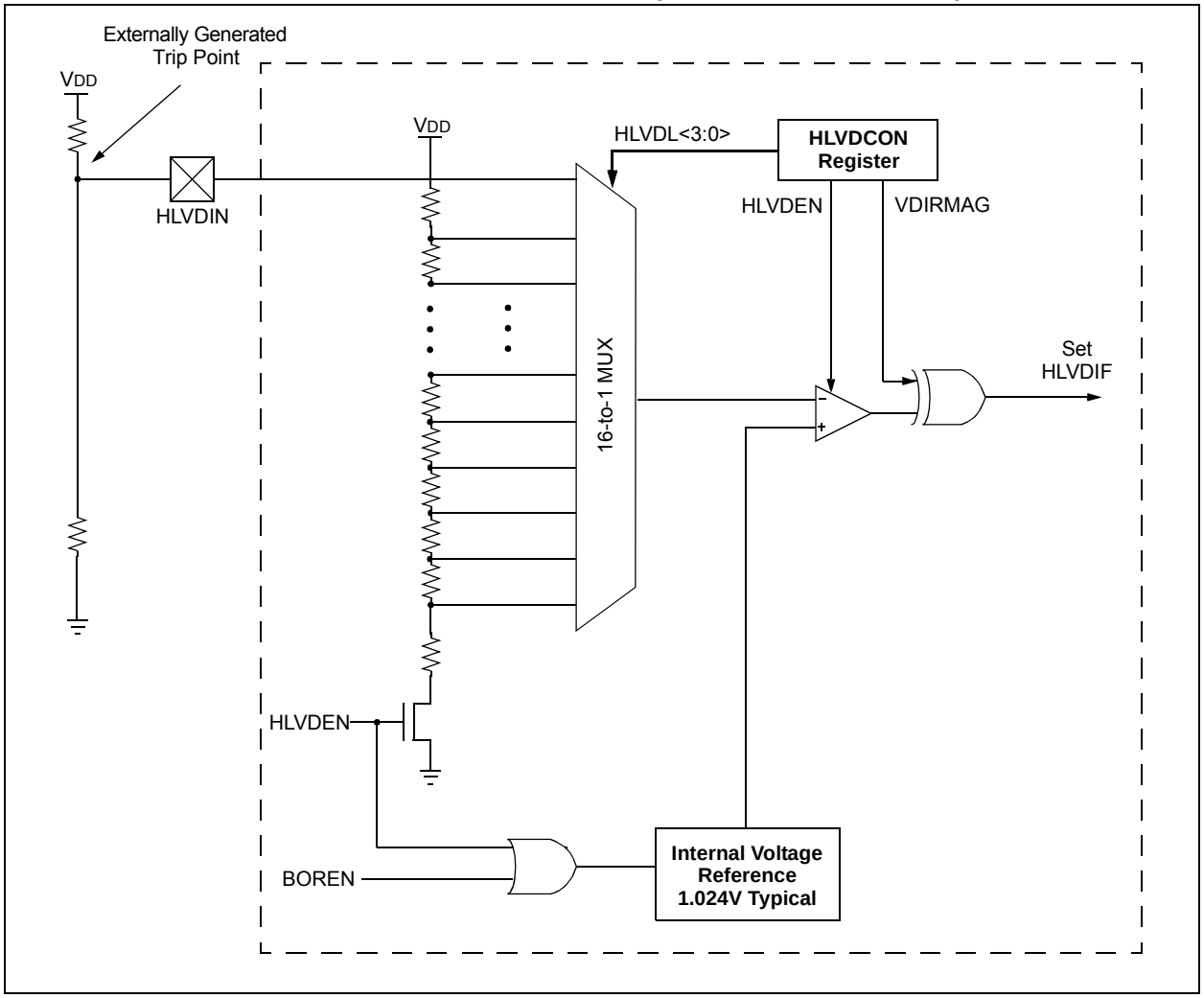
When the HLVD module is enabled, a comparator uses an internally generated voltage reference as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The "trip point" voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module.

When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit.

The trip point voltage is software programmable to any of 16 values. The trip point is selected by programming the HLVDL<3:0> bits (HLVDCON<3:0>).

The HLVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits, HLVDL<3:0>, are set to '1111'. In this state, the comparator input is multiplexed from the external input pin, HLVDIN. This gives users the flexibility of configuring the High/Low-Voltage Detect interrupt to occur at any voltage in the valid operating range.

FIGURE 26-1: HLVD MODULE BLOCK DIAGRAM (WITH EXTERNAL INPUT)



REGISTER 28-1: CONFIG1L: CONFIGURATION REGISTER 1 LOW (BYTE ADDRESS 300000h)

U-0	R/P-1	U-0	R/P-1	R/P-1	R/P-1	U-0	R/P-1
—	XINST	—	SOSCSEL1	SOSCSEL0	INTOSCSEL	—	$\overline{\text{RETEN}}$
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **XINST:** Extended Instruction Set Enable bit

1 = Instruction set extension and Indexed Addressing mode are enabled
0 = Instruction set extension and Indexed Addressing mode are disabled (Legacy mode)

bit 5 **Unimplemented:** Read as ‘0’

bit 4-3 **SOSCSEL<1:0>:** SOSC Power Selection and Mode Configuration bits

11 = High-power SOSC circuit is selected
10 = Digital (SCLKI) mode; I/O port functionality of RC0 and RC1 is enabled
01 = Low-power SOSC circuit is selected
00 = Reserved

bit 2 **INTOSCSEL:** LF-INTOSC Low-power Enable bit

1 = LF-INTOSC is in High-Power mode during Sleep
0 = LF-INTOSC is in Low-Power mode during Sleep

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **$\overline{\text{RETEN}}$:** VREG Sleep Enable bit

1 = Regulator power while in Sleep mode is controlled by VREGSLP (WDTCON<7>)
0 = Regulator power while in Sleep mode is controlled by SRETEN (WDTCON<4>). Ultra low-power regulator is enabled.

28.3.2 OPERATION OF REGULATOR IN SLEEP

The difference in the two regulators' operation arises with Sleep mode. The ultra low-power regulator gives the device the lowest current in the Regulator Enabled mode.

The on-chip regulator can go into a lower power mode, when the device goes to Sleep, by setting the REGSLP bit (WDTCON<7>). This puts the regulator in a Standby mode so that the device consumes much less current.

The on-chip regulator can also go into the Ultra Low-Power mode, which consumes the lowest current possible with the regulator enabled. This mode is controlled by the $\overline{\text{RETEN}}$ bit (CONFIG1L<0>) and SRETEN bit (WDTCON<4>).

The various modes of regulator operation are shown in Table 28-3.

When the ultra low-power regulator is in Sleep mode, the internal reference voltages in the chip will be shut off and any interrupts referring to the internal reference will not wake up the device. If the BOR or LVD is enabled, the regulator will keep the internal references on and the lowest possible current will not be achieved.

When using the ultra low-power regulator in Sleep mode, the device will take about 250 μs, typical, to start executing the code after it wakes up.

TABLE 28-3: SLEEP MODE REGULATOR SETTINGS(1)

Regulator	Power Mode	VREGSLP WDTCON<7>	SRETEN WDTCON<4>	$\overline{\text{RETEN}}$ CONFIG1L<0>
Enabled	Normal Operation (Sleep)	0	x	1
Enabled	Low-Power mode (Sleep)	1	x	1
Enabled	Normal Operation (Sleep)	0	0	x
Enabled	Low-Power mode (Sleep)	1	0	x
Enabled	Ultra Low-Power mode (Sleep)	x	1	0

Note 1: x = Indicates that VIT status is invalid.

INCFSZ **Increment f, Skip if 0**

Syntax: INCFSZ f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) + 1 → dest,
skip if result = 0

Status Affected: None

Encoding:

0011	11da	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If the result is '0', the next instruction which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    INCFSZ   CNT, 1, 0
NZERO   :
ZERO    :
```

Before Instruction
PC = Address (HERE)
After Instruction
CNT = CNT + 1
If CNT = 0;
PC = Address (ZERO)
If CNT ≠ 0;
PC = Address (NZERO)

INFSNZ **Increment f, Skip if Not 0**

Syntax: INFSNZ f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) + 1 → dest,
skip if result ≠ 0

Status Affected: None

Encoding:

0100	10da	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If the result is not '0', the next instruction which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    INFSNZ  REG, 1, 0
ZERO
NZERO
```

Before Instruction
PC = Address (HERE)
After Instruction
REG = REG + 1
If REG ≠ 0;
PC = Address (NZERO)
If REG = 0;
PC = Address (ZERO)

IORLW **Inclusive OR Literal with W**

Syntax: IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. k → W

Status Affected: N, Z

Encoding:

0000	1001	kkkk	kkkk

Description: The contents of W are ORed with the eight-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: IORLW 35h

Before Instruction
W = 9Ah
After Instruction
W = BFh

IORWF **Inclusive OR W with f**

Syntax: IORWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .OR. (f) → dest

Status Affected: N, Z

Encoding:

0001	00da	ffff	ffff

Description: Inclusive OR W with register 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: IORWF RESULT, 0, 1

Before Instruction
RESULT = 13h
W = 91h
After Instruction
RESULT = 13h
W = 93h

NEGF **Negate f**

Syntax: NEGF f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: $(\bar{f}) + 1 \rightarrow f$

Status Affected: N, OV, C, DC, Z

Encoding:

0110	110a	ffff	ffff

Description: Location ‘f’ is negated using two’s complement. The result is placed in the data memory location ‘f’.

If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank.

If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode”** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write register ‘f’

Example:
```
NEGF    REG, 1
```
Before Instruction
REG = 0011 1010 [3Ah]
After Instruction
REG = 1100 0110 [C6h]

NOP **No Operation**

Syntax: NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

0000 1111	0000 xxxx	0000 xxxx	0000 xxxx

Description: No operation.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation

Example:

None.

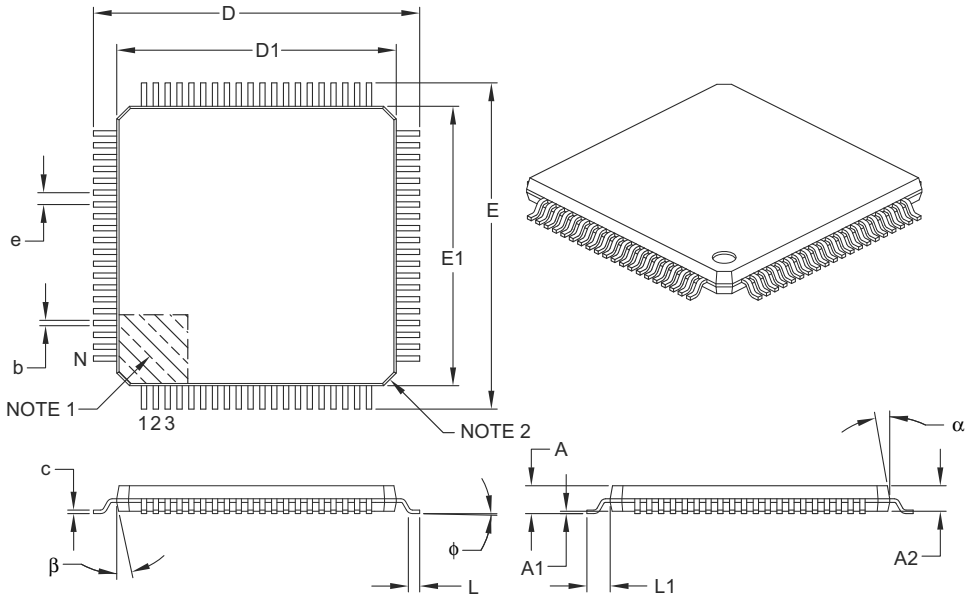
31.3 DC Characteristics: PIC18F87K22 Family (Industrial/Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O Ports:				
D030		with TTL Buffer	VSS	0.15 VDD	V	VDD < 4.5V
D031		with Schmitt Trigger Buffer	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
		RC3, RC4	VSS	0.2 VDD	V	VDD < 4.5
		RD5, RD6	VSS	1.5	V	4.5V ≤ VDD ≤ 5.5V
D031A		RC3, RC4	VSS	0.3 VDD	V	I2C™ enabled
D031B		RD5, RD6	VSS	0.8	V	SMBus enabled
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.2 VDD	V	LP, XT, HS modes
D033A		OSC1	VSS	0.2 VDD	V	EC modes
D034		SOSCI	VSS	0.3 VDD	V	
	VIH	**Input High Voltage**				
		I/O Ports with Analog Functions:				
D040		with TTL Buffer	0.25 VDD	VDD	V	VDD < 4.5V
			2.0	VDD	V	4.5V ≤ VDD ≤ 5.5V
D041		with Schmitt Trigger Buffer	0.8	VDD	V	VDD < 4.5V
		RC3, RC4	0.7 VDD	VDD	V	VDD < 4.5V
		RD5, RD6	3V	5.5	V	4.5V ≤ VDD ≤ 5.5V
D041A		RC3, RC4	0.7 VDD	VDD	V	I2C enabled
D041B		RD5, RD6	2.1	VDD	V	SMBus enabled
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.9 VDD	VDD	V	RC mode
D043A		OSC1	0.7 VDD	VDD	V	HS mode
D044		SOSCI	0.7 VDD	VDD	V	
	IIL	**Input Leakage Current(1)**				
D060		I/O Ports	±50	±200	nA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D061		$\overline{MCLR}$	—	±5	µA	Vss ≤ VPIN ≤ VDD, +85°C
D063		OSC1	—	±5	µA	Vss ≤ VPIN ≤ VDD
	IPU	**Weak Pull-up Current**				
D070	IPURB	PORTB Weak Pull-up Current	50	400	µA	VDD = 3.3V, VPIN = VSS

Note 1: Negative current is defined as current sourced by the pin.

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B

APPENDIX A: REVISION HISTORY

Revision A (November 2009)

Original data sheet for PIC18F87K22 family devices.

Revision B (May 2010)

Minor edits to text throughout document. Replaced all TBDs with the correct value.

Revision C (March 2011)

Section 2.4 "Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)" has been replaced with a new and more detailed description and the 80-pin TQFP diagrams have been updated. Minor text edits throughout document.

Revision D (June 2011)

Updated **Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial/Extended)"** and Table 31-8 with new electrical specification information. The extended temperature information has been included in this revision.

APPENDIX B: MIGRATION FROM PIC18F87J11 AND PIC18F8722 TO PIC18F87K22

Devices in the PIC18F87K22, PIC18F87J11 and PIC18F8722 families are similar in their functions and features. Code can be migrated from the other families to the PIC18F87K22 without many changes. The differences between the device families are listed in Table B-1.

TABLE B-1: NOTABLE DIFFERENCES BETWEEN PIC18F87K22, PIC18F87J11 AND PIC18F8722 FAMILIES

Characteristic	PIC18F87K22 Family	18F87J11 Family	PIC18F8722 Family
Max Operating Frequency	64 MHz	48 MHz	40 MHz
Max Program Memory	128 Kbytes	128 Kbytes	128 Kbytes
Data Memory	3,862 bytes	3,930 bytes	3,930 bytes
Program Memory Endurance	10,000 Write/Erase (minimum)	10,000 Write/Erase (minimum)	10,000 Write/Erase (minimum)
Single Word Write for Flash	No	Yes	No
Oscillator Options	PLL can be used with INTOSC	PLL can be used with INTOSC	PLL can be used with INTOSC
CTMU	Yes	No	No
RTCC	Yes	No	No
SOSC Oscillator Options TICKI Clock	Low-Power Oscillator Option for SOSC T1CKI can be used as a Clock without Enabling the SOSC Oscillator	No	No
INTOSC	Up to 16 MHz	Up to 8 MHz	Up to 8 MHz
SPI/I^2C™	2	2	2
Timers	11	5	5
ECCP	3	3	
CCP	7	2	2
Data EEPROM	Yes	No	Yes
Programmable BOR	Multiple Level BOR	One Level BOR	Multiple Level BOR
WDT Prescale Options	22	16	16
5V Operation	Yes	No (3.3V)	Yes
nanoWatt XLP	Yes	No	No
Regulator	Yes	Yes	No
Low-Power BOR	Yes	No	No
A/D Converter	12-Bit Resolution, 24 Input Channels, Differential	10-Bit Resolution, 15 Input Channels, Non-Differential	10-Bit Resolution, 16 Input Channels, Non-Differential
Internal Temperature Sensor	Yes	No	No
Programmable HLVD	Yes	No	Yes
EUSART	2 EUSARTs	2 EUSARTs	2 EUSARTs
Comparators	3	2	2
Oscillator options	14 Options by FOSC<3:0>	8 Options by FOSC<3:0>	12 Options by FOSC<3:0>
Ultra-Low-Power Wake-up (ULPW)	Yes	No	No
Power-up Timer	Yes	Yes	Yes
$\overline{MCLR}$ Pin as Input Port	Yes	No	Yes

Q

R