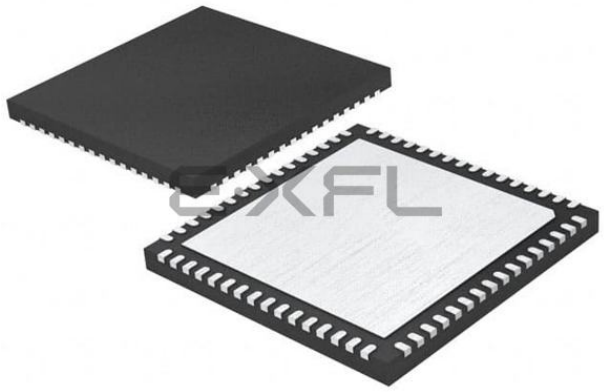
Microchip Technology - PIC18F65K22T-I/MRRSL Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65k22t-i-mrrsl

TABLE 1-4: PIC18F8XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RE6/P1B/CCP6/AD14	74			
RE6		I/O	ST	Digital I/O.
P1B		O	—	ECCP1 PWM Output B.
CCP6(5)		I/O	ST	Capture 6 input/Compare 6 output/PWM6 output.
AD14		I/O	ST	External Memory Address/Data 14.
RE7/ECCP2/P2A/AD15	73			
RE7		I/O	ST	Digital I/O.
ECCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A		O	—	ECCP2 PWM Output A.
AD15		I/O	ST	External Memory Address/Data 15.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); I^2C = I^2C™/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K22 and PIC18F85K22 devices.

4: PSP is available only in Microcontroller mode.

5: The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
INDF2	PIC18F6XK22	PIC18F8XK22	N/A	N/A	N/A
POSTINC2	PIC18F6XK22	PIC18F8XK22	N/A	N/A	N/A
POSTDEC2	PIC18F6XK22	PIC18F8XK22	N/A	N/A	N/A
PREINC2	PIC18F6XK22	PIC18F8XK22	N/A	N/A	N/A
PLUSW2	PIC18F6XK22	PIC18F8XK22	N/A	N/A	N/A
FSR2H	PIC18F6XK22	PIC18F8XK22	---- xxxx	----uuuu	---- uuuu
FSR2L	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	PIC18F6XK22	PIC18F8XK22	---x xxxx	---u uuuu	---u uuuu
TMR0H	PIC18F6XK22	PIC18F8XK22	0000 0000	uuuu uuuu	uuuu uuuu
TMR0L	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	PIC18F6XK22	PIC18F8XK22	1111 1111	1111 1111	uuuu uuuu
SPBRGH1	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
OSCCON	PIC18F6XK22	PIC18F8XK22	0110 q000	0110 q000	uuuu quuu
IPR5	PIC18F65K22	PIC18F85K22	---1 -111	---1 -111	---u -uuu
IPR5	PIC18F66K22 PIC18F67K22	PIC18F86K22 PIC18F87K22	1000 0000	1000 0000	uuuu uuuu
WDTCON	PIC18F6XK22	PIC18F8XK22	0-x0 -000	0-x0 -000	u-uu -uuu
RCON	PIC18F6XK22	PIC18F8XK22	0111 11qq	0uqq qquu	uuuu qquu
TMR1H	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	PIC18F6XK22	PIC18F8XK22	0000 0000	uuuu uuuu	uuuu uuuu
TMR2	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
PR2	PIC18F6XK22	PIC18F8XK22	1111 1111	1111 1111	uuuu uuuu
T2CON	PIC18F6XK22	PIC18F8XK22	-000 0000	-000 0000	-uuu uuuu
SSP1BUF	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSP1ADD	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
SSP1STAT	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
SSP1CON1	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
SSP1CON2	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
ADRESH	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADRESL	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	PIC18F6XK22	PIC18F8XK22	-000 0000	-000 0000	-uuu uuuu
ADCON1	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
ADCON2	PIC18F6XK22	PIC18F8XK22	0-00 0000	0-00 0000	u-uu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.
Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for Reset value for specific condition.

REGISTER 11-11: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIE	—	SSP2IE	BCL2IE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **OSCFIE:** Oscillator Fail Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **SSP2IE:** Master Synchronous Serial Port 2 Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 4 **BCL2IE:** Bus Collision Interrupt Enable bit
1 = Enables the bus collision interrupt
0 = Disables the bus collision interrupt

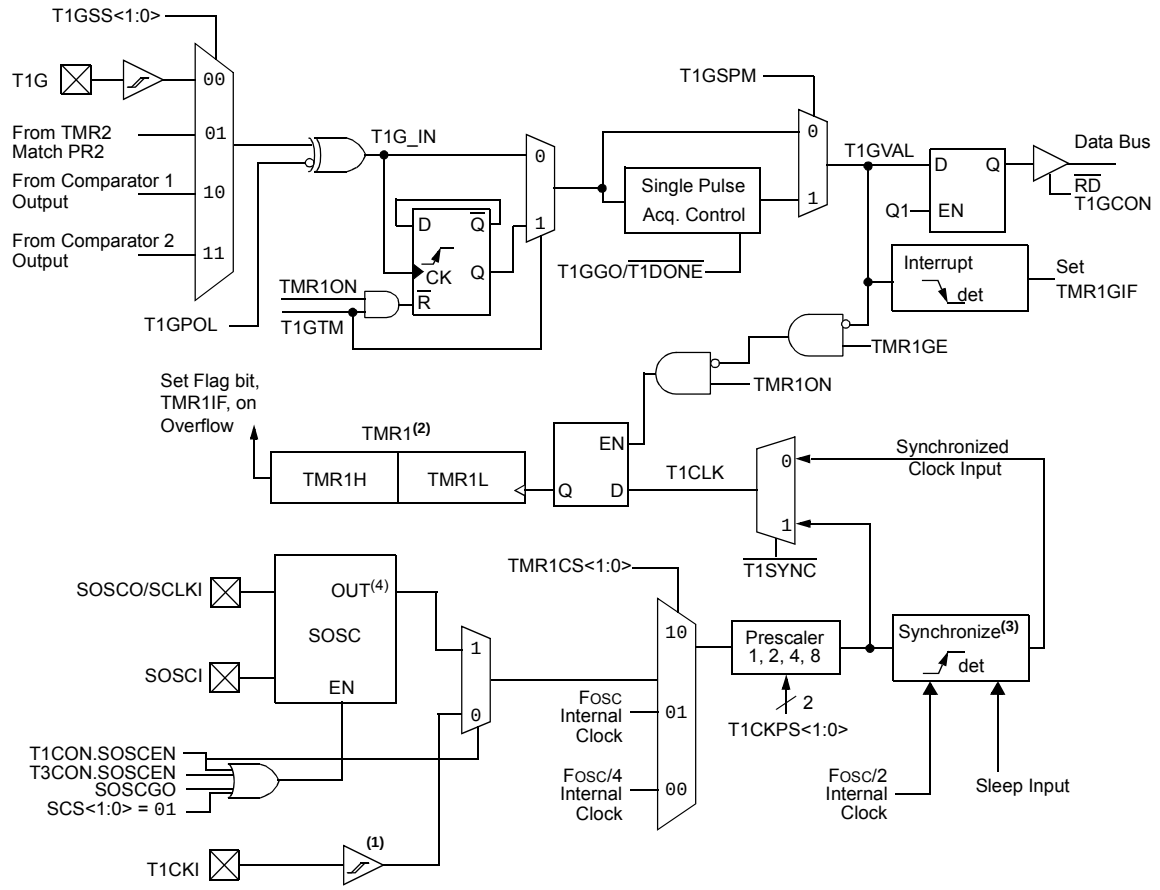
bit 3 **BCL1IE:** Bus Collision Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **HLVDIE:** High/Low-Voltage Detect Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **TMR3IE:** TMR3 Overflow Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **TMR3GIE:** Timer3 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

FIGURE 14-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is a high-speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronization does not operate while in Sleep.
4: The output of SOSC is determined by the SOSCSEL<1:0> Configuration bits.

REGISTER 16-3: OSCCON2: OSCILLATOR CONTROL REGISTER 2

U-0	R-0	U-0	U-0	R/W-0	U-0	R-x	R/W-0
—	SOSCRUN	—	—	SOSCGO	—	MFIOFS	MFIOSEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **SOSCRUN:** SOSC Run Status bit
1 = System clock comes from a secondary SOSC
0 = System clock comes from an oscillator other than SOSC

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3 **SOSCGO:** Oscillator Start Control bit
1 = Oscillator is running even if no other sources are requesting it
0 = Oscillator is shut off if no other sources are requesting it (When the SOSC is selected to run from a digital clock input, rather than an external crystal, this bit has no effect.)

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **MFIOFS:** MF-INTOSC Frequency Stable bit
1 = MF-INTOSC is stable
0 = MF-INTOSC is not stable

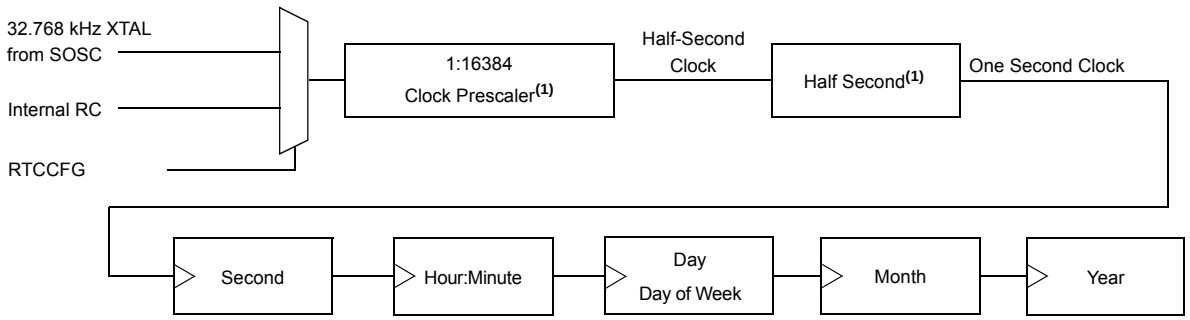
bit 0 **MFIOSEL:** MF-INTOSC Select bit
1 = MF-INTOSC is used in place of HF-INTOSC frequencies of 500 kHz, 250 kHz and 31.25 kHz
0 = MF-INTOSC is not used

18.2.2 CLOCK SOURCE

As previously mentioned, the RTCC module is intended to be clocked by an external Real-Time Clock (RTC) crystal, oscillating at 32.768 kHz, but an internal oscillator can be used. The RTCC clock selection is decided by the RTCOSC bit (CONFIG3L<0>).

Calibration of the crystal can be done through this module to yield an error of 3 seconds or less per month. (For further details, see **Section 18.2.9 "Calibration"**.)

FIGURE 18-4: CLOCK SOURCE MULTIPLEXING



Note 1: Writing to the lower half of the MINSEC register resets all counters, allowing fraction of a second synchronization; clock prescaler is held in Reset when RTCEN = 0.

18.2.2.1 Real-Time Clock Enable

The RTCC module can be clocked by an external, 32.768 kHz crystal (SOSC oscillator) or the LF-INTOSC oscillator, which can be selected in CONFIG3L<0>.

If the external clock is used, the SOSC oscillator should be enabled. If LF-INTOSC is providing the clock, the INTOSC clock can be brought out to the RTCC pin by the RTSECSEL<1:0> bits (PADCFG<2:1>).

18.2.3 DIGIT CARRY RULES

This section explains which timer values are affected when there is a rollover:

- Time of Day: From 23:59:59 to 00:00:00 with a carry to the Day field
- Month: From 12/31 to 01/01 with a carry to the Year field
- Day of Week: From 6 to 0 with no carry (see Table 18-1)
- Year Carry: From 99 to 00; this also surpasses the use of the RTCC

For the day-to-month rollover schedule, see Table 18-2.

Because the following values are in BCD format, the carry to the upper BCD digit occurs at the count of 10, not 16 (SECONDS, MINUTES, HOURS, WEEKDAY, DAYS and MONTHS).

TABLE 18-1: DAY OF WEEK SCHEDULE

Day of Week	
Sunday	0
Monday	1
Tuesday	2
Wednesday	3
Thursday	4
Friday	5
Saturday	6

TABLE 18-2: DAY TO MONTH ROLLOVER SCHEDULE

Month	Maximum Day Field
01 (January)	31
02 (February)	28 or 29(1)
03 (March)	31
04 (April)	30
05 (May)	31
06 (June)	30
07 (July)	31
08 (August)	31
09 (September)	30
10 (October)	31
11 (November)	30
12 (December)	31

Note 1: See **Section 18.2.4 "Leap Year"**.

NOTES:

19.4 PWM Mode

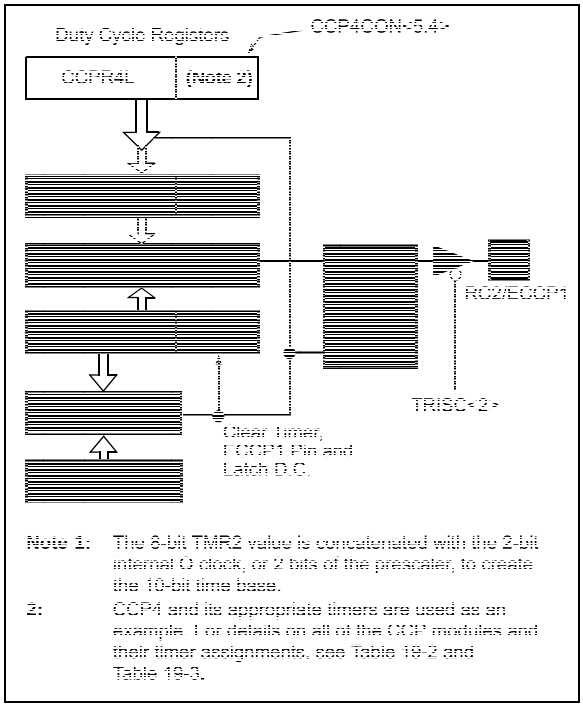
In Pulse-Width Modulation (PWM) mode, the CCP4 pin produces up to a 10-bit resolution PWM output. Since the CCP4 pin is multiplexed with a PORTC or PORTE data latch, the appropriate TRIS bit must be cleared to make the CCP4 pin an output.

Note:	Clearing the CCP4CON register will force the RC1 or RE7 output latch (depending on device configuration) to the default low level. This is not the PORTC or PORTE I/O data latch.

Figure 19-3 shows a simplified block diagram of the ECCP1 module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 19.4.3 "Setup for PWM Operation"**.

FIGURE 19-3: SIMPLIFIED PWM BLOCK DIAGRAM

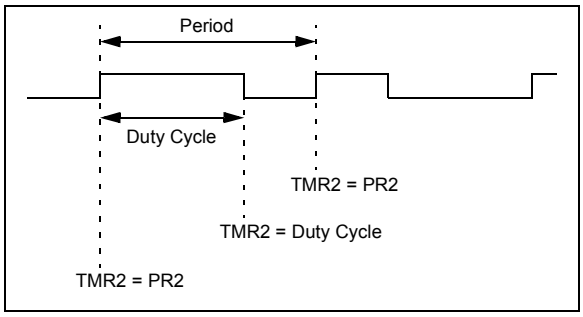


Note 1: The 8-bit TMR2 value is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler, to create the 10-bit time base.

2: CCP4 and its appropriate timers are used as an example. For details on all of the CCP modules and their timer assignments, see Table 19-2 and Table 19-3.

A PWM output (Figure 19-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 19-4: PWM OUTPUT



19.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

EQUATION 19-1:

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

PWM frequency is defined as 1/[PWM period].

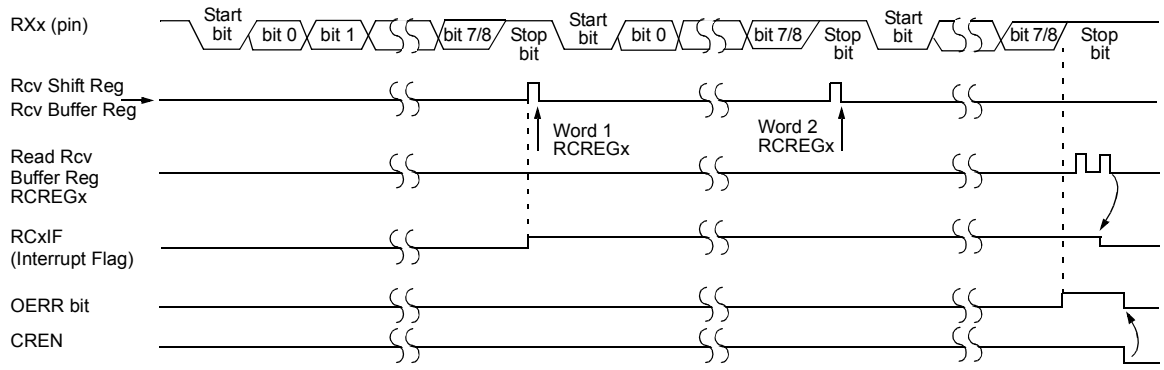
When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP4 pin is set

  (An exception: If PWM duty cycle = 0%, the CCP4 pin will not be set)
- The PWM duty cycle is latched from CCPR4L into CCPR4H

Note:	The Timer2 postscalers (see **Section 15.0 "Timer2 Module"**) are not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

FIGURE 22-7: ASYNCHRONOUS RECEPTION



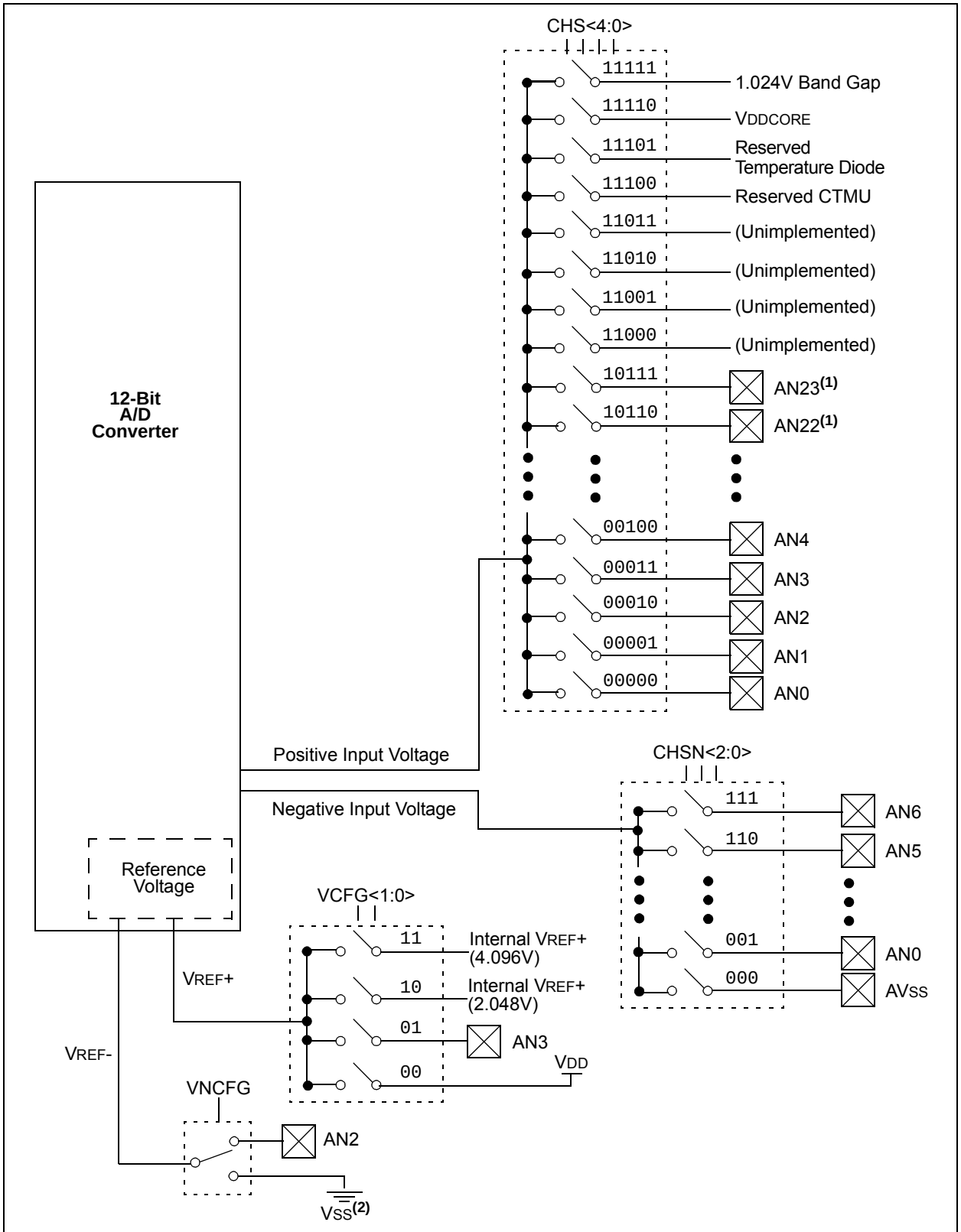
Note: This timing diagram shows three words appearing on the RXx input. The RCREGx (Receive Buffer) is read after the third word, causing the OERR (Overrun) bit to be set.

TABLE 22-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	TMR1GIF	TMR2IF	TMR1IF
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	TMR1GIE	TMR2IE	TMR1IE
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	TMR1GIP	TMR2IP	TMR1IP
PIR3	TMR5GIF	—	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF
PIE3	TMR5GIE	—	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE
IPR3	TMR5GIP	—	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	RTCCIP
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
RCREG1	EUSART1 Receive Register							
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
SPBRGH1	EUSART1 Baud Rate Generator Register High Byte							
SPBRG1	EUSART1 Baud Rate Generator Register							
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
RCREG2	EUSART2 Receive Register							
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCON2	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
SPBRGH2	EUSART2 Baud Rate Generator Register High Byte							
SPBRG2	EUSART2 Baud Rate Generator Register							
ODCON3	U2OD	U1OD	—	—	—	—	—	CTMUDS
PMD0	CCP3MD	CCP2MD	CCP1MD	UART2MD	UART1MD	SSP2MD	SSP1MD	ADCMD

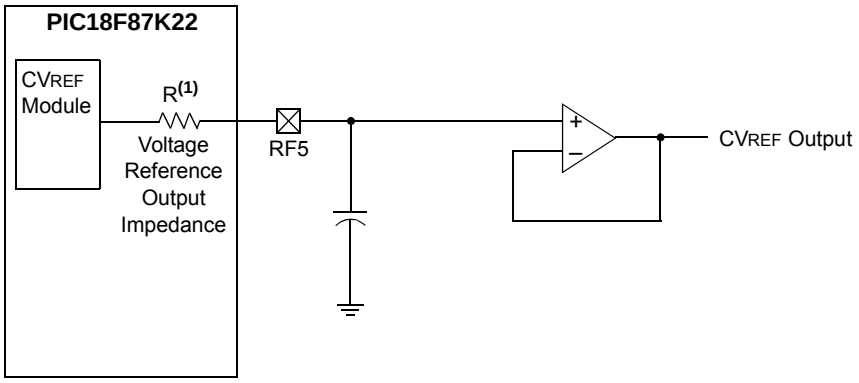
Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

FIGURE 23-4: A/D BLOCK DIAGRAM



Note 1: Channels, AN15 through AN12, and AN20 through AN23, are not available on 64-pin devices.
2: I/O pins have diode protection to VDD and VSS.

FIGURE 25-2: COMPARATOR VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



Note 1: R is dependent upon the Voltage Reference Configuration bits, CVRCON<3:0> and CVRCON<5>.

TABLE 25-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CVRCON	CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0
CM1CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0
CM2CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0
CM3CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
ANCON0	ANSEL7	ANSEL6	ANSEL5	ANSEL4	ANSEL3	ANSEL2	ANSEL1	ANSEL0
ANCON1	ANSEL15	ANSEL14	ANSEL13	ANSEL12	ANSEL11	ANSEL10	ANSEL9	ANSEL8

Legend: — = unimplemented, read as '0'. Shaded cells are not used with the comparator voltage reference.

EXAMPLE 27-4: ROUTINE FOR CAPACITIVE TOUCH SWITCH

```
#include "p18cxxx.h"

#define COUNT 500                       //@ 8MHz = 125uS.
#define DELAY for(i=0;i<COUNT;i++)
#define OPENSW 1000                     //Un-pressed switch value
#define TRIP 300                        //Difference between pressed
                                        //and un-pressed switch
#define HYST 65                         //amount to change
                                        //from pressed to un-pressed
#define PRESSED 1
#define UNPRESSED 0

int main(void)
{
    unsigned int Vread;                 //storage for reading
    unsigned int switchState;
    int i;

    //assume CTMU and A/D have been setup correctly
    //see Example 25-1 for CTMU & A/D setup
    setup();

    CTMUCONHbits.CTMUEN = 1;            //Enable the CTMU

    CTMUCONHbits.IDISSEN = 1;           //drain charge on the circuit
    DELAY;                              //wait 125us
    CTMUCONHbits.IDISSEN = 0;           //end drain of circuit

    CTMUCONLbits.EDG1STAT = 1;          //Begin charging the circuit
                                        //using CTMU current source
    DELAY;                              //wait for 125us
    CTMUCONLbits.EDG1STAT = 0;          //Stop charging circuit

    PIR1bits.ADIF = 0;                  //make sure A/D Int not set
    ADCON0bits.GO=1;                    //and begin A/D conv.
    while(!PIR1bits.ADIF);              //Wait for A/D convert complete

    Vread = ADRES;                      //Get the value from the A/D

    if(Vread < OPENSW - TRIP)
    {
        switchState = PRESSED;
    }
    else if(Vread > OPENSW - TRIP + HYST)
    {
        switchState = UNPRESSED;
    }
}
```

BCF **Bit Clear f**

Syntax: BCF f, b {,a}

Operands: $0 \le f \le 255$
$0 \le b \le 7$
$a \in [0,1]$

Operation: $0 \rightarrow f<b>$

Status Affected: None

Encoding:

1001	bbba	ffff	ffff

Description: Bit 'b' in register 'f' is cleared.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: `BCF FLAG_REG, 7, 0`

Before Instruction
FLAG_REG = C7h
After Instruction
FLAG_REG = 47h

BN **Branch if Negative**

Syntax: BN n

Operands: $-128 \le n \le 127$

Operation: if Negative bit is '1',
$(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding:

1110	0110	nnnn	nnnn

Description: If the Negative bit is '1', then the program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example:
```
HERE    BN   Jump
```
Before Instruction
PC = address (HERE)
After Instruction
If Negative = 1;
PC = address (Jump)
If Negative = 0;
PC = address (HERE + 2)

CALLW **Subroutine Call Using WREG**

Syntax: CALLW

Operands: None

Operation: (PC + 2) → TOS,
(W) → PCL,
(PCLATH) → PCH,
(PCLATU) → PCU

Status Affected: None

Encoding:

0000	0000	0001	0100

Description: First, the return address (PC + 2) is pushed onto the return stack. Next, the contents of W are written to PCL; the existing value is discarded. Then, the contents of PCLATH and PCLATU are latched into PCH and PCU, respectively. The second cycle is executed as a NOP instruction while the new next instruction is fetched.

Unlike CALL, there is no option to update W, STATUS or BSR.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read WREG	Push PC to stack	No operation
No operation	No operation	No operation	No operation

Example: HERE CALLW

Before Instruction
PC = address (HERE)
PCLATH = 10h
PCLATU = 00h
W = 06h
After Instruction
PC = 001006h
TOS = address (HERE + 2)
PCLATH = 10h
PCLATU = 00h
W = 06h

MOVSF **Move Indexed to f**

Syntax: MOVSF [z_s], f_d

Operands: $0 \le z_s \le 127$
$0 \le f_d \le 4095$

Operation: ((FSR2) + z_s) → f_d

Status Affected: None

Encoding:

1st word (source)	1110	1011	0zzz	$zzzz_s$
2nd word (destin.)	1111	ffff	ffff	$ffff_d$

Description: The contents of the source register are moved to destination register 'f_d'. The actual address of the source register is determined by adding the 7-bit literal offset 'z_s', in the first word, to the value of FSR2. The address of the destination register is specified by the 12-bit literal 'f_d' in the second word. Both addresses can be anywhere in the 4096-byte data space (000h to FFFh).

The MOVSF instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register.

If the resultant source address points to an Indirect Addressing register, the value returned will be 00h.

Words: 2

Cycles: 2

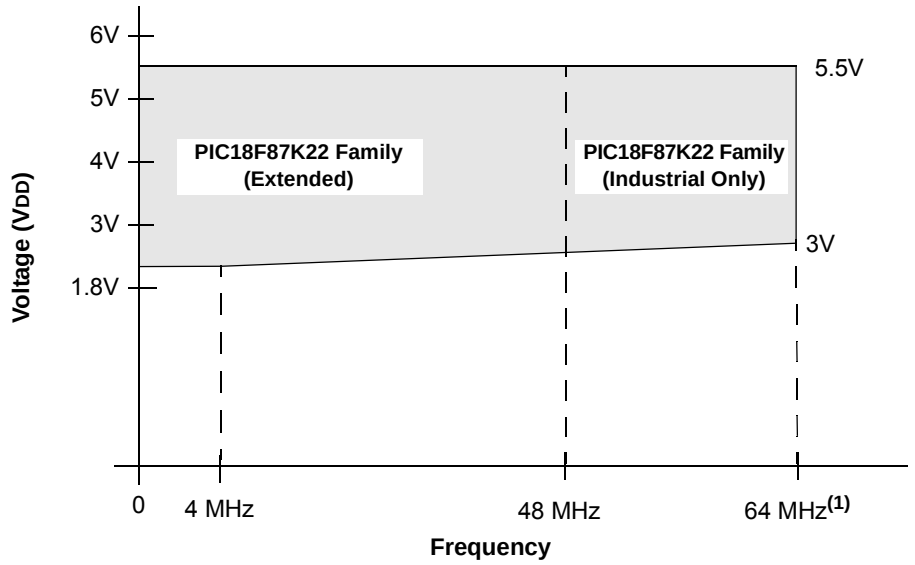
Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Determine source addr	Determine source addr	Read source reg
Decode	No operation No dummy read	No operation	Write register 'f' (dest)

Example: MOVSF [05h], REG2

Before Instruction
FSR2 = 80h
Contents of 85h = 33h
REG2 = 11h
After Instruction
FSR2 = 80h
Contents of 85h = 33h
REG2 = 33h

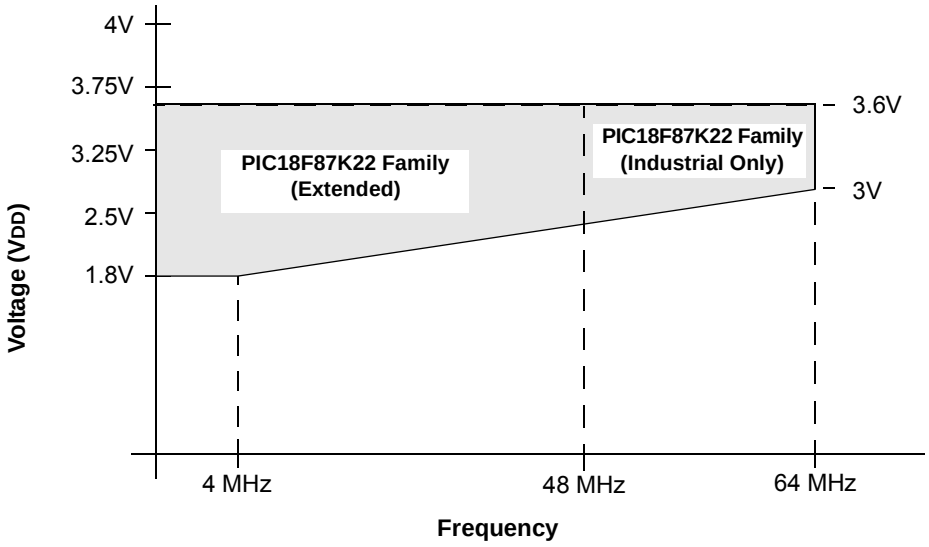
FIGURE 31-1: VOLTAGE-FREQUENCY GRAPH, REGULATOR ENABLED (INDUSTRIAL/EXTENDED)(1)



Note 1: FMAX = 25 MHz in 8-Bit External Memory mode. For VDD values, 1.8V to 3V, FMAX = (VDD – 1.72)/0.02 MHz.

2: FMAX = 64 MHz in all other modes. For VDD values, 1.8V to 3V, FMAX = (VDD – 1.72)/0.02 MHz.

FIGURE 31-2: VOLTAGE-FREQUENCY GRAPH, REGULATOR DISABLED (INDUSTRIAL/EXTENDED)(1,2)



Note 1: When the on-chip voltage regulator is disabled, VDD must be maintained so that VDD ≤ 3.6V.

2: For VDD values, 1.8V to 3V, FMAX = (VDD – 1.72)/0.02 MHz.

31.3 DC Characteristics: PIC18F87K22 Family (Industrial/Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**				
D080		I/O Ports:				
		PORTA, PORTB, PORTC	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +125°C
		PORTD, PORTE, PORTF, PORTG, PORTH, PORTJ	—	0.6	V	IOL = 3.5 mA, VDD = 4.5V, -40°C to +125°C
D083		OSC2/CLKO (EC modes)	—	0.6	V	IOL = 1.6 mA. VDD = 5.5V, -40°C to +125°C
	VOH	**Output High Voltage(1)**				
D090		I/O Ports:			V	
		PORTA, PORTB, PORTC	VDD – 0.7	—	V	IOH = -3 mA, VDD = 4.5V, -40°C to +125°C
		PORTD, PORTE, PORTF, PORTG, PORTH, PORTJ	VDD – 0.7	—	V	IOH = -2 mA, VDD = 4.5V, -40°C to +125°C
D092		OSC2/CLKO (INTOSC, EC modes)	VDD – 0.7	—	V	IOH = -1 mA, VDD = 5.5V, -40°C to +125°C
		Capacitive Loading Specs on Output Pins				
D100	COSC2	OSC2 Pin	—	20	pF	In HS mode when external clock is used to drive OSC1
D101	CIO	All I/O Pins and OSC2	—	50	pF	To meet the AC Timing Specifications
D102	CB	SCLx, SDAx	—	400	pF	I^2C™ Specification

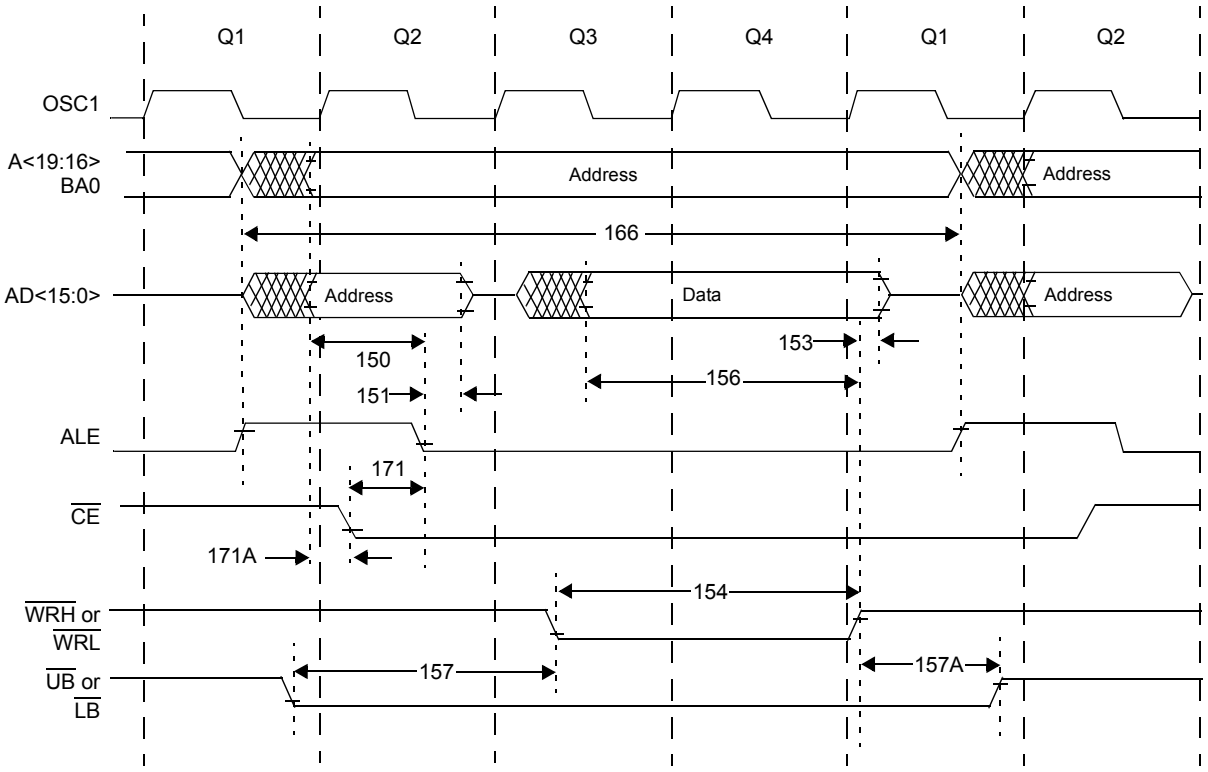
Note 1: Negative current is defined as current sourced by the pin.

31.4 DC Characteristics: CTMU Current Source Specifications

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	IOUT1	CTMU Current Source, Base Range	—	550	—	nA	CTMUICON<1:0> = 01
	IOUT2	CTMU Current Source, 10x Range	—	5.5	—	μA	CTMUICON<1:0> = 10
	IOUT3	CTMU Current Source, 100x Range	—	55	—	μA	CTMUICON<1:0> = 11

Note 1: Nominal value at center point of current trim range (CTMUICON<7:2> = 000000).

FIGURE 31-8: PROGRAM MEMORY WRITE TIMING DIAGRAM



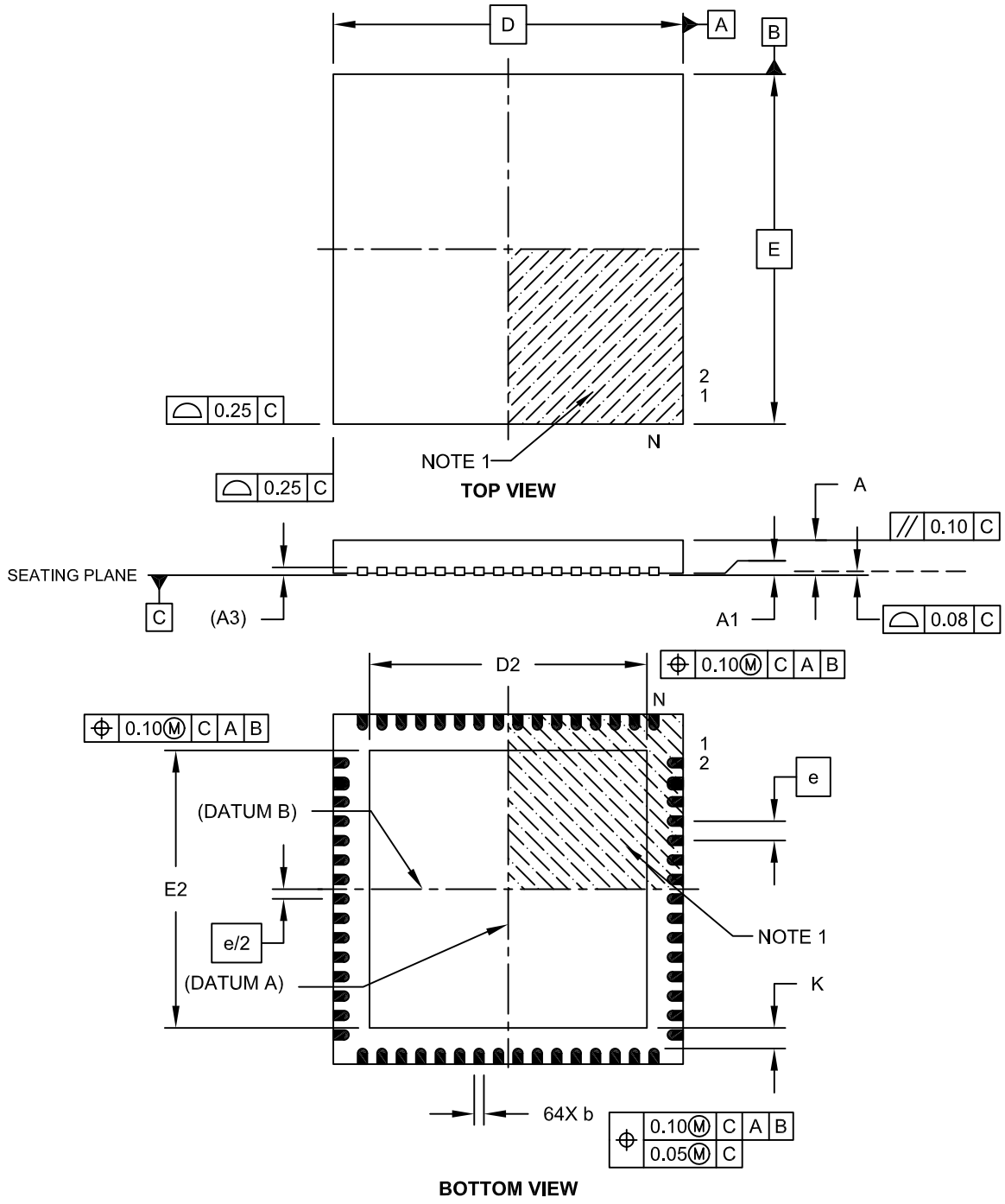
Operating Conditions: 2.0V < VCC < 3.6V, -40°C < TA < +125°C unless otherwise stated.

TABLE 31-12: PROGRAM MEMORY WRITE TIMING REQUIREMENTS

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2alL	Address Out Valid to ALE ↓ (address setup time)	0.25 TCY – 10	—	—	ns
151	TalL2adl	ALE ↓ to Address Out Invalid (address hold time)	5	—	—	ns
153	TwrH2adl	$\overline{WRn}$ ↑ to Data Out Invalid (data hold time)	5	—	—	ns
154	TwrL	$\overline{WRn}$ Pulse Width	0.5 TCY – 5	0.5 TCY	—	ns
156	TadV2wrH	Data Valid before $\overline{WRn}$ ↑ (data setup time)	0.5 TCY – 10	—	—	ns
157	TbsV2wrL	Byte Select Valid before $\overline{WRn}$ ↓ (byte select setup time)	0.25 TCY	—	—	ns
157A	TwrH2bsI	$\overline{WRn}$ ↑ to Byte Select Invalid (byte select hold time)	0.125 TCY – 5	—	—	ns
166	TalH2alH	ALE ↑ to ALE ↑ (cycle time)	—	TCY	—	ns
171	TalH2csL	Chip Enable Active to ALE ↓	0.25 TCY – 20	—	—	ns
171A	TubL2oeH	AD Valid to Chip Enable Active	—	—	10	ns

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149B Sheet 1 of 2

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