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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 64MHz |
| Connectivity | EBI/EMI, I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 69 |
| Program Memory Size | 32KB (16K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 24x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f85k22-i-pt |

### 1.1.6 EASY MIGRATION

All devices share the same rich set of peripherals except that the devices with 32 Kbytes of program memory (PIC18F65K22 and PIC18F85K22) have two less CCPs and three less timers. This provides a smooth migration path within the device family as applications evolve and grow.

The consistent pinout scheme, used throughout the entire family, also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 80-pin members, or even jumping from 64-pin to 80-pin devices.

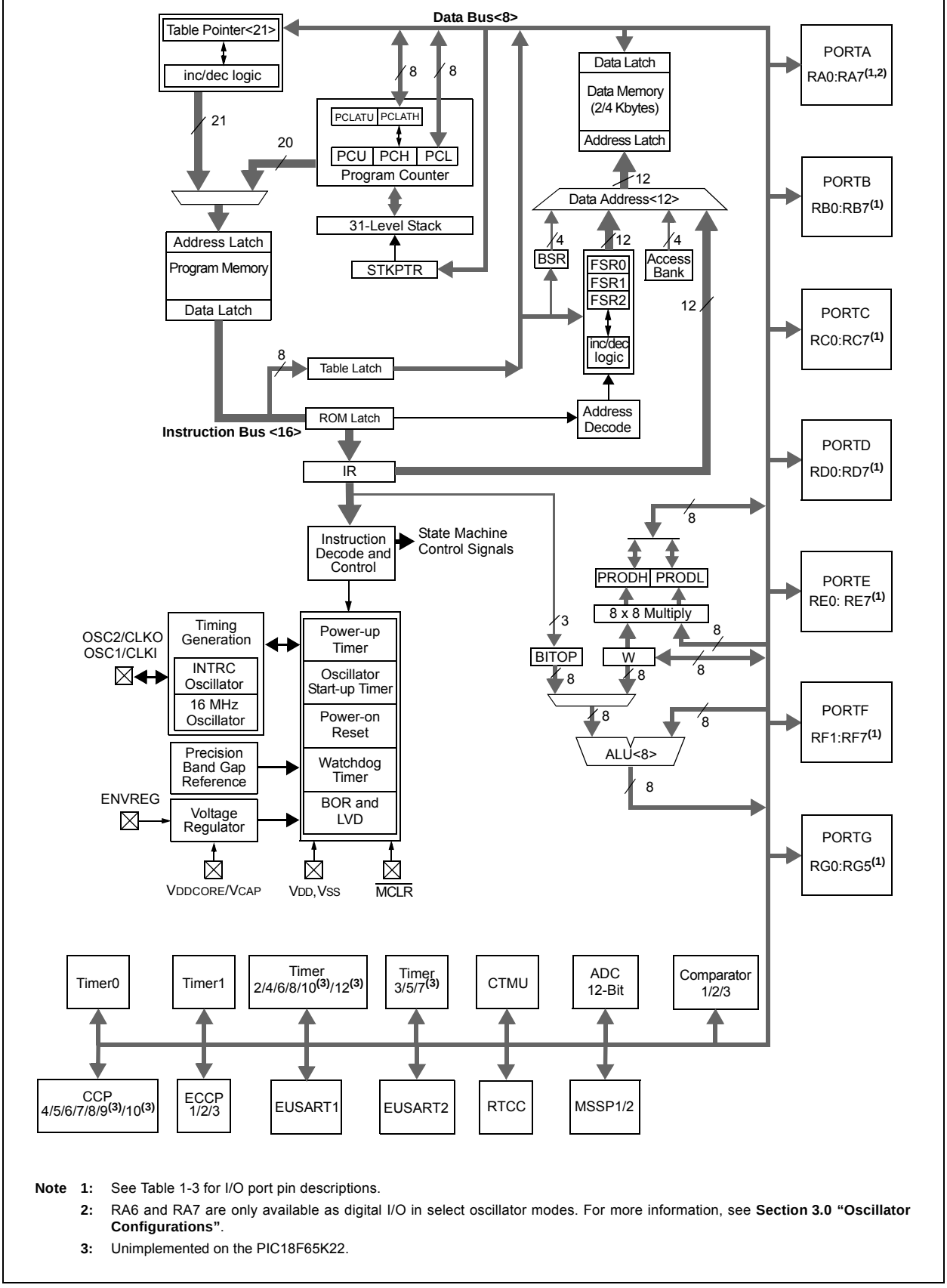
All of the devices in the family share the same rich set of peripherals, except for those with 32 Kbytes of program memory (PIC18F65K22 and PIC18F85K22). Those devices have two less CCPs and three less timers.

The PIC18F87K22 family is also largely pin compatible with other PIC18 families, such as the PIC18F8720 and PIC18F8722 and the PIC18F85J11. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining a similar feature set.

## 1.2 Other Special Features

- **Communications:** The PIC18F87K22 family incorporates a range of serial communication peripherals, including two Enhanced USARTs (EUSART) that support LIN/J2602, and two Master SSP modules, capable of both SPI and $I^2C$™ (Master and Slave) modes of operation.
- **CCP Modules:** PIC18F87K22 family devices incorporate up to seven Capture/Compare/PWM (CCP) modules. Up to six different time bases can be used to perform several different operations at once.
- **ECCP Modules:** The PIC18F87K22 family has three Enhanced CCP (ECCP) modules to maximize flexibility in control applications:
  - Up to eight different time bases for performing several different operations at once
  - Up to four PWM outputs for each module, for a total of 12 PWMs
  - Other beneficial features, such as polarity selection, programmable dead time, auto-shutdown and restart, and Half-Bridge and Full-Bridge Output modes
- **12-Bit A/D Converter:** The PIC18F87K22 family has differential ADC. It incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and thus, reducing code overhead.
- **Charge Time Measurement Unit (CTMU):** The CTMU is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation.
- Together with other on-chip analog modules, the CTMU can precisely measure time, measure capacitance or relative changes in capacitance, or generate output pulses that are independent of the system clock.
- **LP Watchdog Timer (WDT):** This enhanced version incorporates a 22-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 31.0 "Electrical Characteristics"** for time-out periods.
- **Real-Time Clock and Calendar Module (RTCC):** The RTCC module is intended for applications requiring that accurate time be maintained for extended periods of time with minimum to no intervention from the CPU.
- The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

**FIGURE 1-1: PIC18F6XK22 (64-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-3 for I/O port pin descriptions.

**2:** RA6 and RA7 are only available as digital I/O in select oscillator modes. For more information, see **Section 3.0 "Oscillator Configurations"**.

**3:** Unimplemented on the PIC18F65K22.

**TABLE 1-4: PIC18F8XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| RH7/CCP6/P1B/AN15 | 19 | | | |
| RH7 | | I/O | ST | Digital I/O. |
| CCP6(5) | | I/O | ST | Capture 6 input/Compare 6 output/PWM6 output. |
| P1B | | O | — | ECCP1 PWM Output B. |
| AN15 | | I | Analog | Analog Input 15. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); $I^2C$ = $I^2C$™/SMBus

**Note 1:** Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

**2:** Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

**3:** Not available on PIC18F65K22 and PIC18F85K22 devices.

**4:** PSP is available only in Microcontroller mode.

**5:** The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

**REGISTER 4-4: PMD0: PERIPHERAL MODULE DISABLE REGISTER 0**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CCP3MD | CCP2MD | CCP1MD | UART2MD | UART1MD | SSP2MD | SSP1MD | ADCMD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **CCP3MD:** PMD ECCP3 Enable/Disable bit
1 = Peripheral Module Disable (PMD) is enabled for ECCP3, disabling all of its clock sources
0 = PMD is disabled for ECCP3

bit 6 **CCP2MD:** PMD ECCP2 Enable/Disable bit
1 = PMD is enabled for ECCP2, disabling all of its clock sources
0 = PMD is disabled for ECCP2

bit 5 **CCP1MD:** PMD ECCP1 Enable/Disable bit
1 = PMD is enabled for ECCP1, disabling all of its clock sources
0 = PMD is disabled for ECCP1

bit 4 **UART2MD:** PMD UART2 Enable/Disable bit
1 = PMD is enabled for UART2, disabling all of its clock sources
0 = PMD is disabled for UART2

bit 3 **UART1MD:** PMD UART1 Enable/Disable bit
1 = PMD is enabled for UART1, disabling all of its clock sources
0 = PMD is disabled for UART1

bit 2 **SSP2MD:** PMD MSSP2 Enable/Disable bit
1 = PMD is enabled for MSSP2, disabling all of its clock sources
0 = PMD is disabled for MSSP2

bit 1 **SSP1MD:** PMD MSSP1 Enable/Disable bit
1 = PMD is enabled for MSSP1, disabling all of its clock sources
0 = PMD is disabled for MSSP1

bit 0 **ADCMD:** PMD Analog/Digital Converter PMD Enable/Disable bit
1 = PMD is enabled for the Analog/Digital Converter, disabling all of its clock sources
0 = PMD is disabled for the Analog/Digital Converter

## 4.7 Ultra Low-Power Wake-up

The Ultra Low-Power Wake-up (ULPWU) on pin, RA0, allows a slow falling voltage to generate an interrupt without excess current consumption.

To use this feature:

1. Charge the capacitor on RA0 by configuring the RA0 pin to an output and setting it to '1'.
2. Stop charging the capacitor by configuring RA0 as an input.
3. Discharge the capacitor by setting the ULPEN and ULPSINK bits in the WDTCON register.
4. Configure Sleep mode.
5. Enter Sleep mode.

When the voltage on RA0 drops below VIL, the device wakes up and executes the next instruction.

This feature provides a low-power technique for periodically waking up the device from Sleep mode.

The time-out is dependent on the discharge time of the RC circuit on RA0.

When the ULPWU module wakes the device from Sleep mode, the ULPLVL bit (WDTCON<5>) is set. Software can check this bit upon wake-up to determine the wake-up source.

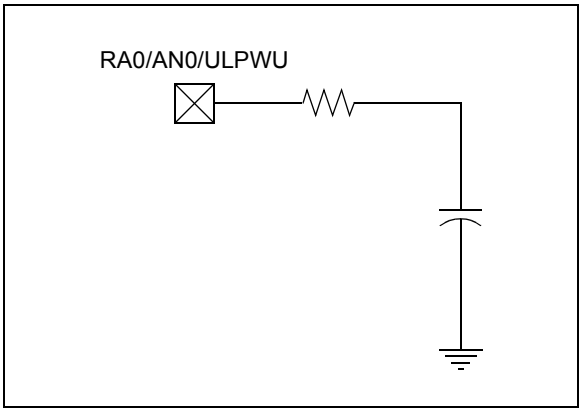
See Example 4-1 for initializing the ULPWU module.

**EXAMPLE 4-1: ULTRA LOW-POWER WAKE-UP INITIALIZATION**

```
            //**************************
            //Charge the capacitor on RA0
            //**************************
TRISAbits.TRISA0 = 0;
PORTAbits.RA0 = 1;
for(i = 0; i < 10000; i++) Nop();
            //*****************************
            //Stop Charging the capacitor
            //on RA0
            //*****************************
TRISAbits.TRISA0 = 1;
            //*****************************
            //Enable the Ultra Low Power
            //Wakeup module and allow
            //capacitor discharge
            //*****************************
WDTCONbits.ULPEN = 1;
WDTCONbits.ULPSINK = 1;
            //For Sleep
OSCCONbits.IDLEN = 0;
            //Enter Sleep Mode
            //
Sleep();
            //for sleep, execution will
            //resume here
```

A series resistor, between RA0 and the external capacitor, provides overcurrent protection for the RA0/AN0/ULPWU pin and enables software calibration of the time-out (see Figure 4-9).

**FIGURE 4-9: ULTRA LOW-POWER WAKE-UP INITIALIZATION**




A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired delay in Sleep. This technique compensates for the affects of temperature, voltage and component accuracy. The peripheral can also be configured as a simple Programmable Low-Voltage Detect (LVD) or temperature sensor.

**Note:** For more information, see *AN879, "Using the Microchip Ultra Low-Power Wake-up Module"* (DS00879).

## 8.8 Operation in Power-Managed Modes

In alternate, power-managed Run modes, the external bus continues to operate normally. If a clock source with a lower speed is selected, bus operations will run at that speed. In these cases, excessive access times for the external memory may result if Wait states have been enabled and added to external memory operations. If operations in a lower power Run mode are anticipated, users should provide in their applications for adjusting memory access times at the lower clock speeds.

In Sleep and Idle modes, the microcontroller core does not need to access data; bus operations are suspended. The state of the external bus is frozen, with the address/data pins, and most of the control pins, holding at the same state they were in when the mode was invoked. The only potential changes are to the $\overline{CE}$, $\overline{LB}$ and $\overline{UB}$ pins, which are held at logic high.

**TABLE 8-3: REGISTERS ASSOCIATED WITH THE EXTERNAL MEMORY BUS**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| MEMCON(1) | EBDIS | — | WAIT1 | WAIT0 | — | — | WM1 | WM0 |
| PADCFG1 | RDPU | REPU | RJPU(1) | — | — | RTSECSEL1 | RTSECSEL0 | — |
| PMD1 | PSPMD | CTMUMD | RTCCMD | TMR4MD | TMR3MD | TMR2MD | TMR1MD | EMBMD |

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used during External Memory Bus access.

**Note 1:** Unimplemented in 64-pin devices (PIC18F6XK22), read as '0'.

**EXAMPLE 9-1: DATA EEPROM READ**

```
        MOVLW   DATA_EE_ADDRH      ;
        MOVWF   EEADRH             ; Upper bits of Data Memory Address to read
        MOVLW   DATA_EE_ADDR       ;
        MOVWF   EEADR              ; Lower bits of Data Memory Address to read
        BCF     EECON1, EEPGD      ; Point to DATA memory
        BCF     EECON1, CFGS       ; Access EEPROM
        BSF     EECON1, RD         ; EEPROM Read
        NOP
        MOVF    EEDATA, W          ; W = EEDATA
```

**EXAMPLE 9-2: DATA EEPROM WRITE**

```
                MOVLW   DATA_EE_ADDRH      ;
                MOVWF   EEADRH             ; Upper bits of Data Memory Address to write
                MOVLW   DATA_EE_ADDR       ;
                MOVWF   EEADR              ; Lower bits of Data Memory Address to write
                MOVLW   DATA_EE_DATA       ;
                MOVWF   EEDATA             ; Data Memory Value to write
                BCF     EECON1, EEPGD      ; Point to DATA memory
                BCF     EECON1, CFGS       ; Access EEPROM
                BSF     EECON1, WREN       ; Enable writes

                BCF     INTCON, GIE        ; Disable Interrupts
                MOVLW   0x55               ;
Required        MOVWF   EECON2             ; Write 55h
Sequence        MOVLW   0xAA               ;
                MOVWF   EECON2             ; Write 0AAh
                BSF     EECON1, WR         ; Set WR bit to begin write
                BTFSC   EECON1, WR         ; Wait for write to complete GOTO $-2
                BSF     INTCON, GIE        ; Enable Interrupts

                                           ; User code execution
                BCF     EECON1, WREN       ; Disable writes on write complete (EEIF set)
```

## 13.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not directly readable or writable. Its value is set by the PSA and T0PS<2:0> bits (T0CON<3:0>), which determine the prescaler assignment and prescale ratio.

Clearing the PSA bit assigns the prescaler to the Timer0 module. When it is assigned, prescale values from 1:2 through 1:256, in power-of-two increments, are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (for example, `CLRF TMR0`, `MOVWF TMR0`, `BSF TMR0`) clear the prescaler count.

| **Note:** | Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count but will not change the prescaler assignment. |
|---|---|

### 13.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control and can be changed “on-the-fly” during program execution.

## 13.4 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or from FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF flag bit. The interrupt can be masked by clearing the TMR0IE bit (INTCON<5>). Before re-enabling the interrupt, the TMR0IF bit must be cleared in software by the Interrupt Service Routine (ISR).

Since Timer0 is shut down in Sleep mode, the TMR0 interrupt cannot awaken the processor from Sleep.

**TABLE 13-1: REGISTERS ASSOCIATED WITH TIMER0**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| TMR0L | Timer0 Register Low Byte | | | | | | | |
| TMR0H | Timer0 Register High Byte | | | | | | | |
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF |
| T0CON | TMR0ON | T08BIT | T0CS | T0SE | PSA | T0PS2 | T0PS1 | T0PS0 |

**Legend:** — = unimplemented, read as ‘0’. Shaded cells are not used by Timer0.

**TABLE 16-5: REGISTERS ASSOCIATED WITH TIMER3/5/7 AS A TIMER/COUNTER**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF |
| PIR5 | TMR7GIF(1) | TMR12IF(1) | TMR10IF(1) | TMR8IF | TMR7IF(1) | TMR6IF | TMR5IF | TMR4IF |
| IPR5 | TMR7GIP(1) | TMR12IP(1) | TMR10IP(1) | TMR8IP | TMR7IP(1) | TMR6IP | TMR5IP | TMR4IP |
| PIE5 | TMR7GIE(1) | TMR12IE(1) | TMR10IE(1) | TMR8IE | TMR7IE(1) | TMR6IE | TMR5IE | TMR4IE |
| PIE3 | TMR5GIE | — | RC2IE | TX2IE | CTMUIE | CCP2IE | CCP1IE | RTCCIE |
| IPR3 | TMR5GIP | — | RC2IP | TX2IP | CTMUIP | CCP2IP | CCP1IP | RTCCIP |
| PIR3 | TMR5GIF | — | RC2IF | TX2IF | CTMUIF | CCP2IF | CCP1IF | RTCCIF |
| PIE2 | OSCFIE | — | SSP2IE | BCL2IE | BCL1IE | HLVDIE | TMR3IE | TMR3GIE |
| PIR2 | OSCFIF | — | SSP2IF | BCL2IF | BCL1IF | HLVDIF | TMR3IF | TMR3GIF |
| IPR2 | OSCFIP | — | SSP2IP | BCL2IP | BCL1IP | HLVDIP | TMR3IP | TMR3GIP |
| TMR3H | Timer3 Register High Byte | | | | | | | |
| TMR3L | Timer3 Register Low Byte | | | | | | | |
| T3GCON | TMR3GE | T3GPOL | T3GTM | T3GSPM | T3GGO/$\overline{\text{T3DONE}}$ | T3GVAL | T3GSS1 | T3GSS0 |
| T3CON | TMR3CS1 | TMR3CS0 | T3CKPS1 | T3CKPS0 | SOSCEN | $\overline{\text{T3SYNC}}$ | RD16 | TMR3ON |
| TMR5H | Timer5 Register High Byte | | | | | | | |
| TMR5L | Timer5 Register Low Byte | | | | | | | |
| T5GCON | TMR5GE | T5GPOL | T5GTM | T5GSPM | T5GGO/$\overline{\text{T5DONE}}$ | T5GVAL | T5GSS1 | T5GSS0 |
| T5CON | TMR5CS1 | TMR5CS0 | T5CKPS1 | T5CKPS0 | SOSCEN | $\overline{\text{T5SYNC}}$ | RD16 | TMR5ON |
| TMR7H(1) | Timer7 Register High Byte | | | | | | | |
| TMR7L(1) | Timer7 Register Low Byte | | | | | | | |
| T7GCON(1) | TMR7GE | T7GPOL | T7GTM | T7GSPM | T7GGO/$\overline{\text{T7DONE}}$ | T7GVAL | T7GSS1 | T7GSS0 |
| T7CON(1) | TMR7CS1 | TMR7CS0 | T7CKPS1 | T7CKPS0 | SOSCEN | $\overline{\text{T7SYNC}}$ | RD16 | TMR7ON |
| OSCCON2 | — | SOSCRUN | — | — | SOSCGO | — | MFIOFS | MFIOSEL |
| PMD1 | PSPMD | CTMUMD | RTCCMD | TMR4MD | TMR3MD | TMR2MD | TMR1MD | EMBMD |
| PMD2 | TMR10MD(1) | TMR8MD | TMR7MD(1) | TMR6MD | TMR5MD | CMP3MD | CMP2MD | CMP2MD |

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used by the Timer3/5/7 module.

**Note 1:** Unimplemented on devices with a program memory of 32 Kbytes (PIC18FX5K22).

## 17.0 TIMER4/6/8/10/12 MODULES

The Timer4/6/8/10/12 timer modules have the following features:

- Eight-bit Timer register (TMRx)
- Eight-bit Period register (PRx)
- Readable and writable (all registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMRx match of PRx

Timer10 and Timer12 are unimplemented for devices with a program memory of 32 Kbytes (PIC18FX5K22).

**Note:** Throughout this section, generic references are used for register and bit names that are the same, except for an 'x' variable that indicates the item's association with the Timer4, Timer6, Timer8, Timer10 or Timer12 module. For example, the control register is named TxCON and refers to T4CON, T6CON, T8CON, T10CON and T12CON.

The Timer4/6/8/10/12 modules have a control register, which is shown in Register 17-1. Timer4/6/8/10/12 can be shut off by clearing control bit, TMRxON (TxCON<2>), to minimize power consumption. The prescaler and post-scaler selection of Timer4/6/8/10/12 are also controlled by this register. Figure 17-1 is a simplified block diagram of the Timer4/6/8/10/12 modules.

### 17.1 Timer4/6/8/10/12 Operation

Timer4/6/8/10/12 can be used as the PWM time base for the PWM mode of the ECCP modules. The TMRx registers are readable and writable, and are cleared on any device Reset. The input clock (FOSC/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits, TxCKPS<1:0> (TxCON<1:0>). The match output of TMRx goes through a four-bit postscaler (that gives a 1:1 to 1:16 inclusive scaling) to generate a TMRx interrupt, latched in the flag bit, TMRxIF. Table 17-1 shows each module's flag bit.

**TABLE 17-1: TIMER4/6/8/10/12 FLAG BITS**

| Timer Module | Flag Bit PIR5<x> | Timer Module | Flag Bit PIR5<x> |
|---|---|---|---|
| 4 | 0 | 10 | 5 |
| 6 | 2 | 12 | 6 |
| 8 | 4 | | |

The interrupt can be enabled or disabled by setting or clearing the Timerx Interrupt Enable bit (TMRxIE), shown in Table 17-2.

**TABLE 17-2: TIMER4/6/8/10/12 INTERRUPT ENABLE BITS**

| Timer Module | Flag Bit PIE5<x> | Timer Module | Flag Bit PIE5<x> |
|---|---|---|---|
| 4 | 0 | 10 | 5 |
| 6 | 2 | 12 | 6 |
| 8 | 4 | | |

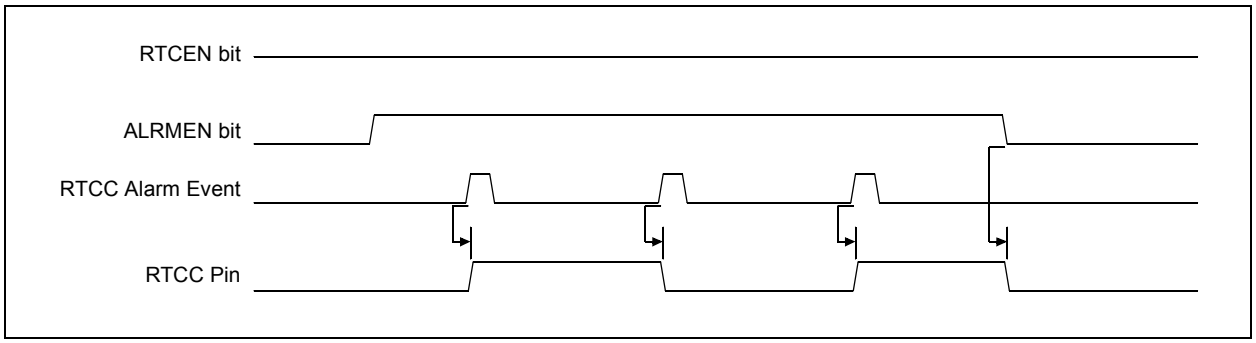
The prescaler and postscaler counters are cleared when any of the following occurs:

- A write to the TMRx register
- A write to the TxCON register
- Any device Reset – Power-on Reset (POR), MCLR Reset, Watchdog Timer Reset (WDTR) or Brown-out Reset (BOR)

A TMRx is not cleared when a TxCON is written.

**Note:** The CCP and ECCP modules use Timers, 1 through 8, for some modes. The assignment of a particular timer to a CCP/ECCP module is determined by the Timer to CCP enable bits in the CCPTMRSx registers. For more details, see Register 19-2, Register 19-3 and Register 20-2.

**FIGURE 18-6: TIMER PULSE GENERATION**




## 18.4 Sleep Mode

The timer and alarm continue to operate while in Sleep mode. The operation of the alarm is not affected by Sleep, as an alarm event can always wake up the CPU.

The Idle mode does not affect the operation of the timer or alarm.

## 18.5 Reset

### 18.5.1 DEVICE RESET

When a device Reset occurs, the ALRMRPT register is forced to its Reset state, causing the alarm to be disabled (if enabled prior to the Reset). If the RTCC was enabled, it will continue to operate when a basic device Reset occurs.

### 18.5.2 POWER-ON RESET (POR)

The RTCCFG and ALRMRPT registers are reset only on a POR. Once the device exits the POR state, the clock registers should be reloaded with the desired values.

The timer prescaler values can be reset only by writing to the SECONDS register. No device Reset can affect the prescalers.

## 22.4 EUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTAx<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the CKx pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

### 22.4.1 EUSART SYNCHRONOUS SLAVE TRANSMISSION

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep mode.

If two words are written to the TXREGx and then the SLEEP instruction is executed, the following will occur:

a) The first word will immediately transfer to the TSR register and transmit.
b) The second word will remain in the TXREGx register.
c) Flag bit, TXxIF, will not be set.
d) When the first word has been shifted out of TSR, the TXREGx register will transfer the second word to the TSR and flag bit, TXxIF, will now be set.
e) If enable bit, TXxIE, is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

1. Enable the synchronous slave serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
2. Clear bits, CREN and SREN.
3. If interrupts are desired, set enable bit, TXxIE.
4. If 9-bit transmission is desired, set bit, TX9.
5. Enable the transmission by setting enable bit, TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Start transmission by loading data to the TXREGx register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

**TABLE 22-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF |
| PIR1 | PSPIF | ADIF | RC1IF | TX1IF | SSP1IF | TMR1GIF | TMR2IF | TMR1IF |
| PIE1 | PSPIE | ADIE | RC1IE | TX1IE | SSP1IE | TMR1GIE | TMR2IE | TMR1IE |
| IPR1 | PSPIP | ADIP | RC1IP | TX1IP | SSP1IP | TMR1GIP | TMR2IP | TMR1IP |
| PIR3 | TMR5GIF | — | RC2IF | TX2IF | CTMUIF | CCP2IF | CCP1IF | RTCCIF |
| PIE3 | TMR5GIE | — | RC2IE | TX2IE | CTMUIE | CCP2IE | CCP1IE | RTCCIE |
| IPR3 | TMR5GIP | — | RC2IP | TX2IP | CTMUIP | CCP2IP | CCP1IP | RTCCIP |
| RCSTA1 | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D |
| TXREG1 | EUSART1 Transmit Register | | | | | | | |
| TXSTA1 | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D |
| BAUDCON1 | ABDOVF | RCIDL | RXDTP | TXCKP | BRG16 | — | WUE | ABDEN |
| SPBRGH1 | EUSART1 Baud Rate Generator Register High Byte | | | | | | | |
| SPBRG1 | EUSART1 Baud Rate Generator Register | | | | | | | |
| RCSTA2 | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D |
| TXREG2 | EUSART2 Transmit Register | | | | | | | |
| TXSTA2 | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D |
| BAUDCON2 | ABDOVF | RCIDL | RXDTP | TXCKP | BRG16 | — | WUE | ABDEN |
| SPBRGH2 | EUSART2 Baud Rate Generator Register High Byte | | | | | | | |
| SPBRG2 | EUSART2 Baud Rate Generator Register | | | | | | | |
| ODCON3 | U2OD | U1OD | — | — | — | — | — | CTMUDS |
| PMD0 | CCP3MD | CCP2MD | CCP1MD | UART2MD | UART1MD | SSP2MD | SSP1MD | ADCMD |

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

### 22.4.2 EUSART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical except in the case of Sleep, or any Idle mode, and bit, SREN, which is a “don’t care” in Slave mode.

If receive is enabled by setting the CREN bit prior to entering Sleep or any Idle mode, then a word may be received while in this low-power mode. Once the word is received, the RSR register will transfer the data to the RCREGx register. If the RCxIE enable bit is set, the interrupt generated will wake the chip from the low-power mode. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Reception:

1. Enable the synchronous master serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
2. If interrupts are desired, set enable bit, RCxIE.
3. If 9-bit reception is desired, set bit, RX9.
4. To enable reception, set enable bit, CREN.
5. Flag bit, RCxIF, will be set when reception is complete. An interrupt will be generated if enable bit, RCxIE, was set.
6. Read the RCSTAx register to get the 9th bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREGx register.
8. If any error occurred, clear the error by clearing bit, CREN.
9. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

**TABLE 22-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF |
| PIR1 | PSPIF | ADIF | RC1IF | TX1IF | SSP1IF | TMR1GIF | TMR2IF | TMR1IF |
| PIE1 | PSPIE | ADIE | RC1IE | TX1IE | SSP1IE | TMR1GIE | TMR2IE | TMR1IE |
| IPR1 | PSPIP | ADIP | RC1IP | TX1IP | SSP1IP | TMR1GIP | TMR2IP | TMR1IP |
| PIR3 | TMR5GIF | — | RC2IF | TX2IF | CTMUIF | CCP2IF | CCP1IF | RTCCIF |
| PIE3 | TMR5GIE | — | RC2IE | TX2IE | CTMUIE | CCP2IE | CCP1IE | RTCCIE |
| IPR3 | TMR5GIP | — | RC2IP | TX2IP | CTMUIP | CCP2IP | CCP1IP | RTCCIP |
| RCSTA1 | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D |
| RCREG1 | EUSART1 Receive Register | | | | | | | |
| TXSTA1 | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D |
| BAUDCON1 | ABDOVF | RCIDL | RXDTP | TXCKP | BRG16 | — | WUE | ABDEN |
| SPBRGH1 | EUSART1 Baud Rate Generator Register High Byte | | | | | | | |
| SPBRG1 | EUSART1 Baud Rate Generator Register | | | | | | | |
| RCSTA2 | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D |
| RCREG2 | EUSART2 Receive Register | | | | | | | |
| TXSTA2 | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D |
| BAUDCON2 | ABDOVF | RCIDL | RXDTP | TXCKP | BRG16 | — | WUE | ABDEN |
| SPBRGH2 | EUSART2 Baud Rate Generator Register High Byte | | | | | | | |
| SPBRG2 | EUSART2 Baud Rate Generator Register | | | | | | | |
| ODCON3 | U2OD | U1OD | — | — | — | — | — | CTMUDS |
| PMD0 | CCP3MD | CCP2MD | CCP1MD | UART2MD | UART1MD | SSP2MD | SSP1MD | ADCMD |

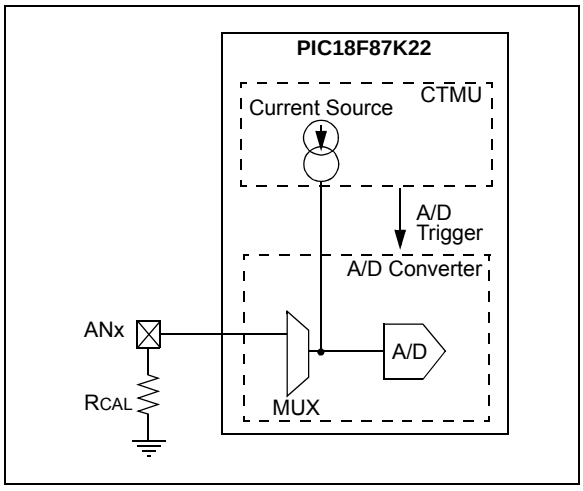
**Legend:** — = unimplemented, read as ‘0’. Shaded cells are not used for synchronous slave reception.

The CTMU current source may be trimmed with the trim bits in CTMUICON using an iterative process to get the exact current desired. Alternatively, the nominal value without adjustment may be used. That value may be stored by software for use in all subsequent capacitive or time measurements.

To calculate the value for RCAL, the nominal current must be chosen. Then, the resistance can be calculated.

For example, if the A/D Converter reference voltage is 3.3V, use 70% of full scale (or 2.31V) as the desired approximate voltage to be read by the A/D Converter. If the range of the CTMU current source is selected to be 0.55 μA, the resistor value needed is calculated as RCAL = 2.31V/0.55 μA, for a value of 4.2 MΩ. Similarly, if the current source is chosen to be 5.5 μA, RCAL would be 420,000Ω, and 42,000Ω if the current source is set to 55 μA.

**FIGURE 27-2: CTMU CURRENT SOURCE CALIBRATION CIRCUIT**




A value of 70% of full-scale voltage is chosen to make sure that the A/D Converter was in a range that is well above the noise floor. If an exact current is chosen to incorporate the trimming bits from CTMUICON, the resistor value of RCAL may need to be adjusted accordingly. RCAL may also be adjusted to allow for available resistor values. RCAL should be of the highest precision available, in light of the precision needed for the circuit that the CTMU will be measuring. A recommended minimum would be 0.1% tolerance.

The following examples show a typical method for performing a CTMU current calibration.

- Example 27-1 demonstrates how to initialize the A/D Converter and the CTMU.

  This routine is typical for applications using both modules.

- Example 27-2 demonstrates one method for the actual calibration routine.

  This method manually triggers the A/D Converter to demonstrate the entire step-wise process. It is also possible to automatically trigger the conversion by setting the CTMU's CTTRIG bit (CTMUCONH<0>).

**REGISTER 28-6: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)**

| R/P-1 | U-0 | U-0 | U-0 | R/P-1 | U-0 | R/P-1 | R/P-1 |
|---|---|---|---|---|---|---|---|
| MCLRE | — | — | — | MSSPMSK | — | ECCPMX(1) | CCP2MX |
| bit 7 | | | | | | | bit 0 |

| Legend: | P = Programmable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **MCLRE:** $\overline{\text{MCLR}}$ Pin Enable bit
1 = $\overline{\text{MCLR}}$ pin is enabled; RG5 input pin is disabled
0 = RG5 input pin is enabled; $\overline{\text{MCLR}}$ is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **MSSPMSK:** MSSP V3 7-Bit Address Masking Mode Enable bit
1 = 7-Bit Address Masking mode is enabled
0 = 5-Bit Address Masking mode is enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **ECCPMX:** ECCP MUX bit(1)
1 =
- ECCP1 (P1B/P1C) is multiplexed onto RE6 and RE5, CCP6 onto RE6, and CCP7 onto RE5
- ECCP3 (P3B/P3C) is multiplexed onto RE4 and RE3, CCP8 onto RE4, and CCP9 onto RE3

0 =
- ECCP1 (P1B/P1C) is multiplexed onto RH7 and RH6, CCP6 onto RH7, and CCP7(2) onto RH6
- ECCP3 (P3B/P3C) is multiplexed onto RH5 and RH4, CCP8 onto RH5, and CCP9(2) onto RH4

bit 0 **CCP2MX:** ECCP2 MUX bit
1 = ECCP2 is multiplexed with RC1
0 = ECCP2 is multiplexed with RB3 in Extended Microcontroller mode; ECCP2 is multiplexed with RE7 in Microcontroller mode

**Note 1:** Unimplemented on 64-pin devices (PIC18F6XK22), read as '0'.
**2:** Not implemented on 32K devices (PIC18F65K22 and PIC18F85K22).

**REGISTER 28-8: CONFIG5L: CONFIGURATION REGISTER 5 LOW (BYTE ADDRESS 300008h)**

| R/C-1 | R/C-1 | R/C-1 | R/C-1 | R/C-1 | R/C-1 | R/C-1 | R/C-1 |
|---|---|---|---|---|---|---|---|
| CP7(1) | CP6(1) | CP5(1) | CP4(1) | CP3 | CP2 | CP1 | CP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **CP7:** Code Protection bit(1)
1 = Block 7 is not code-protected(2)
0 = Block 7 is code-protected(2)

bit 6 **CP6:** Code Protection bit(1)
1 = Block 6 is not code-protected(2)
0 = Block 6 is code-protected(2)

bit 5 **CP5:** Code Protection bit(1)
1 = Block 5 is not code-protected(2)
0 = Block 5 is code-protected(2)

bit 4 **CP4:** Code Protection bit(1)
1 = Block 4 is not code-protected(2)
0 = Block 4 is code-protected(2)

bit 3 **CP3:** Code Protection bit
1 = Block 3 is not code-protected(2)
0 = Block 3 is code-protected(2)

bit 2 **CP2:** Code Protection bit
1 = Block 2 is not code-protected(2)
0 = Block 2 is code-protected(2)

bit 1 **CP1:** Code Protection bit
1 = Block 1 is not code-protected(2)
0 = Block 1 is code-protected(2)

bit 0 **CP0:** Code Protection bit
1 = Block 0 is not code-protected(2)
0 = Block 0 is code-protected(2)

**Note 1:** This bit is available only on PIC18F67K22 and PIC18F87K22 devices.
**2:** For the memory size of the blocks, see Figure 28-6.

**RRNCF** **Rotate Right f (No Carry)**

Syntax: RRNCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f<n>) → dest<n – 1>,
(f<0>) → dest<7>

Status Affected: N, Z

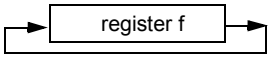
Encoding:

| | | | |
|---|---|---|---|
| 0100 | 00da | ffff | ffff |

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.




Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process Data | Write to destination |

Example 1:
```
RRNCF   REG, 1, 0
Before Instruction
    REG     =   1101 0111
After Instruction
    REG     =   1110 1011
```

Example 2:
```
RRNCF   REG, 0, 0
Before Instruction
    W       =   ?
    REG     =   1101 0111
After Instruction
    W       =   1110 1011
    REG     =   1101 0111
```

**SETF** **Set f**

Syntax: SETF f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: FFh → f

Status Affected: None

Encoding:

| | | | |
|---|---|---|---|
| 0110 | 100a | ffff | ffff |

Description: The contents of the specified register are set to FFh.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process Data | Write register 'f' |

Example:
```
SETF    REG,1
Before Instruction
    REG     =   5Ah
After Instruction
    REG     =   FFh
```

## 31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial/Extended) (Continued)

| PIC18F87K22 Family (Industrial/Extended) | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device** | **Typ** | **Max** | **Units** | **Conditions** | | |
| | **Supply Current (IDD) Cont.(2,3)** | | | | | | |
| | All devices | 2.1 | 5.5 | µA | -40°C | VDD = 1.8V(4) Regulator Disabled | FOSC = 31 kHz (**RC_IDLE** mode, LF-INTOSC) |
| | | 2.1 | 5.7 | µA | +25°C | | |
| | | 2.2 | 6.0 | µA | +85°C | | |
| | | 10 | 20 | µA | +125ºC | | |
| | All devices | 3.7 | 7.5 | µA | -40°C | VDD = 3.3V(4) Regulator Disabled | |
| | | 3.9 | 7.8 | µA | +25°C | | |
| | | 3.9 | 8.5 | µA | +85°C | | |
| | | 12 | 24 | µA | +125ºC | | |
| | All devices | 70 | 180 | µA | -40°C | VDD = 5V(5) Regulator Enabled | |
| | | 80 | 190 | µA | +25°C | | |
| | | 80 | 200 | µA | +85°C | | |
| | | 200 | 420 | µA | +125ºC | | |
| | All devices | 330 | 650 | µA | -40°C | VDD = 1.8V(4) Regulator Disabled | FOSC = 1 MHz (**RC_IDLE** mode, HF-INTOSC) |
| | | 330 | 640 | µA | +25°C | | |
| | | 330 | 630 | µA | +85°C | | |
| | | 500 | 850 | µA | +125ºC | | |
| | All devices | 520 | 850 | µA | -40°C | VDD = 3.3V(4) Regulator Disabled | |
| | | 520 | 900 | µA | +25°C | | |
| | | 520 | 850 | µA | +85°C | | |
| | | 800 | 1200 | µA | +125ºC | | |
| | All devices | 590 | 940 | µA | -40°C | VDD = 5V(5) Regulator Enabled | |
| | | 600 | 960 | µA | +25°C | | |
| | | 620 | 990 | µA | +85°C | | |
| | | 1000 | 1400 | µA | +125ºC | | |
| | All devices | 470 | 770 | µA | -40°C | VDD = 1.8V(4) Regulator Disabled | FOSC = 4 MHz (**RC_IDLE** mode, internal HF-INTOSC) |
| | | 470 | 770 | µA | +25°C | | |
| | | 460 | 760 | µA | +85°C | | |
| | | 700 | 1000 | µA | +125ºC | | |
| | All devices | 800 | 1400 | µA | -40°C | VDD = 3.3V(4) Regulator Disabled | |
| | | 800 | 1350 | µA | +25°C | | |
| | | 790 | 1300 | µA | +85°C | | |
| | | 1100 | 1400 | µA | +125ºC | | |
| | All devices | 880 | 1600 | µA | -40°C | VDD = 5V(5) Regulator Enabled | |
| | | 890 | 1700 | µA | +25°C | | |
| | | 910 | 1800 | µA | +85°C | | |
| | | 1200 | 2200 | µA | +125ºC | | |

**Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

**2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = External square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT enabled/disabled as specified.

**3:** Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

**4:** Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

**5:** Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

**6:** 48 MHz, maximum frequency at +125ºC.

## 31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial/Extended) (Continued)

| PIC18F87K22 Family (Industrial/Extended) | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Device** | **Typ** | **Max** | **Units** | **Conditions** | | |
| | **Module Differential Currents (ΔIWDT, ΔIBOR, ΔIHLVD, ΔIOSCB, ΔIAD)** | | | | | | |
| | **Watchdog Timer** | | | | | | |
| D022 (ΔIWDT) | All devices | 0.3 | 1 | µA | -40°C | VDD = 1.8V(4) Regulator Disabled | |
| | | 0.3 | 1 | µA | +25°C | | |
| D022 (ΔIWDT) | | 0.3 | 1 | µA | +85°C | | |
| | | 0.5 | 2 | µA | +125ºC | | |
| | All devices | 0.6 | 2 | µA | -40°C | VDD = 3.3V(4) Regulator Disabled | |
| | | 0.6 | 2 | µA | +25°C | | |
| | | 0.7 | 2 | µA | +85°C | | |
| | | 1 | 3 | µA | +125ºC | | |
| | All Devices | 0.6 | 2 | µA | -40°C | VDD = 5V(5) Regulator Enabled | |
| | | 0.6 | 2 | µA | +25°C | | |
| | | 0.7 | 2 | µA | +85°C | | |
| | | 1.5 | 4 | µA | +125ºC | | |
| D022A (ΔIBOR) (ΔIBOR) | **Brown-out Reset** | | | | | | |
| | All devices | 4.6 | 19 | µA | -40°C | VDD = 3.3V(4) Regulator Disabled | High-Power BOR |
| | | 4.5 | 20 | µA | +25°C | | |
| | | 4.7 | 20 | µA | +85°C | | |
| | | 18 | 40 | µA | +125ºC | | |
| | All devices | 4.2 | 20 | µA | -40°C | VDD = 5V(5) Regulator Enabled | High-Power BOR |
| | | 4.3 | 20 | µA | +25°C | | |
| | | 4.4 | 20 | µA | +85°C | | |
| | | 20 | 40 | µA | +125ºC | | |
| D022B (ΔIHLVD) | **High/Low-Voltage Detect** | | | | | | |
| | All devices | 3.8 | 9 | µA | -40°C | VDD = 1.8V(4) Regulator Disabled | |
| | | 4.2 | 9 | µA | +25°C | | |
| | | 4.3 | 10 | µA | +85°C | | |
| | | 4.5 | 12 | µA | +125ºC | | |
| | All devices | 4.5 | 11 | µA | -40°C | VDD = 3.3V(4) Regulator Disabled | |
| | | 4.8 | 12 | µA | +25°C | | |
| | | 4.8 | 12 | µA | +85°C | | |
| | | 5.0 | 14 | µA | +125ºC | | |
| | All devices | 4.9 | 13 | µA | -40°C | VDD = 5V(5) Regulator Enabled | |
| | | 4.9 | 13 | µA | +25°C | | |
| | | 4.9 | 13 | µA | +85°C | | |
| | | 5.3 | 15 | µA | +125ºC | | |

**Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

**2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = External square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

**3:** Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

**4:** Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{RETEN}$ (CONFIG1L<0>) = 1).

**5:** Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{RETEN}$ (CONFIG1L<0>) = 0).

**6:** 48 MHz, maximum frequency at +125ºC.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | |
|---|---|
| Device[1,2] | PIC18F65K22, PIC18F65K22T<br>PIC18F66K22, PIC18F66K22T<br>PIC18F67K22, PIC18F67K22T<br>PIC18F85K22, PIC18F85K22T<br>PIC18F86K22, PIC18F86K22T<br>PIC18F87K22, PIC18F87K22T |
| Temperature Range | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended) |
| Package | PT = TQFP (Plastic Thin Quad Flatpack)<br>MR = QFN (Plastic Quad Flat) |
| Pattern | QTP, SQTP, Code or Special Requirements (blank otherwise) |

**Examples:**

a) PIC18F87K22-I/PT 301 = Industrial temperature, TQFP package, QTP pattern #301.

b) PIC18F87K22T-I/PT = Tape and reel, Industrial temperature, TQFP package

c) PIC18F87K22T-E/PT = Tape and reel, Extended temperature, TQFP package

**Note 1:** F = Standard Voltage Range
**2:** T = In tape and reel PLCC and TQFP packages only
**3:** RSL = Silicon Revision A3