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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f85k22t-i-ptrsl

Peripheral Highlights:

- Up to Ten CCP/ECCP modules:
  - Up to seven Capture/Compare/PWM (CCP) modules
  - Three Enhanced Capture/Compare/PWM (ECCP) modules
- Up to Eleven 8/16-Bit Timer/Counter modules:
  - Timer0 – 8/16-bit timer/counter with 8-bit programmable prescaler
  - Timer1,3 – 16-bit timer/counter
  - Timer2,4,6,8 – 8-bit timer/counter
  - Timer5,7 – 16-bit timer/counter for 64k and 128k parts
  - Timer10,12 – 8-bit timer/counter for 64k and 128k parts
- Three Analog Comparators
- Configurable Reference Clock Output
- Hardware Real-Time Clock and Calendar (RTCC) module with Clock, Calendar and Alarm Functions
- Charge Time Measurement Unit (CTMU):
  - Capacitance measurement for mTouch™ sensing solution
  - Time measurement with 1 ns typical resolution
  - Integrated temperature sensor
- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Up to Four External Interrupts
- Two Master Synchronous Serial Port (MSSP) modules:
  - 3/4-wire SPI (supports all four SPI modes)
  - I^2C™ Master and Slave modes
- Two Enhanced Addressable USART modules:
  - LIN/J2602 support
  - Auto-Baud Detect (ABD)
- 12-Bit A/D Converter with up to 24 Channels:
  - Auto-acquisition and Sleep operation
  - Differential input mode of operation
- Integrated Voltage Reference

TABLE 1-3: PIC18F6XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	QFN/TQFP			
				PORTE is a bidirectional I/O port.
RE0/$\overline{RD}$/P2D	2			
RE0		I/O	ST	Digital I/O.
$\overline{RD}$		I	TTL	Parallel Slave Port read strobe.
P2D		O	—	EECP2 PWM Output D.
RE1/$\overline{WR}$/P2C	1			
RE1		I/O	ST	Digital I/O.
$\overline{WR}$		I	TTL	Parallel Slave Port write strobe.
P2C		O	—	ECCP2 PWM Output C.
RE2/$\overline{CS}$/P2B/CCP10	64			
RE2		I/O	ST	Digital I/O.
$\overline{CS}$		I	TTL	Parallel Slave Port chip select.
P2B		O	—	ECCP2 PWM Output B.
CCP10(3)		I/O	S/T	Capture 10 input/Compare 10 output/PWM10 output.
RE3/P3C/CCP9/REFO	63			
RE3		I/O	ST	Digital I/O.
P3C		O	—	ECCP3 PWM Output C.
CCP9(3,4)		I/O	S/T	Capture 9 input/Compare 9 output/PWM9 output.
REFO		O	—	Reference clock out.
RE4/P3B/CCP8	62			
RE4		I/O	ST	Digital I/O.
P3B		O	—	ECCP3 PWM Output B.
CCP8(4)		I/O	S/T	Capture 8 input/Compare 8 output/PWM8 output.
RE5/P1C/CCP7	61			
RE5		I/O	ST	Digital I/O.
P1C		O	—	ECCP1 PWM Output C.
CCP7(4)		I/O	S/T	Capture 7 input/Compare 7 output/PWM7 output.
RE6/P1B/CCP6	60			
RE6		I/O	ST	Digital I/O.
P1B		O	—	ECCP1 PWM Output B.
CCP6(4		I/O	S/T	Capture 6 input/Compare 6 output/PWM6 output.
RE7/ECCP2/P2A	59			
RE7		I/O	ST	Digital I/O.
ECCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A		O	—	ECCP2 PWM Output A.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C = I^2C™/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K22 and PIC18F85K22 devices.

4: The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

TABLE 1-4: PIC18F8XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RH7/CCP6/P1B/AN15	19			
RH7		I/O	ST	Digital I/O.
CCP6(5)		I/O	ST	Capture 6 input/Compare 6 output/PWM6 output.
P1B		O	—	ECCP1 PWM Output B.
AN15		I	Analog	Analog Input 15.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C = I^2C™/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K22 and PIC18F85K22 devices.

4: PSP is available only in Microcontroller mode.

5: The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
ODCON2	PIC18F66K22 PIC18F67K22	PIC18F86K22 PIC18F87K22	0000 0000	uuuu uuuu	uuuu uuuu
ODCON2	PIC18F65K22	PIC18F85K22	--00 0000	--uu uuuu	--uu uuuu
ODCON3	PIC18F6XK22	PIC18F8XK22	00-- ---0	uu-- ---u	uu-- ---u
MEMCON	PIC18F6XK22	PIC18F8XK22	0-00 --00	0-00 --00	u-uu --uu
ANCON0	PIC18F6XK22	PIC18F8XK22	1111 1111	uuuu uuuu	uuuu uuuu
ANCON1	PIC18F6XK22	PIC18F8XK22	1111 1111	uuuu uuuu	uuuu uuuu
ANCON2	PIC18F6XK22	PIC18F8XK22	1111 1111	uuuu uuuu	uuuu uuuu
RCSTA2	PIC18F6XK22	PIC18F8XK22	0000 000x	0000 000x	uuuu uuuu
TXSTA2	PIC18F6XK22	PIC18F8XK22	0000 0010	0000 0010	uuuu uuuu
BAUDCON2	PIC18F6XK22	PIC18F8XK22	0100 0-00	0100 0-00	uuuu u-uu
SPBRGH2	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
SPBRG2	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
RCREG2	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
TXREG2	PIC18F6XK22	PIC18F8XK22	xxxx xxxx	xxxx xxxx	uuuu uuuu
PSTR2CON	PIC18F6XK22	PIC18F8XK22	00-0 0001	00-0 0001	uu-u uuuu
PSTR3CON	PIC18F6XK22	PIC18F8XK22	00-0 0001	00-0 0001	uu-u uuuu
PMD0	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
PMD1	PIC18F6XK22	PIC18F8XK22	0000 0000	0000 0000	uuuu uuuu
PMD2	PIC18F66K22 PIC18F67K22	PIC18F86K22 PIC18F87K22	0000 0000	0000 0000	uuuu uuuu
PMD2	PIC18F65K22	PIC18F85K22	-0-0 0000	-0-0 0000	-u-u uuuu
PMD3	PIC18F66K22 PIC18F67K22	PIC18F86K22 PIC18F87K22	0000 0000	0000 0000	uuuu uuuu
PMD3	PIC18F65K22	PIC18F85K22	--00 000-	--00 000-	--uu uuu-

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.
Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for Reset value for specific condition.

6.0 MEMORY ORGANIZATION

PIC18F87K22 family devices have these types of memory:

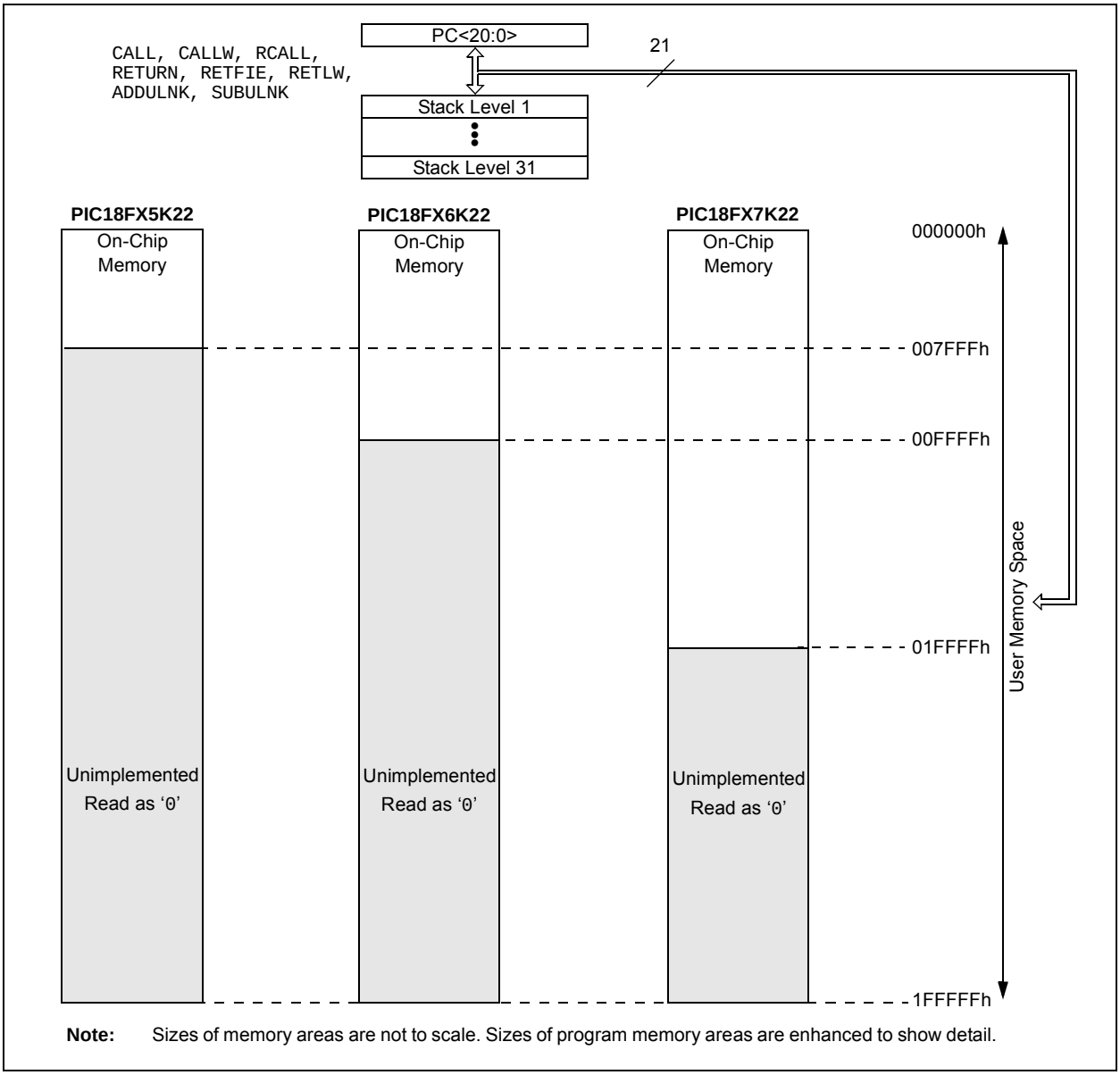
- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses. This enables concurrent access of the two memory spaces.

The data EEPROM, for practical purposes, can be regarded as a peripheral device because it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 7.0 "Flash Program Memory"**. The data EEPROM is discussed separately in **Section 9.0 "Data EEPROM Memory"**.

FIGURE 6-1: MEMORY MAPS FOR PIC18F87K22 FAMILY DEVICES



Note: Sizes of memory areas are not to scale. Sizes of program memory areas are enhanced to show detail.

8.8 Operation in Power-Managed Modes

In alternate, power-managed Run modes, the external bus continues to operate normally. If a clock source with a lower speed is selected, bus operations will run at that speed. In these cases, excessive access times for the external memory may result if Wait states have been enabled and added to external memory operations. If operations in a lower power Run mode are anticipated, users should provide in their applications for adjusting memory access times at the lower clock speeds.

In Sleep and Idle modes, the microcontroller core does not need to access data; bus operations are suspended. The state of the external bus is frozen, with the address/data pins, and most of the control pins, holding at the same state they were in when the mode was invoked. The only potential changes are to the $\overline{CE}$, $\overline{LB}$ and $\overline{UB}$ pins, which are held at logic high.

TABLE 8-3: REGISTERS ASSOCIATED WITH THE EXTERNAL MEMORY BUS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MEMCON(1)	EBDIS	—	WAIT1	WAIT0	—	—	WM1	WM0
PADCFG1	RDPU	REPU	RJPU(1)	—	—	RTSECSEL1	RTSECSEL0	—
PMD1	PSPMD	CTMUMD	RTCCMD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	EMBMD

Legend: — = unimplemented, read as '0'. Shaded cells are not used during External Memory Bus access.

Note 1: Unimplemented in 64-pin devices (PIC18F6XK22), read as '0'.

NOTES:

REGISTER 11-12: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0	U-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR5GIE	—	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR5GIE:** Timer5 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **RC2IE:** EUSART Receive Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 4 **TX2IE:** EUSART Transmit Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3 **CTMUIE:** CTMU Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **CCP2IE:** ECCP2 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **CCP1IE:** ECCP1 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **RTCCIE:** RTCC Interrupt Enable bit
1 = Enabled
0 = Disabled

REGISTER 11-13: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP10IE(1)	CCP9IE(1)	CCP8IE	CCP7IE	CCP6IE	CCP5IE	CCP4IE	CCP3IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **CCP<10:3>IE:** CCP<10:3> Interrupt Enable bits(1)
1 = Enabled
0 = Disabled

Note 1: Unimplemented on devices with a program memory of 32 Kbytes (PIC18FX5K22).

12.11 Parallel Slave Port

PORTD can function as an 8-bit-wide Parallel Slave Port (PSP), or microprocessor port, when control bit, PSPMODE (PSPCON<4>), is set. The port is asynchronously readable and writable by the external world through the $\overline{RD}$ control input pin (RE0/P2D/$\overline{RD}$/AD8) and $\overline{WR}$ control input pin (RE1/P2C/$\overline{WR}$/AD9).

Note:	The Parallel Slave Port is available only in Microcontroller mode.

The PSP can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an eight-bit latch.

Setting bit, PSPMODE, enables port pin, RE0/P2D/$\overline{RD}$/AD8, to be the $\overline{RD}$ input, RE1/P2C/$\overline{WR}$/AD9 to be the $\overline{WR}$ input and RE2/P2B/CCP10/$\overline{CS}$/AD10 to be the $\overline{CS}$ (Chip Select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (= 111).

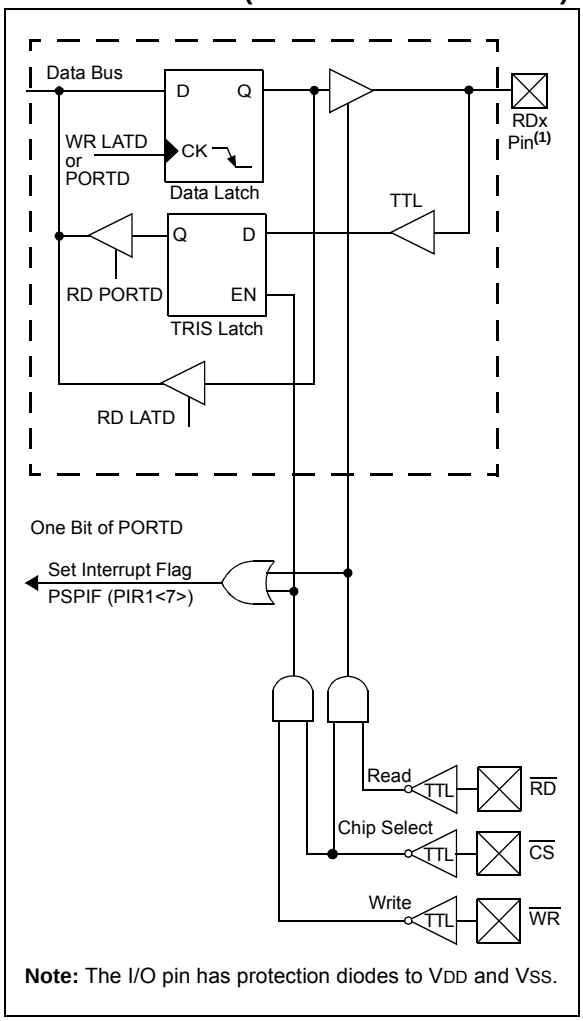
A write to the PSP occurs when both the $\overline{CS}$ and $\overline{WR}$ lines are first detected low and ends when either are detected high. The PSPIF and IBF flag bits (PIR1<7> and PSPCON<7>, respectively) are set when the write ends.

A read from the PSP occurs when both the $\overline{CS}$ and $\overline{RD}$ lines are first detected low. The data in PORTD is read out and the OBF bit (PSPCON<6>) is set. If the user writes new data to PORTD to set OBF, the data is immediately read out, but the OBF bit is not set.

When either the $\overline{CS}$ or $\overline{RD}$ line is detected high, the PORTD pins return to the input state and the PSPIF bit is set. User applications should wait for PSPIF to be set before servicing the PSP. When this happens, the IBF and OBF bits can be polled and the appropriate action taken.

The timing for the control signals in Write and Read modes is shown in Figure 12-4 and Figure 12-5, respectively.

FIGURE 12-3: PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE PORT)



Note: The I/O pin has protection diodes to VDD and VSS.

REGISTER 20-2: CCPTMRS0: CCP TIMER SELECT 0 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C3TSEL1	C3TSEL0	C2TSEL2	C2TSEL1	C2TSEL0	C1TSEL2	C1TSEL1	C1TSEL0
bit 7							bit 0

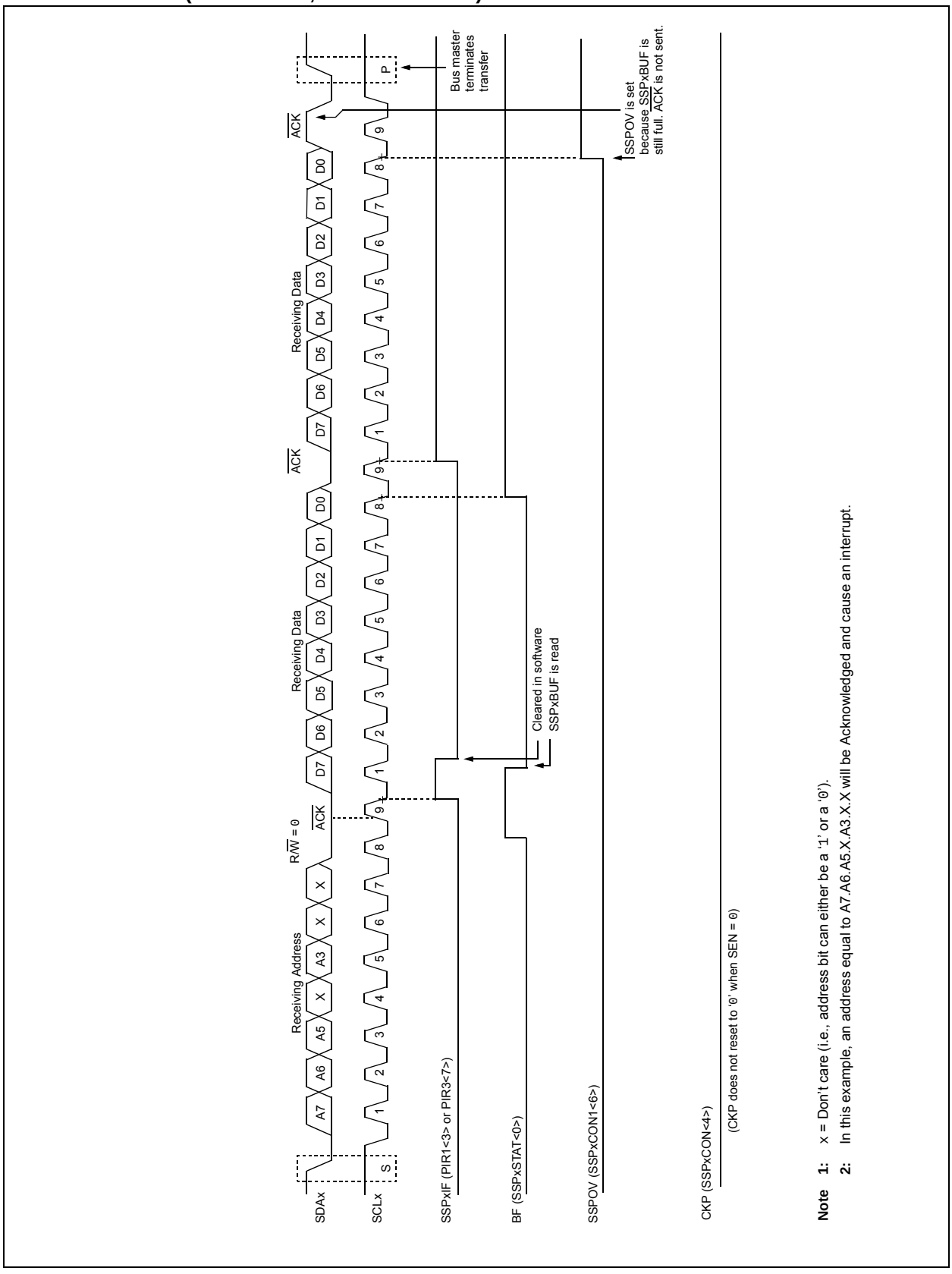
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **C3TSEL<1:0>:** ECCP3 Timer Selection bits
00 = ECCP3 is based off of TMR1/TMR2
01 = ECCP3 is based off of TMR3/TMR4
10 = ECCP3 is based off of TMR3/TMR6
11 = ECCP3 is based off of TMR3/TMR8

bit 5-3 **C2TSEL<2:0>:** ECCP2 Timer Selection bits
000 = ECCP2 is based off of TMR1/TMR2
001 = ECCP2 is based off of TMR3/TMR4
010 = ECCP2 is based off of TMR3/TMR6
011 = ECCP2 is based off of TMR3/TMR8
100 = ECCP2 is based off of TMR3/TMR10: option reserved on the 32-Kbyte device variant; do not use
101 = Reserved; do not use
110 = Reserved; do not use
111 = Reserved; do not use

bit 2-0 **C1TSEL<2:0>:** ECCP1 Timer Selection bits
000 = ECCP1 is based off of TMR1/TMR2
001 = ECCP1 is based off of TMR3/TMR4
010 = ECCP1 is based off of TMR3/TMR6
011 = ECCP1 is based off of TMR3/TMR8
100 = ECCP1 is based off of TMR3/TMR10: option reserved on the 32-Kbyte device variant; do not use
101 = ECCP1 is based off of TMR3/TMR12: option reserved on the 32-Kbyte device variant; do not use
110 = Reserved; do not use
111 = Reserved; do not use

FIGURE 21-9: I²C™ SLAVE MODE TIMING WITH SEN = 0 AND ADMSK<5:1> = 01011 (RECEPTION, 7-BIT ADDRESS)



Note 1: x = Don't care (i.e., address bit can either be a '1' or a '0').

2: In this example, an address equal to A7.A6.A5.X.A3.X.X will be Acknowledged and cause an interrupt.

REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

R-x	R-x	R-x	U-0	U-0	U-0	U-0	U-0
CMP3OUT	CMP2OUT	CMP1OUT	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **CMP<3:1>OUT:** Comparator x Status bits

If CPOL (CMxCON<5>)= 0 (non-inverted polarity):

1 = Comparator x's VIN+ > VIN-

0 = Comparator x's VIN+ < VIN-

If CPOL = 1 (inverted polarity):

1 = Comparator x's VIN+ < VIN-

0 = Comparator x's VIN+ > VIN-

bit 4-0 **Unimplemented:** Read as '0'

25.0 COMPARATOR VOLTAGE REFERENCE MODULE

The comparator voltage reference is a 32-tap resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it may also be used independently of them.

A block diagram of the module is shown in Figure 25-1. The resistor ladder is segmented to provide a range of CVREF values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference.

25.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRCON register (Register 25-1). The comparator voltage reference provides a range of output voltage with 32 levels.

The CVR<4:0> selection bits (CVRCON<4:0>) offer a range of output voltages. Equation 25-1 shows the how the comparator voltage reference is computed.

EQUATION 25-1:

If CVRSS = 1:

$$CV_{REF} = (V_{REF-}) + (CVR<4:0>/32) \bullet (V_{REF+} - V_{REF-})$$

If CVRSS = 0:

$$CV_{REF} = (AV_{SS}) + (CVR<4:0>/32) \bullet (AV_{DD} - AV_{SS})$$

The comparator reference supply voltage can come from either VDD and VSS, or the external VREF+ and VREF- that are multiplexed with RA3 and RA2. The voltage source is selected by the CVRSS bit (CVRCON<5>).

The settling time of the comparator voltage reference must be considered when changing the CVREF output (see Table 31-2 in **Section 31.0 "Electrical Characteristics"**).

REGISTER 25-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = CVREF circuit is powered on
0 = CVREF circuit is powered down

bit 6 **CVROE:** Comparator VREF Output Enable bit
1 = CVREF voltage level is output on CVREF pin
0 = CVREF voltage level is disconnected from CVREF pin

bit 5 **CVRSS:** Comparator VREF Source Selection bit
1 = Comparator reference source, CVRSRC = VREF+ – VREF-
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 4-0 **CVR<4:0>:** Comparator VREF Value Selection 0 ≤ CVR<4:0> ≤ 31 bits
When CVRSS = 1:
CVREF = (VREF-) + (CVR<4:0>/32) • (VREF+ – VREF-)
When CVRSS = 0:
CVREF = (AVSS) + (CVR<4:0>/32) • (AVDD – AVSS)

26.2 HLVD Setup

To set up the HLVD module:

1. Select the desired HLVD trip point by writing the value to the HLVDL<3:0> bits.
2. Set the VDIRMAG bit to detect high voltage (VDIRMAG = 1) or low voltage (VDIRMAG = 0).
3. Enable the HLVD module by setting the HLVDEN bit.
4. Clear the HLVD interrupt flag (PIR2<2>), which may have been set from a previous interrupt.
5. If interrupts are desired, enable the HLVD interrupt by setting the HLVDIE and GIE bits (PIE2<2> and INTCON<7>, respectively).

   An interrupt will not be generated until the IRVST bit is set.

Note:	Before changing any module settings (VDIRMAG, LVDL<3:0>), first disable the module (LVDEN = 0), make the changes and re-enable the module. This prevents the generation of false HLVD events.

26.3 Current Consumption

When the module is enabled, the HLVD comparator and voltage divider are enabled and consume static current. The total current consumption, when enabled, is specified in electrical specification Parameter D022B (Table 31-13).

Depending on the application, the HLVD module does not need to operate constantly. To reduce current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After such a check, the module could be disabled.

26.4 HLVD Start-up Time

The internal reference voltage of the HLVD module, specified in electrical specification Parameter 37 (**Section 31.0 "Electrical Characteristics"**), may be used by other internal circuitry, such as the programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification Parameter 37 (Table 31-13).

The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval (see Figure 26-2 or Figure 26-3).

27.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. By working with other on-chip analog modules, the CTMU can precisely measure time, capacitance and relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The module includes these key features:

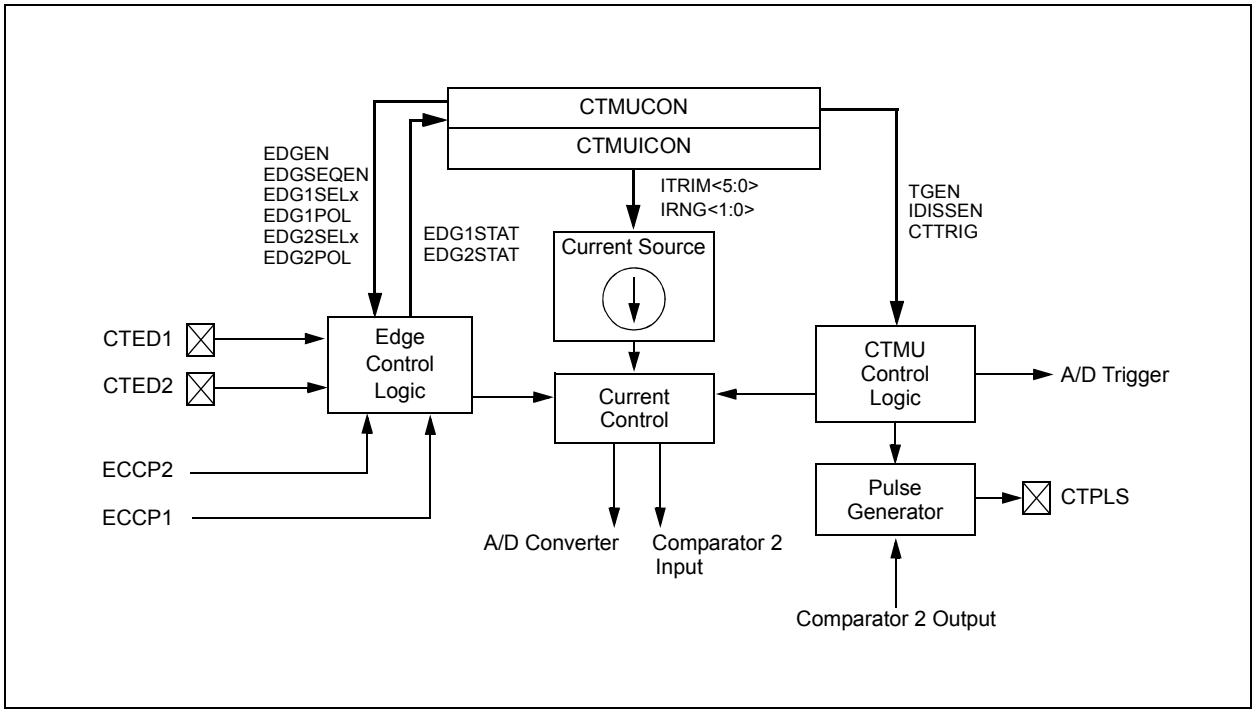
- Up to 24 channels available for capacitive or time measurement input
- On-chip precision current source
- Four-edge input trigger sources
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- Time measurement resolution of 1 nanosecond
- High-precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Accurate current source suitable for capacitive measurement

The CTMU works in conjunction with the A/D Converter to provide up to 24 channels for time or charge measurement, depending on the specific device and the number of A/D channels available. When configured for time delay, the CTMU is connected to one of the analog comparators. The level-sensitive input edge sources can be selected from four sources: two external inputs or the ECCP1/ECCP2 Special Event Triggers.

The CTMU special event can trigger the Analog-to-Digital Converter module.

Figure 27-1 provides a block diagram of the CTMU.

FIGURE 27-1: CTMU BLOCK DIAGRAM



REGISTER 28-4: CONFIG2H: CONFIGURATION REGISTER 2 HIGH (BYTE ADDRESS 300003h)

U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	WDTPS4	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN1	WDTEN0
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-2 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10101-11111 = Reserved
10100 = 1:1,048,576 (4,194.304s)
10011 = 1:524,288 (2,097.152s)
10010 = 1:262,144 (1,048.576s)
10001 = 1:131,072 (524.288s)
10000 = 1:65,536 (262.144s)
01111 = 1:32,768 (131.072s)
01110 = 1:16,384 (65.536s)
01101 = 1:8,192 (32.768s)
01100 = 1:4,096 (16.384s)
01011 = 1:2,048 (8.192s)
01010 = 1:1,024 (4.096s)
01001 = 1:512 (2.048s)
01000 = 1:256 (1.024s)
00111 = 1:128 (512 ms)
00110 = 1:64 (256 ms)
00101 = 1:32 (128 ms)
00100 = 1:16 (64 ms)
00011 = 1:8 (32 ms)
00010 = 1:4 (16 ms)
00001 = 1:2 (8 ms)
00000 = 1:1 (4 ms)

bit 1-0 **WDTEN<1:0>:** Watchdog Timer Enable bits

11 = WDT is enabled in hardware; SWDTEN bit is disabled
10 = WDT is controlled by the SWDTEN bit setting
01 = WDT is enabled only while the device is active and disabled in Sleep mode; SWDTEN bit is disabled
00 = WDT is disabled in hardware; SWDTEN bit is disabled

NOTES:

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial/Extended) (Continued)

PIC18F87K22 Family (Industrial/Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.(2,3)						
	All devices	3.7	8.5	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_RUN** mode, SOSCSEL = 01)
		5.4	10	µA	+25°C		
		6.6	13	µA	+85°C		
		13	30	µA	+125ºC		
	All devices	8.7	18	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		10	20	µA	+25°C		
		12	23	µA	+85°C		
		25	60	µA	+125ºC		
	All devices	60	160	µA	-40°C	VDD = 5V(4) Regulator Enabled	
		90	190	µA	+25°C		
		100	240	µA	+85°C		
		200	450	µA	+125ºC		
	All devices	1.2	4	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 32 kHz(3) (**SEC_IDLE** mode, SOSCSEL = 01)
		1.7	5	µA	+25°C		
		2.6	6	µA	+85°C		
		9	20	µA	+125ºC		
	All devices	1.6	7	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		2.8	9	µA	+25°C		
		4.1	10	µA	+85°C		
		17	40	µA	+125ºC		
	All devices	60	150	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		80	180	µA	+25°C		
		100	240	µA	+85°C		
		180	440	µA	+125ºC		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = External square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{RETEN}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{RETEN}$ (CONFIG1L<0>) = 0).

6: 48 MHz, maximum frequency at +125ºC.

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial/Extended) (Continued)

PIC18F87K22 Family (Industrial/Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Module Differential Currents (ΔIWDT, ΔIBOR, ΔIHLVD, ΔIOSCB, ΔIAD)						
	Watchdog Timer						
D022 (ΔIWDT)	All devices	0.3	1	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	
		0.3	1	µA	+25°C		
D022 (ΔIWDT)		0.3	1	µA	+85°C		
		0.5	2	µA	+125ºC		
	All devices	0.6	2	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		0.6	2	µA	+25°C		
		0.7	2	µA	+85°C		
		1	3	µA	+125ºC		
	All Devices	0.6	2	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		0.6	2	µA	+25°C		
		0.7	2	µA	+85°C		
		1.5	4	µA	+125ºC		
D022A (ΔIBOR) (ΔIBOR)	**Brown-out Reset**						
	All devices	4.6	19	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	High-Power BOR
		4.5	20	µA	+25°C		
		4.7	20	µA	+85°C		
		18	40	µA	+125ºC		
	All devices	4.2	20	µA	-40°C	VDD = 5V(5) Regulator Enabled	High-Power BOR
		4.3	20	µA	+25°C		
		4.4	20	µA	+85°C		
		20	40	µA	+125ºC		
D022B (ΔIHLVD)	**High/Low-Voltage Detect**						
	All devices	3.8	9	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	
		4.2	9	µA	+25°C		
		4.3	10	µA	+85°C		
		4.5	12	µA	+125ºC		
	All devices	4.5	11	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		4.8	12	µA	+25°C		
		4.8	12	µA	+85°C		
		5.0	14	µA	+125ºC		
	All devices	4.9	13	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		4.9	13	µA	+25°C		
		4.9	13	µA	+85°C		
		5.3	15	µA	+125ºC		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = External square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{RETEN}$ (CONFIG1L<0>) = 1).

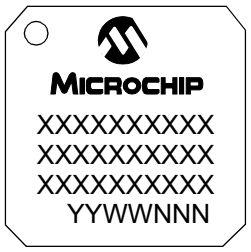
5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{RETEN}$ (CONFIG1L<0>) = 0).

6: 48 MHz, maximum frequency at +125ºC.

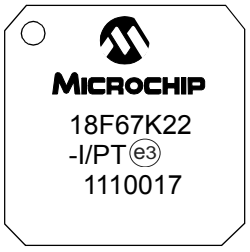
32.0 PACKAGING INFORMATION

32.1 Package Marking Information

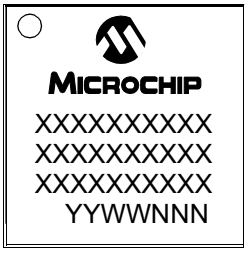
64-Lead TQFP



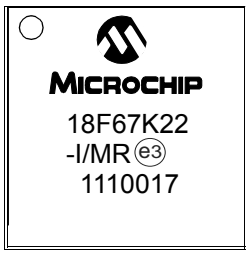
Example



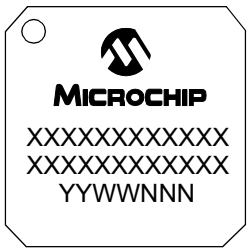
64-Lead QFN



Example



80-Lead TQFP



Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.