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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f86k22t-i-ptrsl

1.3 Details on Individual Family Members

Devices in the PIC18F87K22 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
  - PIC18FX5K22 (PIC18F65K22 and PIC18F85K22) – 32 Kbytes
  - PIC18FX6K22 (PIC18F66K22 and PIC18F86K22) – 64 Kbytes
  - PIC18FX7K22 (PIC18F67K22 and PIC18F87K22) – 128 Kbytes
- Data RAM:
  - All devices except PIC18FX5K22 – 4 Kbytes
  - PIC18FX5K22 – 2 Kbytes
- I/O Ports:
  - PIC18F6XK22 (64-pin devices) – 7 bidirectional ports
  - PIC18F8XK22 (80-pin devices) – 9 bidirectional ports
- CCP modules:
  - PIC18FX5K22 (PIC18F65K22 and PIC18F85K22) – 5 CCP modules
  - PIC18FX6K22 and PIC18FX7K22 (PIC18F66K22, PIC18F86K22, PIC18F67K22, and PIC18F87K22) – 7 CCP modules
- Timer modules:
  - PIC18FX5K22 (PIC18F65K22 and PIC18F85K22) – Four 8-bit timer/counters and four 16-bit timer/counters
  - PIC18FX6K22 and PIC18FX7K22 (PIC18F66K22, PIC18F86K22, PIC18F67K22, and PIC18F87K22) – Six 8-bit timer/counters and five 16-bit timer/counters
- A/D Channels:
  - PIC18F6XK22 (64-pin devices) – 24 channels
  - PIC18F8XK22 (80-pin devices) – 16 channels

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

TABLE 1-4: PIC18F8XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RH7/CCP6/P1B/AN15	19			
RH7		I/O	ST	Digital I/O.
CCP6(5)		I/O	ST	Capture 6 input/Compare 6 output/PWM6 output.
P1B		O	—	ECCP1 PWM Output B.
AN15		I	Analog	Analog Input 15.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C = I^2C™/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K22 and PIC18F85K22 devices.

4: PSP is available only in Microcontroller mode.

5: The CC6, CCP7, CCP8 and CCP9 pin placement depends on the setting of the ECCPMX Configuration bit (CONFIG3H<1>).

REGISTER 4-2: PMD2: PERIPHERAL MODULE DISABLE REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR10MD(1)	TMR8MD	TMR7MD(1)	TMR6MD	TMR5MD	CMP3MD	CMP2MD	CMP1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR10MD:** TMR10MD Disable bit(1)
1 = Peripheral Module Disable (PMD) is enabled and all TMR10MD clock sources are disabled
0 = PMD is disabled and TMR10MD is enabled

bit 6 **TMR8MD:** TMR8MD Disable bit
1 = PMD is enabled and all TMR8MD clock sources are disabled
0 = PMD is disabled and TMR8MD is enabled

bit 5 **TMR7MD:** TMR7MD Disable bit(1)
1 = PMD is enabled and all TMR7MD clock sources are disabled
0 = PMD is disabled and TMR7MD is enabled

bit 4 **TMR6MD:** TMR6MD Disable bit
1 = PMD is enabled and all TMR6MD clock sources are disabled
0 = PMD is disabled and TMR6MD is enabled

bit 3 **TMR5MD:** TMR5MD Disable bit
1 = PMD is enabled and all TMR5MD clock sources are disabled
0 = PMD is disabled and TMR5MD is enabled

bit 2 **CMP3MD:** PMD Comparator 3 Enable/Disable bit
1 = PMD is enabled for Comparator 3, disabling all of its clock sources
0 = PMD is disabled for Comparator 3

bit 1 **CMP2MD:** PMD Comparator 3 Enable/Disable bit
1 = PMD is enabled for Comparator 2, disabling all of its clock sources
0 = PMD is disabled for Comparator 2

bit 0 **CMP1MD:** PMD Comparator 3 Enable/Disable bit
1 = PMD is enabled for Comparator 1, disabling all of its clock sources
0 = PMD is disabled for Comparator 1

Note 1: Unimplemented on devices with a program memory of 32 Kbytes (PIC18FX5K22).

TABLE 6-2: PIC18F87K22 FAMILY REGISTER FILE SUMMARY (CONTINUED)

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
FB6h	PIE4	CCP10IE(3)	CCP9IE(3)	CCP8IE	CCP7IE	CCP6IE	CCP5IE	CCP4IE	CCP3IE	0000 0000
FB5h	CVRCON	CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0	0000 0000
FB4h	CMSTAT	CMP3OUT	CMP2OUT	CMP1OUT	—	—	—	—	—	xxx- ----
FB3h	TMR3H	Timer3 Register High Byte								xxxx xxxx
FB2h	TMR3L	Timer3 Register Low Byte								xxxx xxxx
FB1h	T3CON	TMR3CS1	TMR3CS0	T3CKPS1	T3CKPS0	SOSCEN	$\overline{\text{T3SYNC}}$	RD16	TMR3ON	0000 0000
FB0h	T3GCON	TMR3GE	T3GPOL	T3GTM	T3GSPM	$\frac{\text{T3GGO}}{\text{T3DONE}}$	T3GVAL	T3GSS1	T3GSS0	0000 0x00
FAFh	SPBRG1	USART1 Baud Rate Generator								0000 0000
FAEh	RCREG1	USART1 Receive Register								0000 0000
FADh	TXREG1	USART1 Transmit Register								xxxx xxxx
FACh	TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010
FABh	RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x
FAAh	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	$\frac{\text{T1GGO}}{\text{T1DONE}}$	T1GVAL	T1GSS1	T1GSS0	0000 0x00
FA9h	IPR6	—	—	—	EEIP	—	CMP3IP	CMP2IP	CMP1IP	---1 -111
FA8h	HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0000 0000
FA7h	PSPCON	IBF	OBF	IBOV	PSPMODE	—	—	—	—	0000 ----
FA6h	PIR6	—	—	—	EEIF	—	CMP3IF	CMP2IF	CMP1IF	---0 -000
FA5h	IPR3	TMR5GIP	—	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	RTCCIP	1-11 1111
FA4h	PIR3	TMR5GiF	—	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF	0-00 0000
FA3h	PIE3	TMR5GIE	—	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE	0-00 0000
FA2h	IPR2	OSCFIP	—	SSP2IP	BCL2IP	BCL1IP	HLVDIP	TMR3IP	TMR3GIP	1-11 1111
FA1h	PIR2	OSCFIF	—	SSP2IF	BCL2IF	BCL1IF	HLVDIF	TMR3IF	TMR3GIF	0-00 0000
FA0h	PIE2	OSCFIE	—	SSP2IE	BCL2IE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE	0-00 0000
F9Fh	IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	TMR1GIP	TMR2IP	TMR1IP	1111 1111
F9Eh	PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	TMR1GIF	TMR2IF	TMR1IF	0000 0000
F9Dh	PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	TMR1GIE	TMR2IE	TMR1IE	0000 0000
F9Ch	PSTR1CON	CMPL1	CMPL0	—	STRSYNC	STRD	STRC	STRB	STRA	00-0 0001
F9Bh	OSCTUNE	INTSRC	PLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000 0000
F9Ah	TRISJ(2)	TRISJ7	TRISJ6	TRISJ5	TRISJ4	TRISJ3	TRISJ2	TRISJ1	TRISJ0	1111 1111
F99h	TRISH(2)	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	1111 1111
F98h	TRISG	—	—	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	---1 1111
F97h	TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—	1111 111-
F96h	TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	—	1111 111-
F95h	TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111
F94h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111
F93h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111
F92h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111
F91h	LATJ(2)	LATJ7	LATJ6	LATJ5	LATJ4	LATJ3	LATJ2	LATJ1	LATJ0	xxxx xxxx
F90h	LATH(2)	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	xxxx xxxx
F8Fh	LATG	—	—	—	LATG4	LATG3	LATG2	LATG1	LATG0	---x xxxx
F8Eh	LATF	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	—	xxxx xxx-
F8Dh	LATE	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx xxxx
F8Ch	LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx xxxx
F8Bh	LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx xxxx
F8Ah	LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx xxxx
F89h	LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx xxxx
F88h	PORTJ(2)	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	xxxx xxxx
F87h	PORTH(2)	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	xxxx xxxx

Note 1: This bit is available when Master Clear is disabled (MCLRE = 0). When MCLRE is set, the bit is unimplemented.
2: Unimplemented on 64-pin devices (PIC18F6XK22), read as '0'.
3: Unimplemented on devices with a program memory of 32 Kbytes (PIC18FX5K22).

8.6.2 16-BIT WORD WRITE MODE

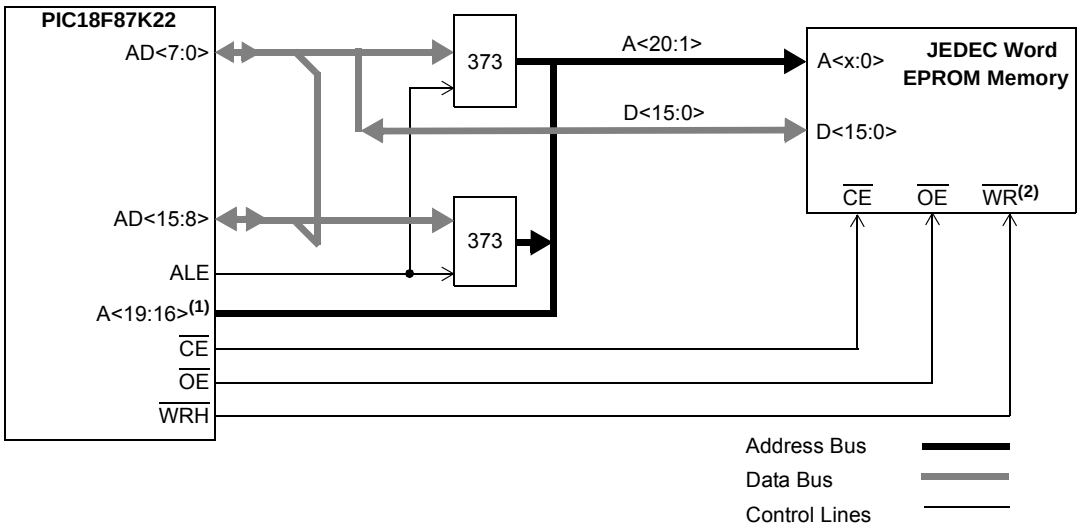
Figure 8-2 shows an example of 16-Bit Word Write mode for PIC18F87K22 family devices. This mode is used for word-wide memories, which includes some of the EPROM and Flash type memories. This mode allows opcode fetches and table reads from all forms of 16-bit memory, and table writes to any type of word-wide external memories. This method makes a distinction between TBLWT cycles to even or odd addresses.

During a TBLWT cycle to an even address (TBLPTR<0> = 0), the TABLAT data is transferred to a holding latch and the external address data bus is tri-stated for the data portion of the bus cycle. No write signals are activated.

During a TBLWT cycle to an odd address (TBLPTR<0> = 1), the TABLAT data is presented on the upper byte of the AD<15:0> bus. The contents of the holding latch are presented on the lower byte of the AD<15:0> bus.

The $\overline{WRH}$ signal is strobed for each write cycle; the $\overline{WRL}$ pin is unused. The signal on the BA0 pin indicates the LSb of the TBLPTR, but it is left unconnected. Instead, the $\overline{UB}$ and $\overline{LB}$ signals are active to select both bytes. The obvious limitation to this method is that the table write must be done in pairs on a specific word boundary to correctly write a word location.

FIGURE 8-2: 16-BIT WORD WRITE MODE EXAMPLE



Note 1: Upper order address lines are used only for 20-bit address widths.

2: This signal only applies to table writes. See **Section 7.1 "Table Reads and Table Writes"**.

REGISTER 11-15: PIE6: PERIPHERAL INTERRUPT ENABLE REGISTER 6

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	EEIE	—	CMP3IE	CMP2IE	CMP1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **EEIE:** Data EEDATA/Flash Write Operation Enable bit
1 = Interrupt is enabled
0 = interrupt is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2 **CMP3IE:** CMP3 Enable bit
1 = Interrupt is enabled
0 = interrupt is disabled

bit 1 **CMP2E:** CMP2 Enable bit
1 = Interrupt is enabled
0 = interrupt is disabled

bit 0 **CMP1IE:** CMP1 Enable bit
1 = Interrupt is enabled
0 = interrupt is disabled

TABLE 12-9: PORTE FUNCTIONS (CONTINUED)

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RE7/ECCP2/ P2A/AD15	RE7	0	O	DIG	LATE<7> data output.
		1	I	ST	PORTE<7> data input.
	ECCP2(1)	0	O	DIG	ECCP2 compare/PWM output; takes priority over port data.
		1	I	ST	ECCP2 capture input.
	P2A	0	O	—	ECCP2 PWM Output A. May be configured for tri-state during Enhanced PWM shutdown event.
	AD15(2)	x	O	DIG	External memory interface, Address/Data Bit 15 output.
		x	I	TTL	External memory interface, Data Bit 15 input.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared and in Microcontroller mode.

2: This feature is only available on PIC18F8XKXX devices.

TABLE 12-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0
LATE	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0
TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0
PADCFG1	RDPU	REPU	RJPU(2)	—	—	RTSECSEL1	RTSECSEL0	—
ODCON1	SSP1OD	CCP2OD	CCP1OD	—	—	—	—	SSP2OD
ODCON2	CCP10OD(1)	CCP9OD(1)	CCP8OD	CCP7OD	CCP6OD	CCP5OD	CCP4OD	CCP3OD

Legend: Shaded cells are not used by PORTE.

Note 1: Unimplemented on PIC18FX5K22 devices, read as '0'.

2: Unimplemented on 64-pin devices (PIC18F6XK22), read as '0'.

12.7 PORTF, LATF and TRISF Registers

PORTF is a 7-bit wide, bidirectional port. The corresponding Data Direction and Output Latch registers are TRISF and LATF. All pins on PORTF are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Pins, RF1 through RF6, may be used as comparator inputs or outputs by setting the appropriate bits in the CMCON register. To use RF<7:1> as digital inputs, it is also necessary to turn off the comparators.

Note 1: On device Resets, pins, RF<7:1>, are configured as analog inputs and are read as '0'.

2: To configure PORTF as a digital I/O, turn off the comparators and clear ANCON1 and ANCON2 to digital.

EXAMPLE 12-6: INITIALIZING PORTF

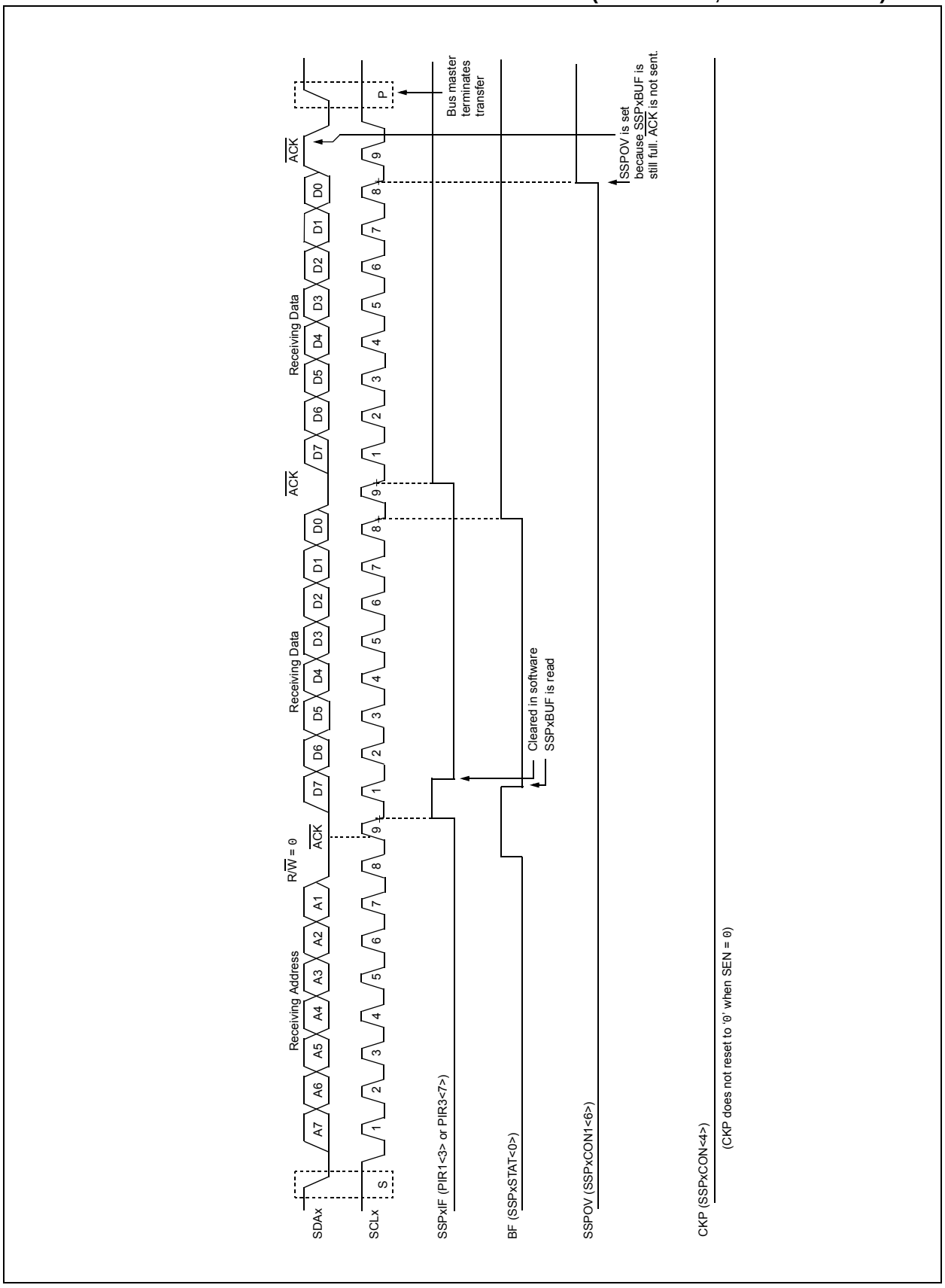
```
CLRF     PORTF    ; Initialize PORTF by
                  ; clearing output
                  ; data latches
CLRF     LATF     ; Alternate method
                  ; to clear output
                  ; data latches
BANKSEL  ANCON1   ; Select bank with ANCON1 register
MOVLW    1Fh      ; Make AN6, AN7 and AN5 digital
MOVWF    ANCON1   ;
MOVLW    0Fh      ; Make AN8, AN9, AN10 and AN11
                    digital
MOVWF    ANCON    ; Set PORTF as digital I/O
BANKSEL  TRISF    ; Select bank with TRISF register
MOVLW    0CEh     ; Value used to
                  ; initialize data
                  ; direction
MOVWF    TRISF    ; Set RF3:RF1 as inputs
                  ; RF5:RF4 as outputs
                  ; RF7:RF6 as inputs
```

TABLE 12-11: PORTF FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RF1/AN6/C2OUT/ CTDIN	RF1	0	O	DIG	LATF<1> data output; not affected by analog input.
		1	I	ST	PORTF<1> data input; disabled when analog input is enabled.
	AN6	1	I	ANA	A/D Input Channel 6. Default configuration on POR.
	C2OUT	0	O	DIG	Comparator 2 output; takes priority over port data.
	CTDIN	1	I	ST	CTMU pulse delay input.
RF2/AN7/C1OUT	RF2	0	O	DIG	LATF<2> data output; not affected by analog input.
		1	I	ST	PORTF<2> data input; disabled when analog input is enabled.
	AN7	1	I	ANA	A/D Input Channel 7. Default configuration on POR.
	C1OUT	0	O	DIG	Comparator 1 output; takes priority over port data.
RF3/AN8/C2INB/ CTMUI	RF3	0	O	DIG	LATF<3> data output; not affected by analog input.
		1	I	ST	PORTF<3> data input; disabled when analog input is enabled.
	AN8	1	I	ANA	A/D Input Channel 8 and Comparator C2+ input. Default input configuration on POR; not affected by analog output.
	C2INB	1	I	ANA	Comparator 2 Input B.
	CTMUI	x	O	—	CTMU pulse generator charger for the C2INB comparator input.
RF4/AN9/C2INA	RF4	0	O	DIG	LATF<4> data output; not affected by analog input.
		1	I	ST	PORTF<4> data input; disabled when analog input is enabled.
	AN9	1	I	ANA	A/D Input Channel 9 and Comparator C2- input. Default input configuration on POR; does not affect digital output.
	C2INA	1	I	ANA	Comparator 2 Input A.
RF5/AN10/CVREF/ C1INB	RF5	0	O	DIG	LATF<5> data output; not affected by analog input. Disabled when CVREF output is enabled.
		1	I	ST	PORTF<5> data input; disabled when analog input is enabled. Disabled when CVREF output is enabled.
	AN10	1	I	ANA	A/D Input Channel 10 and Comparator C1+ input. Default input configuration on POR.
	CVREF	x	O	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
	C1INB	1	I	ANA	Comparator 1 Input B.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

FIGURE 21-8: I²C™ SLAVE MODE TIMING WITH SEN = 0 (RECEPTION, 7-BIT ADDRESS)



21.4.4 CLOCK STRETCHING

Both 7-Bit and 10-Bit Slave modes implement automatic clock stretching during a transmit sequence.

The SEN bit (SSPxCON2<0>) allows clock stretching to be enabled during receives. Setting SEN will cause the SCLx pin to be held low at the end of each data receive sequence.

21.4.4.1 Clock Stretching for 7-Bit Slave Receive Mode (SEN = 1)

In 7-Bit Slave Receive mode, on the falling edge of the ninth clock at the end of the ACK sequence, if the BF bit is set, the CKP bit in the SSPxCON1 register is automatically cleared, forcing the SCLx output to be held low. The CKP bit being cleared to '0' will assert the SCLx line low. The CKP bit must be set in the user's ISR before reception is allowed to continue. By holding the SCLx line low, the user has time to service the ISR and read the contents of the SSPxBUF before the master device can initiate another receive sequence. This will prevent buffer overruns from occurring (see Figure 21-15).

Note 1: If the user reads the contents of the SSPxBUF before the falling edge of the ninth clock, thus clearing the BF bit, the CKP bit will not be cleared and clock stretching will not occur.

2: The CKP bit can be set in software regardless of the state of the BF bit. The user should be careful to clear the BF bit in the ISR before the next receive sequence in order to prevent an overflow condition.

21.4.4.2 Clock Stretching for 10-Bit Slave Receive Mode (SEN = 1)

In 10-Bit Slave Receive mode, during the address sequence, clock stretching automatically takes place but CKP is not cleared. During this time, if the UA bit is set after the ninth clock, clock stretching is initiated. The UA bit is set after receiving the upper byte of the 10-bit address and following the receive of the second byte of the 10-bit address with the R/W bit cleared to '0'. The release of the clock line occurs upon updating SSPxADD. Clock stretching will occur on each data receive sequence as described in 7-bit mode.

Note: If the user polls the UA bit and clears it by updating the SSPxADD register before the falling edge of the ninth clock occurs, and if the user hasn't cleared the BF bit by reading the SSPxBUF register before that time, then the CKP bit will still NOT be asserted low. Clock stretching, on the basis of the state of the BF bit, only occurs during a data sequence, not an address sequence.

21.4.4.3 Clock Stretching for 7-Bit Slave Transmit Mode

The 7-Bit Slave Transmit mode implements clock stretching by clearing the CKP bit after the falling edge of the ninth clock if the BF bit is clear. This occurs regardless of the state of the SEN bit.

The user's ISR must set the CKP bit before transmission is allowed to continue. By holding the SCLx line low, the user has time to service the ISR and load the contents of the SSPxBUF before the master device can initiate another transmit sequence (see Figure 21-10).

Note 1: If the user loads the contents of SSPxBUF, setting the BF bit before the falling edge of the ninth clock, the CKP bit will not be cleared and clock stretching will not occur.

2: The CKP bit can be set in software regardless of the state of the BF bit.

21.4.4.4 Clock Stretching for 10-Bit Slave Transmit Mode

In 10-Bit Slave Transmit mode, clock stretching is controlled during the first two address sequences by the state of the UA bit, just as it is in 10-Bit Slave Receive mode. The first two addresses are followed by a third address sequence, which contains the high-order bits of the 10-bit address and the R/W bit set to '1'. After the third address sequence is performed, the UA bit is not set, the module is now configured in Transmit mode and clock stretching is controlled by the BF flag as in 7-Bit Slave Transmit mode (see Figure 21-13).

21.4.7 BAUD RATE

In I²C Master mode, the Baud Rate Generator (BRG) reload value is placed in the lower 7 bits of the SSPxADD register (Figure 21-19). When a write occurs to SSPxBUF, the Baud Rate Generator will automatically begin counting. The BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (TCY) on the Q2 and Q4 clocks. In I²C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by $\overline{ACK}$), the internal clock will automatically stop counting and the SCLx pin will remain in its last state.

Table 21-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD. The SSPxADD BRG value of `0x00` is not supported.

21.4.7.1 Baud Rate and Module Interdependence

Because MSSP1 and MSSP2 are independent, they can operate simultaneously in I²C Master mode at different baud rates. This is done by using different BRG reload values for each module.

Because this mode derives its basic clock source from the system clock, any changes to the clock will affect both modules in the same proportion. It may be possible to change one or both baud rates back to a previous value by changing the BRG reload value.

FIGURE 21-19: BAUD RATE GENERATOR BLOCK DIAGRAM

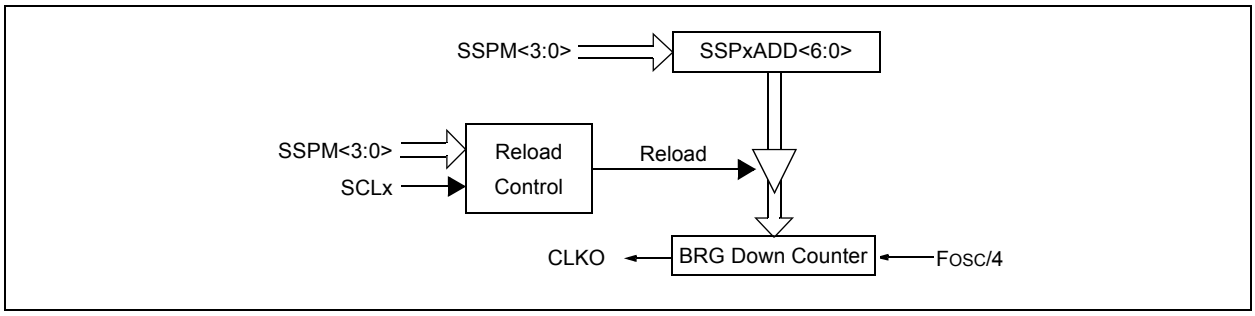


TABLE 21-3: I²C™ CLOCK RATE w/BRG

FOSC	FCY	FCY * 2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	18h	400 kHz
40 MHz	10 MHz	20 MHz	1Fh	312.5 kHz
40 MHz	10 MHz	20 MHz	63h	100 kHz
16 MHz	4 MHz	8 MHz	09h	400 kHz
16 MHz	4 MHz	8 MHz	0Ch	308 kHz
16 MHz	4 MHz	8 MHz	27h	100 kHz
4 MHz	1 MHz	2 MHz	02h	333 kHz
4 MHz	1 MHz	2 MHz	09h	100 kHz
16 MHz	4 MHz	8 MHz	03h	1 MHz(1)

Note 1: A minimum of 16 MHz FOSC is required to get 1 MHz I²C.

FIGURE 22-3: EUSART TRANSMIT BLOCK DIAGRAM

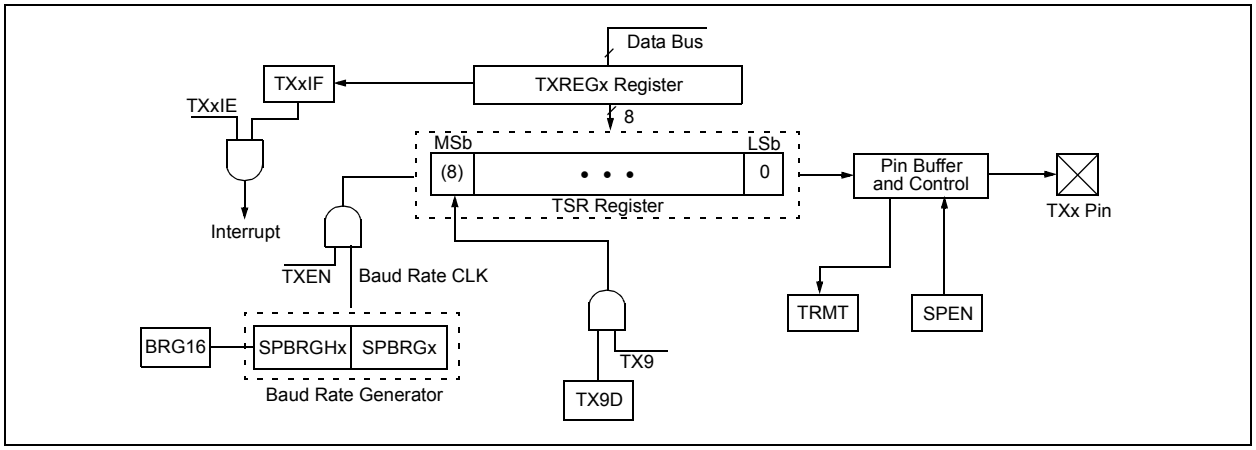


FIGURE 22-4: ASYNCHRONOUS TRANSMISSION

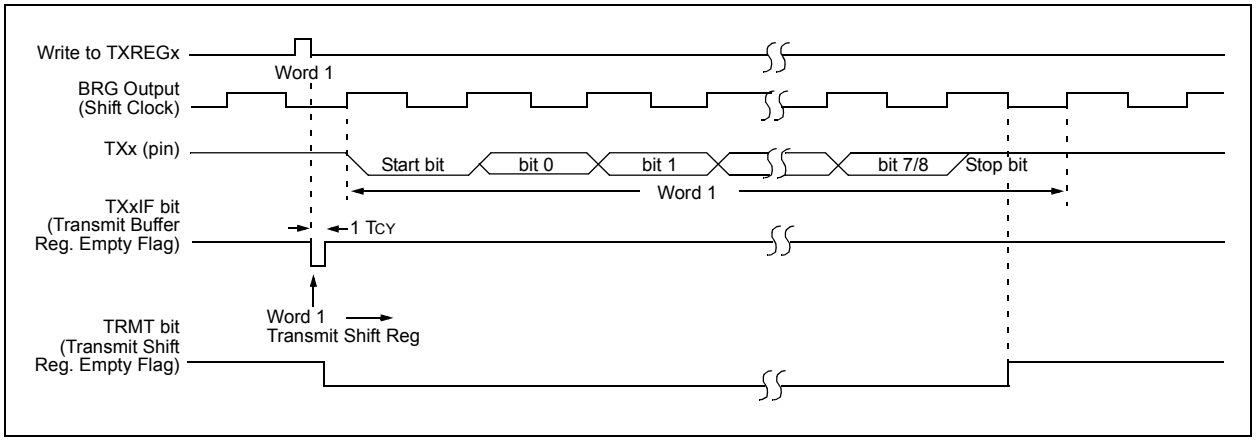
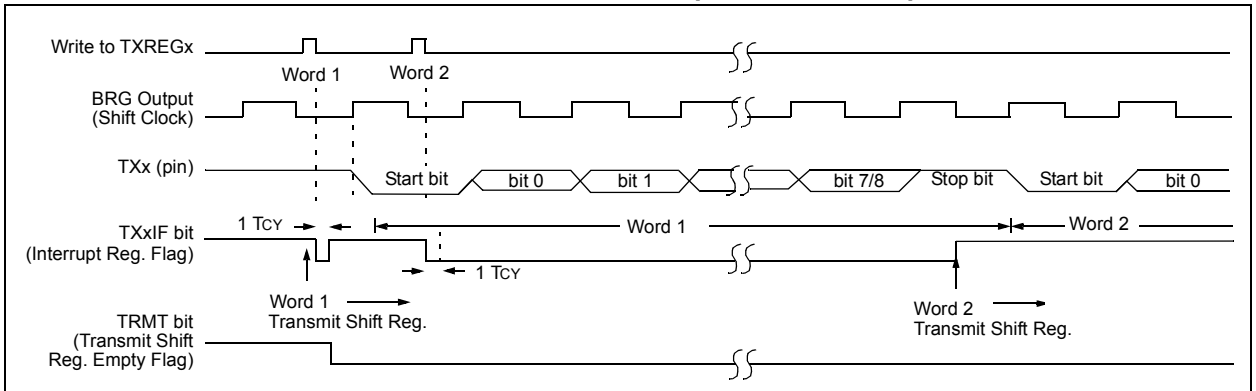


FIGURE 22-5: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)

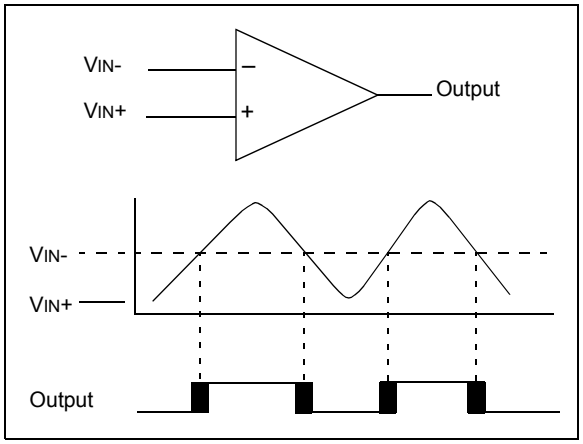


Note: This timing diagram shows two consecutive transmissions.

24.2 Comparator Operation

A single comparator is shown in Figure 24-2, along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input, VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input, VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator, in Figure 24-2, represent the uncertainty due to input offsets and response time.

FIGURE 24-2: SINGLE COMPARATOR



24.3 Comparator Response Time

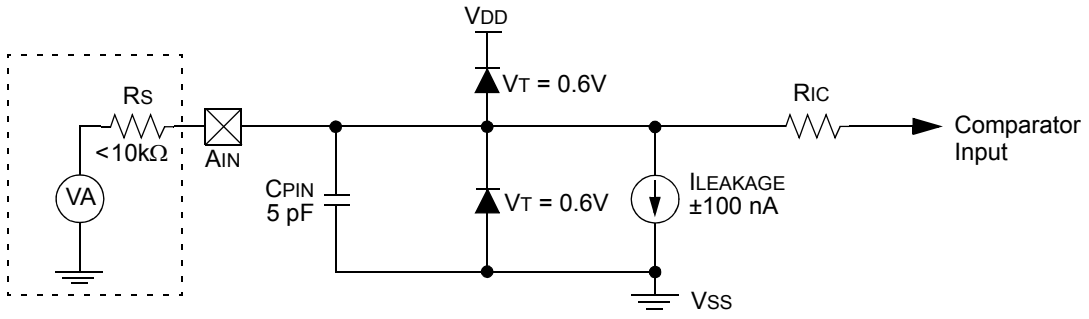
Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response to a comparator input change; otherwise, the maximum delay of the comparators should be used (see **Section 31.0 "Electrical Characteristics"**).

24.4 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 24-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up condition may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 24-3: COMPARATOR ANALOG INPUT MODEL



Legend:

CPIN	=	Input Capacitance
VT	=	Threshold Voltage
ILEAKAGE	=	Leakage Current at the pin due to various junctions
RIC	=	Interconnect Resistance
RS	=	Source Impedance
VA	=	Analog Voltage

24.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional, if enabled. This interrupt will wake up the device from Sleep mode, when enabled. Each operational comparator will consume additional current.

To minimize power consumption while in Sleep mode, turn off the comparators (CON = 0) before entering Sleep. If the device wakes up from Sleep, the contents of the CMxCON register are not affected.

24.8 Effects of a Reset

A device Reset forces the CMxCON registers to their Reset state. This forces both comparators and the voltage reference to the OFF state.

TABLE 24-3: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR6	—	—	—	EEIF	—	CMP3IF	CMP2IF	CMP1IF
PIE6	—	—	—	EEIE	—	CMP3IE	CMP2IE	CMP1IE
IPR6	—	—	—	EEIP	—	CMP3IP	CMP2IP	CMP1IP
CM1CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0
CM2CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0
CM3CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0
CVRCON	CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0
CMSTAT	CMP3OUT	CMP2OUT	CMP1OUT	—	—	—	—	—
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—
LATF	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	—
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—
PORTG	—	—	RG5(1)	RG4	RG3	RG2	RG1	RG0
LATG	—	—	—	LATG4	LATG3	LATG2	LATG1	LATG0
TRISG	—	—	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0
PORTH	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
LATH	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0
TRISH	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0
ANCON0	ANSEL7	ANSEL6	ANSEL5	ANSEL4	ANSEL3	ANSEL2	ANSEL1	ANSEL0
ANCON1	ANSEL15	ANSEL14	ANSEL13	ANSEL12	ANSEL11	ANSEL10	ANSEL9	ANSEL8
ANCON2	ANSEL23	ANSEL22	ANSEL21	ANSEL20	ANSEL19	ANSEL18	ANSEL17	ANSEL16
PMD0	CCP3MD	CCP2MD	CCP1MD	UART2MD	UART1MD	SSP2MD	SSP1MD	ADCMD

Legend: — = unimplemented, read as '0'.

Note 1: Bit is available when Master Clear is disabled (MCLRE = 0). When MCLRE is set, the bit is unimplemented.

REGISTER 28-4: CONFIG2H: CONFIGURATION REGISTER 2 HIGH (BYTE ADDRESS 300003h)

U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	WDTPS4	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN1	WDTEN0
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-2 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10101-11111 = Reserved
10100 = 1:1,048,576 (4,194.304s)
10011 = 1:524,288 (2,097.152s)
10010 = 1:262,144 (1,048.576s)
10001 = 1:131,072 (524.288s)
10000 = 1:65,536 (262.144s)
01111 = 1:32,768 (131.072s)
01110 = 1:16,384 (65.536s)
01101 = 1:8,192 (32.768s)
01100 = 1:4,096 (16.384s)
01011 = 1:2,048 (8.192s)
01010 = 1:1,024 (4.096s)
01001 = 1:512 (2.048s)
01000 = 1:256 (1.024s)
00111 = 1:128 (512 ms)
00110 = 1:64 (256 ms)
00101 = 1:32 (128 ms)
00100 = 1:16 (64 ms)
00011 = 1:8 (32 ms)
00010 = 1:4 (16 ms)
00001 = 1:2 (8 ms)
00000 = 1:1 (4 ms)

bit 1-0 **WDTEN<1:0>:** Watchdog Timer Enable bits

11 = WDT is enabled in hardware; SWDTEN bit is disabled
10 = WDT is controlled by the SWDTEN bit setting
01 = WDT is enabled only while the device is active and disabled in Sleep mode; SWDTEN bit is disabled
00 = WDT is disabled in hardware; SWDTEN bit is disabled

DAW **Decimal Adjust W Register**

Syntax: DAW

Operands: None

Operation: If [W<3:0> > 9] or [DC = 1], then
(W<3:0>) + 6 → W<3:0>;
else
(W<3:0>) → W<3:0>

If [W<7:4> > 9] or [C = 1], then
(W<7:4>) + 6 → W<7:4>;
C = 1;
else
(W<7:4>) → W<7:4>

Status Affected: C

Encoding:

0000	0000	0000	0111

Description: DAW adjusts the 8-bit value in W, resulting from the earlier addition of two variables (each in packed BCD format) and produces a correct packed BCD result.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register W	Process Data	Write W

Example 1: DAW

Before Instruction
W = A5h
C = 0
DC = 0
After Instruction
W = 05h
C = 1
DC = 0

Example 2:

Before Instruction
W = CEh
C = 0
DC = 0
After Instruction
W = 34h
C = 1
DC = 0

DECF **Decrement f**

Syntax: DECF f {,d {,a}}

Operands: 0 ≤ f ≤ 255
d ∈ [0,1]
a ∈ [0,1]

Operation: (f) – 1 → dest

Status Affected: C, DC, N, OV, Z

Encoding:

0000	01da	ffff	ffff

Description: Decrement register, 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: DECF CNT, 1, 0

Before Instruction
CNT = 01h
Z = 0
After Instruction
CNT = 00h
Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: DECFSZ f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) – 1 → dest,
skip if result = 0

Status Affected: None

Encoding:

0010	11da	ffff	ffff

Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If the result is '0', the next instruction which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    DECFSZ  CNT, 1, 1
        GOTO    LOOP
CONTINUE
```
Before Instruction
PC = Address (HERE)
After Instruction
CNT = CNT – 1
If CNT = 0;
PC = Address (CONTINUE)
If CNT ≠ 0;
PC = Address (HERE + 2)

DCFSNZ **Decrement f, Skip if Not 0**

Syntax: DCFSNZ f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) – 1 → dest,
skip if result ≠ 0

Status Affected: None

Encoding:

0100	11da	ffff	ffff

Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If the result is not '0', the next instruction which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    DCFSNZ  TEMP, 1, 0
ZERO    :
NZERO   :
```
Before Instruction
TEMP = ?
After Instruction
TEMP = TEMP – 1,
If TEMP = 0;
PC = Address (ZERO)
If TEMP ≠ 0;
PC = Address (NZERO)

GOTO **Unconditional Branch**

Syntax: GOTO k

Operands: $0 \le k \le 1048575$

Operation: $k \rightarrow PC<20:1>$

Status Affected: None

Encoding:

1st word (k<7:0>)	1110	1111	k_7kkk	$kkkk_0$
2nd word(k<19:8>)	1111	$k_{19}kkk$	kkkk	$kkkk_8$

Description: GOTO allows an unconditional branch anywhere within entire 2-Mbyte memory range. The 20-bit value 'k' is loaded into PC<20:1>. GOTO is always a two-cycle instruction.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>,	No operation	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

Example: GOTO THERE

After Instruction
PC = Address (THERE)

INCF **Increment f**

Syntax: INCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) + 1 → dest

Status Affected: C, DC, N, OV, Z

Encoding:

0010	10da	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: INCF CNT, 1, 0

Before Instruction
CNT = FFh
Z = 0
C = ?
DC = ?
After Instruction
CNT = 00h
Z = 1
C = 1
DC = 1

SUBLW **Subtract W from Literal**

Syntax: SUBLW k

Operands: $0 \le k \le 255$

Operation: $k - (W) \rightarrow W$

Status Affected: N, OV, C, DC, Z

Encoding:

0000	1000	kkkk	kkkk

Description: W is subtracted from the eight-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example 1: SUBLW 02h

Before Instruction
W = 01h
C = ?
After Instruction
W = 01h
C = 1 ; result is positive
Z = 0
N = 0

Example 2: SUBLW 02h

Before Instruction
W = 02h
C = ?
After Instruction
W = 00h
C = 1 ; result is zero
Z = 1
N = 0

Example 3: SUBLW 02h

Before Instruction
W = 03h
C = ?
After Instruction
W = FFh ; (2's complement)
C = 0 ; result is negative
Z = 0
N = 1

SUBWF **Subtract W from f**

Syntax: SUBWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: $(f) - (W) \rightarrow$ dest

Status Affected: N, OV, C, DC, Z

Encoding:

0101	11da	ffff	ffff

Description: Subtract W from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: SUBWF REG, 1, 0

Before Instruction
REG = 3
W = 2
C = ?
After Instruction
REG = 1
W = 2
C = 1 ; result is positive
Z = 0
N = 0

Example 2: SUBWF REG, 0, 0

Before Instruction
REG = 2
W = 2
C = ?
After Instruction
REG = 2
W = 0
C = 1 ; result is zero
Z = 1
N = 0

Example 3: SUBWF REG, 1, 0

Before Instruction
REG = 1
W = 2
C = ?
After Instruction
REG = FFh ;(2's complement)
W = 2
C = 0 ; result is negative
Z = 0
N = 1

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K22 Family (Industrial/Extended) (Continued)

PIC18F87K22 Family (Industrial/Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.(2,3)						
	All devices	2.1	5.5	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 31 kHz (**RC_IDLE** mode, LF-INTOSC)
		2.1	5.7	µA	+25°C		
		2.2	6.0	µA	+85°C		
		10	20	µA	+125ºC		
	All devices	3.7	7.5	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		3.9	7.8	µA	+25°C		
		3.9	8.5	µA	+85°C		
		12	24	µA	+125ºC		
	All devices	70	180	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		80	190	µA	+25°C		
		80	200	µA	+85°C		
		200	420	µA	+125ºC		
	All devices	330	650	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 1 MHz (**RC_IDLE** mode, HF-INTOSC)
		330	640	µA	+25°C		
		330	630	µA	+85°C		
		500	850	µA	+125ºC		
	All devices	520	850	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		520	900	µA	+25°C		
		520	850	µA	+85°C		
		800	1200	µA	+125ºC		
	All devices	590	940	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		600	960	µA	+25°C		
		620	990	µA	+85°C		
		1000	1400	µA	+125ºC		
	All devices	470	770	µA	-40°C	VDD = 1.8V(4) Regulator Disabled	FOSC = 4 MHz (**RC_IDLE** mode, internal HF-INTOSC)
		470	770	µA	+25°C		
		460	760	µA	+85°C		
		700	1000	µA	+125ºC		
	All devices	800	1400	µA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		800	1350	µA	+25°C		
		790	1300	µA	+85°C		
		1100	1400	µA	+125ºC		
	All devices	880	1600	µA	-40°C	VDD = 5V(5) Regulator Enabled	
		890	1700	µA	+25°C		
		910	1800	µA	+85°C		
		1200	2200	µA	+125ºC		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in Active Operation mode are:
OSC1 = External square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

6: 48 MHz, maximum frequency at +125ºC.