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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	99
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12h128vfve

  - Inter-Integrated Circuit interface (IIC)
- Liquid Crystal Display driver with variable input voltage
  - Configurable for up to 32 frontplanes and 4 backplanes or general purpose input or output
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Unused frontplane and backplane pins can be used as general purpose I/O
- 16, 24 high current drivers suited for PWM motor control
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Left, right and center aligned outputs
  - Support for sine and cosine drive
  - Dithering
  - Output slew rate control
- 144-Pin or 112-Pin LQFP package
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs
  - Operation at 32MHz equivalent to 16MHz Bus Speed
  - Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Freescale Use Only**)
  - Special Peripheral Mode (**Freescale Use Only**)

Low power modes

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$009F	ATDDR7L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A0	ATDDR8H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A1	ATDDR8L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A2	ATDDR9H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A3	ATDDR9L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A4	ATDDR10H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A5	ATDDR10L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A6	ATDDR11H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A7	ATDDR11L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A8	ATDDR12H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A9	ATDDR12L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00AA	ATDDR13H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AB	ATDDR13L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00AC	ATDDR14H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AD	ATDDR14L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00aE	ATDDR15H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AF	ATDDR15L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								

$00B0 - $00BF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00B0 - $00BF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C0 - $00C7 IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C0	IBAD	Read: Write:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
$00E1	IBFD	Read: Write:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0

$0110 - $011B EEPROM Control Register (eets4k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0119	EADDRLO	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$011A	EDATAHI	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$011B	EDATALO	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$011C - $011F Reserved for RAM Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$011C - $011F	Reserved	Read: Write:	0	0	0	0	0	0	0	0

$0120 - $0137 LCD (Liquid Crystal Display 32 frontplanes, 4 backplanes)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	LCDCR0	Read: Write:	LCDEN	0	LCLK2	LCLK1	LCLK0	BIAS	DUTY1	DUTY0
$0121	LCDCR1	Read: Write:	0	0	0	0	0	0	LCDSWAI	LCDRPSTP
$0122	FPENR0	Read: Write:	FPEN7	FPEN6	FPEN5	FPEN4	FPEN3	FPEN2	FPEN1	FPEN0
$0123	FPENR1	Read: Write:	FPEN15	FPEN14	FPEN13	FPEN12	FPEN11	FPEN10	FPEN9	FPEN8
$0124	FPENR2	Read: Write:	FPEN23	FPEN22	FPEN21	FPEN20	FPEN19	FPEN18	FPEN17	FPEN16
$0125	FPENR3	Read: Write:	FPEN31	FPEN30	FPEN29	FPEN28	FPEN27	FPEN26	FPEN25	FPEN24
$0126	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0127	Reserved	Read: Write:	0	0	0	0	0	0	0	0
$0128	LCDRAM0	Read: Write:	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
$0129	LCDRAM1	Read: Write:	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
$012A	LCDRAM2	Read: Write:	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
$012B	LCDRAM3	Read: Write:	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
$012C	LCDRAM4	Read: Write:	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
$012D	LCDRAM5	Read: Write:	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
$012E	LCDRAM6	Read: Write:	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
$012F	LCDRAM7	Read: Write:	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0

$01C0 - $01FF MC (Motor Controller 10bit 12 channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01CC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CD	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01D0	MCCC0	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D1	MCCC1	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D2	MCCC2	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D3	MCCC3	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D4	MCCC4	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D5	MCCC5	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D6	MCCC6	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D7	MCCC7	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D8	MCCC8	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D9	MCCC9	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01DA	MCCC10	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01DB	MCCC11	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01DD	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01E0	MCDC0 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01E1	MCDC0 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01E2	MCDC1 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01E3	MCDC1 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01E4	MCDC2 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								

2.3.22 FreescalePL[7:4] / FP[31:28] — Port L I/O Pins [7:4]

PL7-PL4 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP31-FP28 of the LCD module.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.23 PL[3:0] / FP[19:16] — Port L I/O Pins [3:0]

PL3-PL0 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP19-FP16 of the LCD module.

2.3.24 PM5 / TXCAN1 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.25 PM4 / RXCAN1 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.26 PM3 / TXCAN0 — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.27 PM2 / RXCAN0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.28 PM1 / SCL — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the serial clock pin SCL of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.29 PM0 / SDA — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the serial data pin SDA of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.30 PP[5:2] / PWM[5:2] — Port P I/O Pins [5:2]

PP5-PP2 are general purpose input or output pins. They can be configured as Pulse Width Modulator (PWM) channel outputs PWM5-PWM2.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.31 PP[1:0] / PWM[1:0] — Port P I/O Pins [1:0]

PP1-PP0 are general purpose input or output pins. They can be configured as Pulse Width Modulator (PWM) channel outputs PWM1-PWM0.

2.3.32 PS7 / $\overline{SS}$ — Port S I/O Pin 7

PS7 is a general purpose input or output pin. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface (SPI).

2.3.33 PS6 / SCK — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as serial clock pin SCK of the Serial Peripheral Interface (SPI).

2.3.34 PS5 / MOSI — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as the master output (during master mode) or slave input (during slave mode) pin MOSI of the Serial Peripheral Interface (SPI).

2.3.35 PS4 / MISO — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO for the Serial Peripheral Interface (SPI).

2.3.36 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as transmit pin TXD1 of the Serial Communication Interface 1 (SCI1).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.37 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as receive pin RXD1 of the Serial Communication Interface 1 (SCI1).

NOTE: *This pin is not available in the 112-pin LQFP version.*

If an internal access is made while E, R/$\overline{W}$, and $\overline{LSTRB}$ are configured as bus control outputs and internal visibility is off (IVIS=0), E will remain low for the cycle, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

When internal visibility is enabled (IVIS=1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected, R/$\overline{W}$ will remain high, data will maintain its previous state, and address and $\overline{LSTRB}$ pins will be updated with the internal value. During CPU no access cycles when the BDM is not driving, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

4.2.1.5 Emulation Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. These signals allow external memory and peripheral devices to be interfaced to the MCU. These signals can also be used by a logic analyzer to monitor the progress of application programs.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in special mode are restricted.

4.2.1.6 Emulation Expanded Narrow Mode

Expanded narrow modes are intended to allow connection of single 8-bit external memory devices for lower cost systems that do not need the performance of a full 16-bit external data bus. Accesses to internal resources that have been mapped external (i.e. PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, PUCR, RDRIV) will be accessed with a 16-bit data bus on Ports A and B. Accesses of 16-bit external words to addresses which are normally mapped external will be broken into two separate 8-bit accesses using Port A as an 8-bit data bus. Internal operations continue to use full 16-bit data paths. They are only visible externally as 16-bit information if IVIS=1.

Ports A and B are configured as multiplexed address and data output ports. During external accesses, address A15, data D15 and D7 are associated with PA7, address A0 is associated with PB0 and data D8 and D0 are associated with PA0. During internal visible accesses and accesses to internal resources that have been mapped external, address A15 and data D15 is associated with PA7 and address A0 and data D0 is associated with PB0.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in special mode are restricted.

4.2.2 Special Operating Modes

There are two special operating modes that correspond to normal operating modes. These operating modes are commonly used in factory testing and system development.

4.2.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull-ups disabled; however, writing to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the Port E pins (except PE4/ECLK) are initially configured as general purpose high-impedance inputs with pull-ups enabled. PE4/ECLK is configured as the E clock output in this mode.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

4.2.2.2 Special Test Mode (Freescale Use Only)

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

4.2.3 Test Operating Mode (Freescale Use Only)

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

4.2.3.1 Peripheral Mode

This mode is intended for Freescale factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different mode. Background debugging should not be used while the MCU is in special peripheral mode as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the HCS12 Core User Guide for information on resets and interrupts.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Reset and Interrupt Vector Table

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	External or Power On Reset	None	None	-
$FFFC, $FFFD	Clock Monitor fail reset	None	COPCTL (CME, FCME)	-
$FFFA, $FFFB	COP failure reset	None	COP rate select	-
$FFF8, $FFF9	Unimplemented instruction trap	None	None	-
$FFF6, $FFF7	SWI	None	None	-
$FFF4, $FFF5	$\overline{\text{XIRQ}}$	X-Bit	None	-
$FFF2, $FFF3	$\overline{\text{IRQ}}$	I-Bit	INTCR (IRQEN)	$F2
$FFF0, $FFF1	Real Time Interrupt	I-Bit	RTICTL (RTIE)	$F0
$FFEE, $FFEF	Timer channel 0	I-Bit	TIE (C0I)	$EE
$FFEC, $FFED	Timer channel 1	I-Bit	TIE (C1I)	$EC
$FFEA, $FFEB	Timer channel 2	I-Bit	TIE (C2I)	$EA
$FFE8, $FFE9	Timer channel 3	I-Bit	TIE (C3I)	$E8
$FFE6, $FFE7	Timer channel 4	I-Bit	TIE (C4I)	$E6
$FFE4, $FFE5	Timer channel 5	I-Bit	TIE (C5I)	$E4
$FFE2, $FFE3	Timer channel 6	I-Bit	TIE (C6I)	$E2
$FFE0, $FFE1	Timer channel 7	I-Bit	TIE (C7I)	$E0
$FFDE, $FFDF	Timer overflow	I-Bit	TSCR2 (TOI)	$DE
$FFDC, $FFDD	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)	$DC
$FFDA, $FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	$DA
$FFD8, $FFD9	SPI	I-Bit	SPICR1 (SPIE)	$D8
$FFD6, $FFD7	SCI0	I-Bit	SC0CR2 (TIE, TCIE, RIE, ILIE)	$D6
$FFD4, $FFD5	SCI1	I-Bit	SC1CR2 (TIE, TCIE, RIE, ILIE)	$D4
$FFD2, $FFD3	ATD	I-Bit	ATDCTL2 (ASCIE)	$D2
$FFD0, $FFD1	Reserved			
$FFCE, $FFCF	Port J	I-Bit	PTJIF (PTJIE)	$CE
$FFCC, $FFCD	Port H	I-Bit	PTHIF (PTHIE)	$CC
$FFCA, $FFCB	Reserved			

Table 5-1 Reset and Interrupt Vector Table

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFC8, $FFC9	Reserved			
$FFC6, $FFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	$C4
$FFC2, $FFC3	Reserved			
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR (IBIE)	$C0
$FFBE, $FFBF	Reserved			
$FFBC, $FFBD	Reserved			
$FFBA, $FFBB	EEPROM	I-Bit	EECTL (CCIE, CBEIE)	$BA
$FFB8, $FFB9	FLASH	I-Bit	FCTL (CCIE, CBEIE)	$B8
$FFB6, $FFB7	CAN0 wake-up	I-Bit	CAN0RIER (WUPIE)	$B6
$FFB4, $FFB5	CAN0 errors	I-Bit	CAN0RIER (CSCIE, OVRIE)	$B4
$FFB2, $FFB3	CAN0 receive	I-Bit	CAN0RIER (RXFIE)	$B2
$FFB0, $FFB1	CAN0 transmit	I-Bit	CAN0TIER (TXEIE[2:0])	$B0
$FFAE, $FFAF	CAN1 wake-up	I-Bit	CAN0RIER (WUPIE)	$AE
$FFAC, $FFAD	CAN1 errors	I-Bit	CAN1RIER (CSCIE, OVRIE)	$AC
$FFAA, $FFAB	CAN1 receive	I-Bit	CAN1RIER (RXFIE)	$AA
$FFA8, $FFA9	CAN1 transmit	I-Bit	CAN1TIER (TXEIE[2:0])	$A8
$FF98 to $FFA7	Reserved			
$FF96, $FF97	Motor Control Timer Overflow	I-Bit	MCCTL1 (MCOCIE)	$96
$FF9E to $FF95	Reserved			
$FF8C, $FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN(PWMIE)	$8C
$FF80 to $FF8B	Reserved			

5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 I/O pins

Refer to the HCS12 Core User Guides for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

NOTE: *For devices assembled in 112-pin LQFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to* ***Table 2-1*** *for affected pins.*

Section 6 HCS12 Core Block Description

Consult the HCS12 Core User Guide for information about the HCS12 core modules, i.e. central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), breakpoint module (BKP) and background debug mode module (BDM).

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

7.1.1 XCLKS

The XCLKS input signal is active high (see **2.3.10 PE7 / FP22 / XCLKS / NOACC — Port E I/O Pin 7**).

Section 8 Timer (TIM) Block Description

Consult the TIM_16B8C Block User Guide for information about the Timer module.

Section 9 Analog to Digital Converter (ATD) Block Description

Consult the ATD_10B16C Block User Guide for information about the Analog to Digital Converter module.

Section 10 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 11 Serial Communications Interface (SCI) Block Description

VDD1, VSS1 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX1, VDDX2, VDDM as well as VSSA, VSSX1, VSSX2 and VSSM are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDM, VDDR and VDDX1/2; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX1/2, VDDM and VDDR pins.*
VDD is used for VDD1 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDDPLL.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Ensure external VDD5 load will shunt current greater than maximum injection current. This will be the

greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	–0.3	6.0	V
2	Digital Logic Supply Voltage [2]	V_{DD}	–0.3	3.0	V
3	PLL Supply Voltage [2]	V_{DDPLL}	–0.3	3.0	V
4	Voltage difference VDDX1 to VDDX2 to VDDM and VDDA	Δ_{VDDX}	–0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	–0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	–0.3	6.0	V
7	Analog Reference	$V_{RH,}$ V_{RL}	–0.3	6.0	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	–0.3	3.0	V
9	TEST input	V_{TEST}	–0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins except PU, PV and PW [3]	I_D	–25	+25	mA
11	Instantaneous Maximum Current Single pin limit for Port PU, PV and PW [4]	I_D	–55	+55	mA
12	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[5]	I_{DL}	–25	+25	mA
13	Instantaneous Maximum Current Single pin limit for TEST [6]	I_{DT}	–0.25	0	mA
14	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. Beyond absolute maximum ratings device might be damaged.
2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to $V_{SSX1/2}$ and $V_{DDX1/2}$, V_{SSM} and V_{DDM} or V_{SSA} and V_{DDA}.
4. Ports PU, PV, PW are internally clamped to V_{SSM} and V_{DDM}.

Table A-6 5V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	–	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	V_{SS5} – 0.3	–	0.35*V_{DD5}	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current except PU, PV, PW (pins in high impedance input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–1.0	–	1.0	µA
5	P	Input Leakage Current PU, PV, PW (pins in high impedance input mode)[2] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	–	2.5	µA
6	P	Output High Voltage (pins in output mode, except PU, PV and PW) Partial Drive I_{OH} = –1.0mA Full Drive I_{OH} = –10mA	V_{OH}	V_{DD5} – 0.8	–	–	V
7	P	Output Low Voltage (pins in output mode except PU, PV and PW) Partial Drive I_{OL} = +1.0mA Full Drive I_{OL} = +10mA	V_{OL}	–	–	0.8	V
8	P	Output High Voltage (pins PU, PV and PW in output mode) I_{OH} = –20mA	V_{OH}	V_{DD5} – 0.32	V_{DD5} – 0.2	–	V
9	P	Output Low Voltage (pins PU, PV and PW in output mode) I_{OL} = +20mA	V_{OL}	–	.2	0.32	V
10	P	Output Rise Time (pins PU, PV and PW in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH} -40°C, EPP package 25°C, 140°C	t_r	 60 60	 120[3] 100	 180[3] 130	ns
11	P	Output Fall Time (pins PU, PV and PW in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH} -40°C, EPP package 25°C, 140°C	t_f	 60 60	 120[3] 100	 180[3] 130	ns
12	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	–	–	–130	µA
13	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–10	–	–	µA
14	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	–	–	130	µA
15	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	–	–	µA

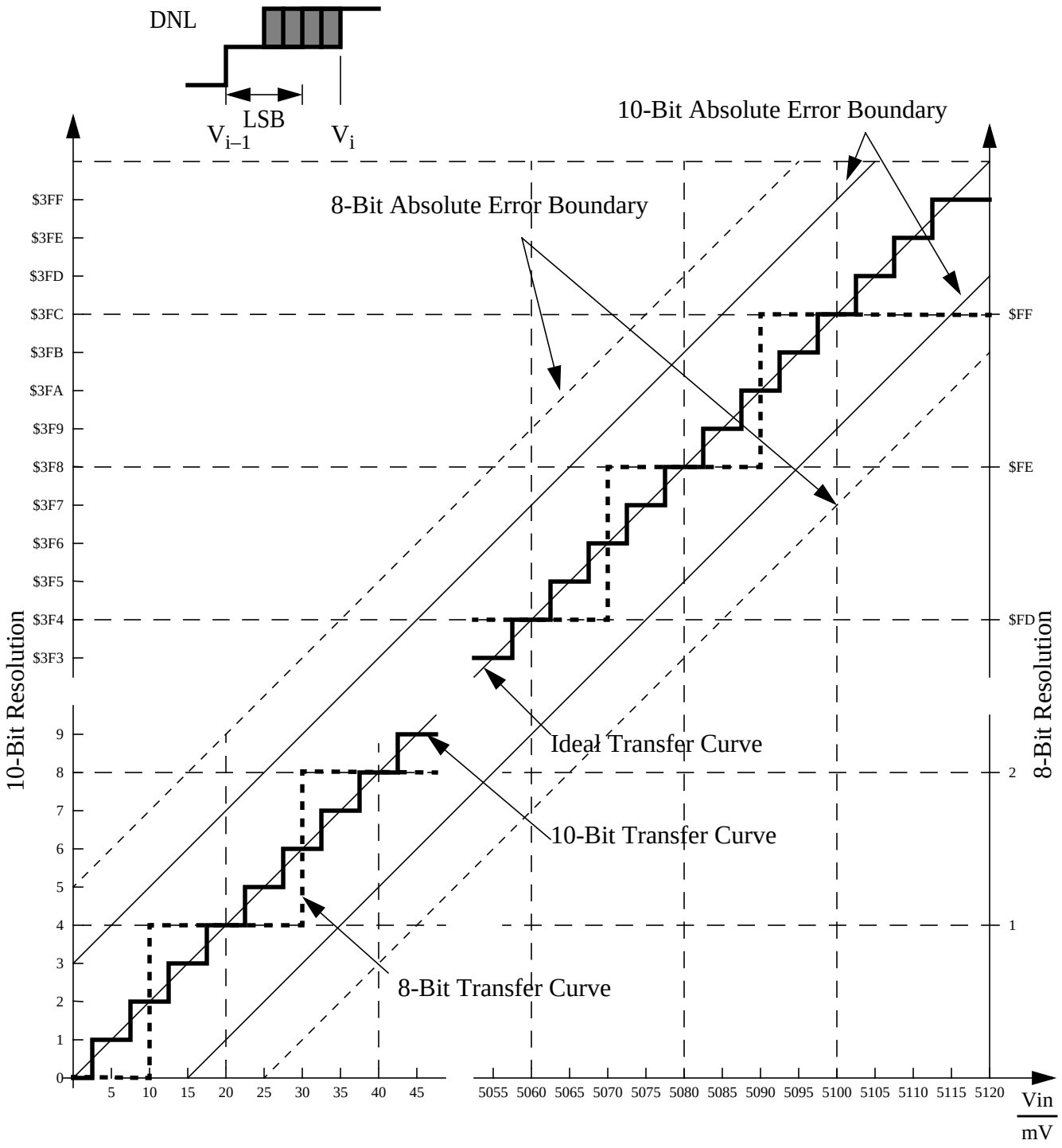

Figure A-1 ATD Accuracy Definitions

NOTE: ***Figure A-1*** *shows only definitions, for specification values refer to* ***Table A-10****.*

3. XCLKS =1 during reset

A.4.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.4.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

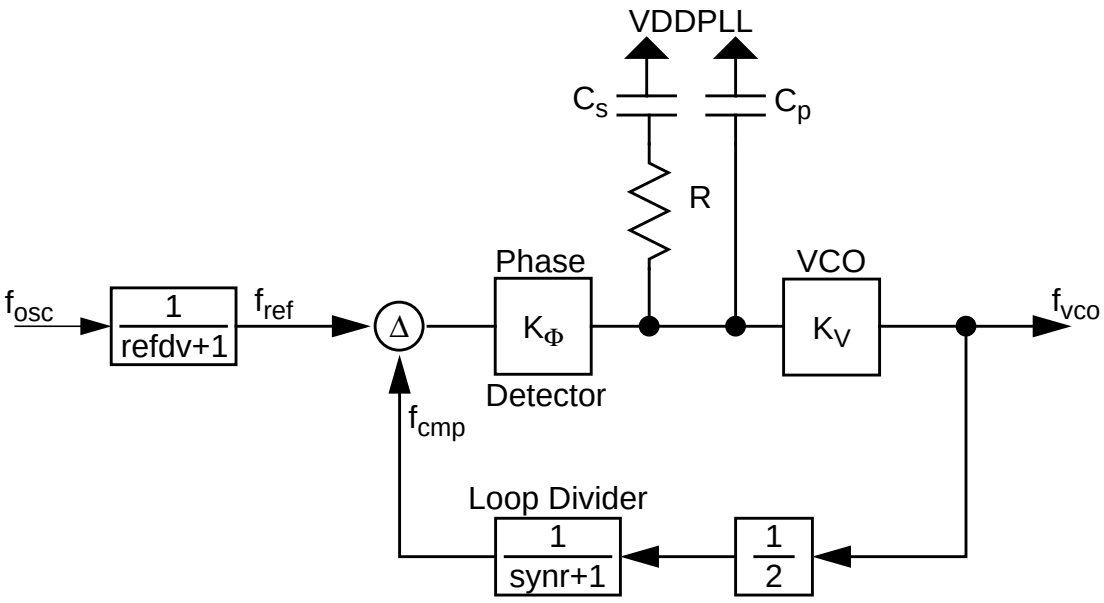

Figure A-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-15**.

The VCO Gain at the desired VCO output frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}}$$

The phase detector relationship is given by:

$$K_\Phi = i_{ch} \cdot K_V$$

i_{ch} is the current in tracking mode.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12H256 and MC9S12H128 packages.

User Guide End Sheet