Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12h128vpve

  - BDM (Background Debug Mode)
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- 8-bit and 4-bit ports with interrupt functionality
  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 128K, 256K Flash EEPROM
  - 2K, 4K byte EEPROM
  - 6K, 12K byte RAM
- Analog-to-Digital Converter
  - 8, 16 channels, 10-bit resolution
  - External conversion trigger capability
- Two 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 2, 6 PWM channels
  - Programmable period and duty cycle
  - 8-bit 2, 6-channel or 16-bit 1, 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Synchronous Serial Peripheral Interface (SPI)

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 is a block diagram of the MC9S12H256 device.

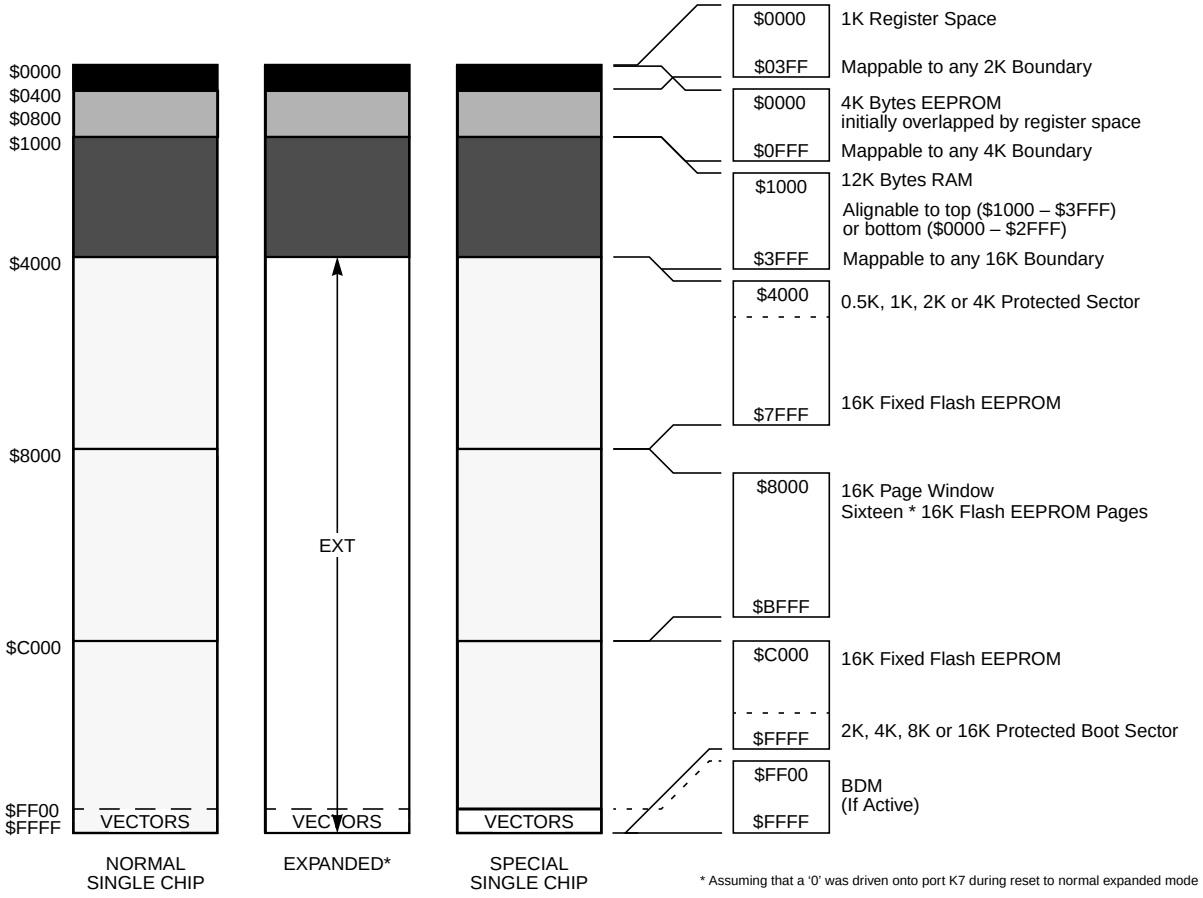


Figure 1-3 MC9S12H256 Memory Map

Table 1-2 and **Figure 1-4** show the device memory map of the MC9S12H128.

Table 1-2 Device Memory Map MC9S12H128

Address	Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 – $0019	Reserved	2
$001A – $001B	Device ID register (PARTID)	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	8
$0028 – $002F	CORE (Background Debug Mode)	8
$0030 – $0033	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $006F	Standard Timer Module 16-bit 8 channels (TIM)	48
$0070 – $007F	Reserved	16
$0080 – $00AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
$00B0 – $00BF	Reserved	16
$00C0 – $00C7	Inter Integrated Circuit (IIC)	8

$0040 - $006F TIM (Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$004A	TCTL3	Read:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Write:								
$004B	TCTL4	Read:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		Write:								
$004C	TIE	Read:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
		Write:								
$004D	TSCR2	Read:	TOI	0	0	0	TCRE	PR2	PR1	PR0
		Write:								
$004E	TFLG1	Read:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
		Write:								
$004F	TFLG2	Read:	TOF	0	0	0	0	0	0	0
		Write:								
$0050	TC0 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0051	TC0 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0052	TC1 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0053	TC1 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0054	TC2 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0055	TC2 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0056	TC3 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0057	TC3 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0058	TC4 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0059	TC4 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005A	TC5 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005B	TC5 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005C	TC6 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005D	TC6 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005E	TC7 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005F	TC7 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0060	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
$0061	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:								
$0062	PACNT (hi)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$022C	PERJ	Read:	0	0	0	0	PERJ3	PERJ2	PERJ1	PERJ0
		Write:								
$022D	PPSJ	Read:	0	0	0	0	PPSJ3	PPSJ2	PPSJ1	PPSJ0
		Write:								
$022E	PIEJ	Read:	0	0	0	0	PIEJ3	PIEJ2	PIEJ1	PIEJ0
		Write:								
$022F	PIFJ	Read:	0	0	0	0	PIFJ3	PIFJ2	PIFJ1	PIFJ0
		Write:								
$0230	PTL	Read:	PTL7	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
		Write:								
$0231	PTIL	Read:	PTIL7	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
		Write:								
$0232	DDRL	Read:	DDRL7	DDRL7	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
		Write:								
$0233	RDRL	Read:	RDRL7	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
		Write:								
$0234	PERL	Read:	PERL7	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
		Write:								
$0235	PPSL	Read:	PPSL7	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
		Write:								
$0236	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0237	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0238	PTU	Read:	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		Write:								
$0239	PTIU	Read:	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		Write:								
$023A	DDRU	Read:	DDRU7	DDRU7	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		Write:								
$023B	SRRU	Read:	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
		Write:								
$023C	PERU	Read:	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		Write:								
$023D	PPSU	Read:	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		Write:								
$023E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0240	PTV	Read:	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
		Write:								
$0241	PTIV	Read:	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
		Write:								
$0242	DDRV	Read:	DDRV7	DDRV7	DDRV5	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
		Write:								
$0243	SRRV	Read:	SRRV7	SRRV6	SRRV5	SRRV4	SRRV3	SRRV2	SRRV1	SRRV0
		Write:								
$0244	PERV	Read:	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0245	PPSV	Read:	PPSV7	PPSV6	PPSV5	PPSV4	PPSV3	PPSV2	PPSV1	PPSV0
		Write:								
$0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0248	PTW	Read:	PTW7	PTW6	PTW5	PTW4	PTW3	PTW2	PTW1	PTW0
		Write:								
$0249	PTIW	Read:	PTIW7	PTIW6	PTIW5	PTIW4	PTIW3	PTIW2	PTIW1	PTIW0
		Write:								
$024A	DDRW	Read:	DDRW7	DDRW7	DDRW5	DDRW4	DDRW3	DDRW2	DDRW1	DDRW0
		Write:								
$024B	SRRW	Read:	SRRW7	SRRW6	SRRW5	SRRW4	SRRW3	SRRW2	SRRW1	SRRW0
		Write:								
$024C	PERW	Read:	PERW7	PERW6	PERW5	PERW4	PERW3	PERW2	PERW1	PERW0
		Write:								
$024D	PPSW	Read:	PPSW7	PPSW6	PPSW5	PPSW4	PPSW3	PPSW2	PPSW1	PPSW0
		Write:								
$024E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250 - $027F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0280 - $03FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0280 - $03FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL at addresses $001A,$001B, respectively. The read-only value is a unique part ID for each revision of the chip. **Table 1-5** shows the assigned part ID numbers.

Table 1-5 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12H256	0K78X	$1000
MC9S12H256	1K78X	$1001

2.3.22 FreescalePL[7:4] / FP[31:28] — Port L I/O Pins [7:4]

PL7-PL4 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP31-FP28 of the LCD module.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.23 PL[3:0] / FP[19:16] — Port L I/O Pins [3:0]

PL3-PL0 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP19-FP16 of the LCD module.

2.3.24 PM5 / TXCAN1 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.25 PM4 / RXCAN1 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.26 PM3 / TXCAN0 — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.27 PM2 / RXCAN0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.28 PM1 / SCL — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the serial clock pin SCL of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.29 PM0 / SDA — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the serial data pin SDA of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12H256. Each mode has an associated default memory map and external bus configuration.

Three low power modes exist for the device.

4.2 Modes of Operation

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (**Table 4-1**). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

Table 4-1 Mode Selection

MODC	MODB	MODA	Mode Description
0	0	0	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	Emulation Expanded Narrow, BDM allowed
0	1	0	Special Test (Expanded Wide) (**Freescale Use Only**), BDM allowed
0	1	1	Emulation Expanded Wide, BDM allowed
1	0	0	Normal Single Chip, BDM allowed
1	0	1	Normal Expanded Narrow, BDM allowed
1	1	0	Peripheral (**Freescale Use Only**); BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	Normal Expanded Wide, BDM allowed

There are two basic types of operating modes:

1. Normal modes: Some registers and bits are protected against accidental changes.
2. Special modes: Allow greater access to protected control registers and bits for special purposes such as testing.

A system development and debug feature, background debug mode (BDM), is available in all modes. In special single-chip mode, BDM is active immediately after reset.

Some aspects of Port E are not mode dependent. Bit 1 of Port E is a general purpose input or the $\overline{\text{IRQ}}$ interrupt input. $\overline{\text{IRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. Bit 0 of Port E is a general purpose input or the $\overline{\text{XIRQ}}$ interrupt input. $\overline{\text{XIRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. The ESTR bit in the EBICTL register is set to one by reset in any user mode. This assures that the reset vector can be fetched

even if it is located in an external slow memory device. The PE6/MODB/IPIPE1 and PE5/MODA/IPIPE0 pins act as high-impedance mode select inputs during reset.

The following paragraphs discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

4.2.1 Normal Operating Modes

These modes provide three operating configurations. Background debug is available in all three modes, but must first be enabled for some operations by means of a BDM background command, then activated.

4.2.1.1 Normal Single-Chip Mode

There is no external expansion bus in this mode. All pins of Ports A, B and E are configured as general purpose I/O pins Port E bits 1 and 0 are available as general purpose input only pins with internal pull-ups enabled. All other pins of Port E are bidirectional I/O pins that are initially configured as high-impedance inputs with internal pull-ups enabled. Ports A and B are configured as high-impedance inputs with their internal pull-ups disabled.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE, and RDWE are reset to zero. Writing the opposite state into them in single chip mode does not change the operation of the associated Port E pins.

In normal single chip mode, the MODE register is writable one time. This allows a user program to change the bus mode to narrow or wide expanded mode and/or turn on visibility of internal accesses.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

4.2.1.2 Normal Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E bit 4 is configured as the E clock output signal. These signals allow external memory and peripheral devices to be interfaced to the MCU.

Port E pins other than PE4/ECLK are configured as general purpose I/O pins (initially high-impedance inputs with internal pull-up resistors enabled). Control bits PIPOE, NECLK, LSTRE, and RDWE in the PEAR register can be used to configure Port E pins to act as bus control outputs instead of general purpose I/O pins.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. Development systems where pipe status signals are monitored would typically use the special variation of this mode.

The Port E bit 2 pin can be reconfigured as the R/$\overline{\text{W}}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded system includes external devices that can be written, such as RAM, the RDWE bit

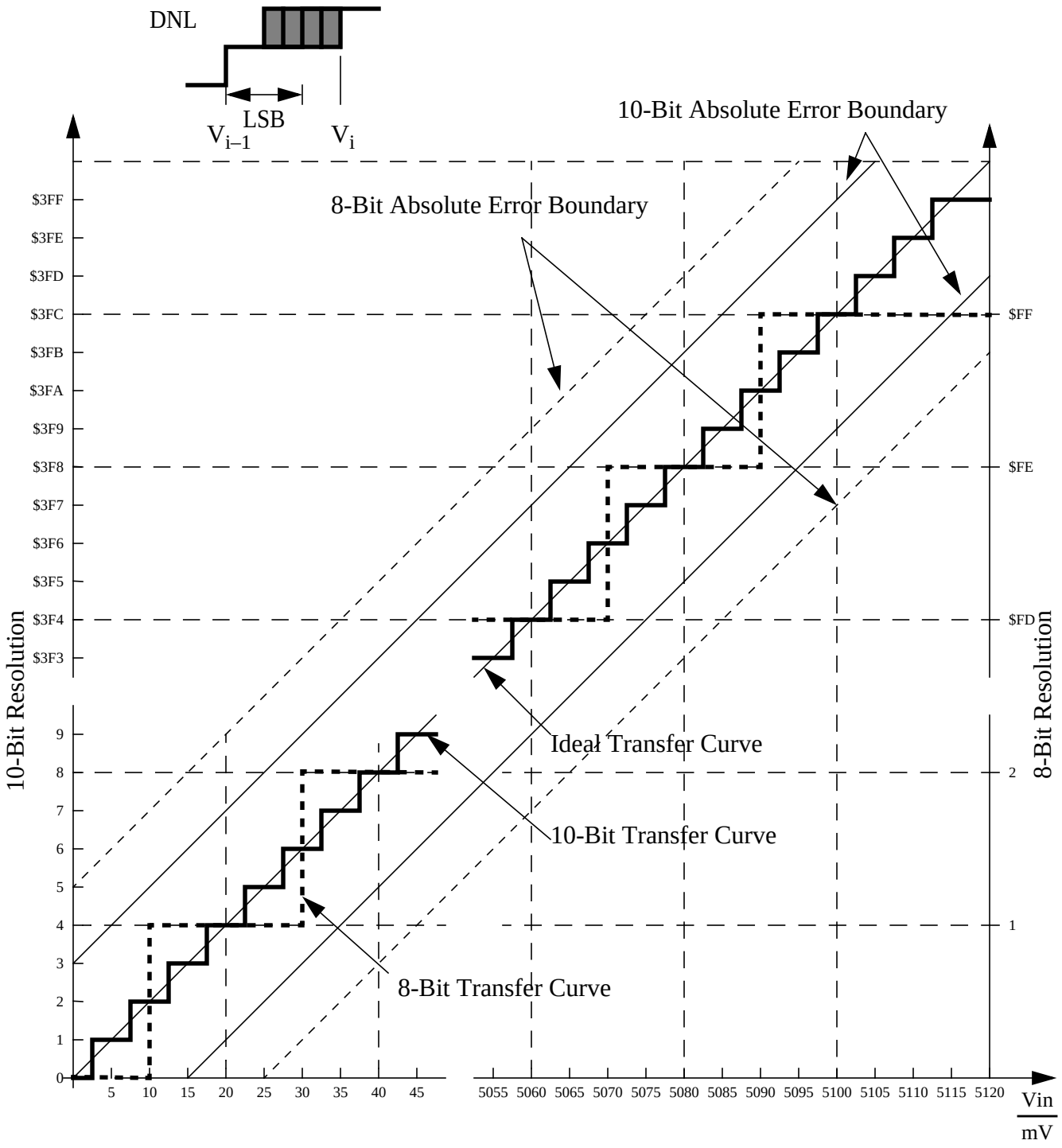


Figure A-1 ATD Accuracy Definitions

NOTE: ***Figure A-1*** *shows only definitions, for specification values refer to* ***Table A-10****.*

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

Table A-11 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		32 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]		31 [3]	µs
6	D	Flash Burst Programming Time for 32 Words [4]	t_{brpgm}	678.4 [2]		1035.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]		133 [3]	ms

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **A.3.1.1 - A.3.1.4** for guidance.
4. urst Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

A.4 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.4.1 Startup

Table A-13 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-13 Startup Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.4.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the VDD supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.4.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.4.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-15 PLL Characteristics

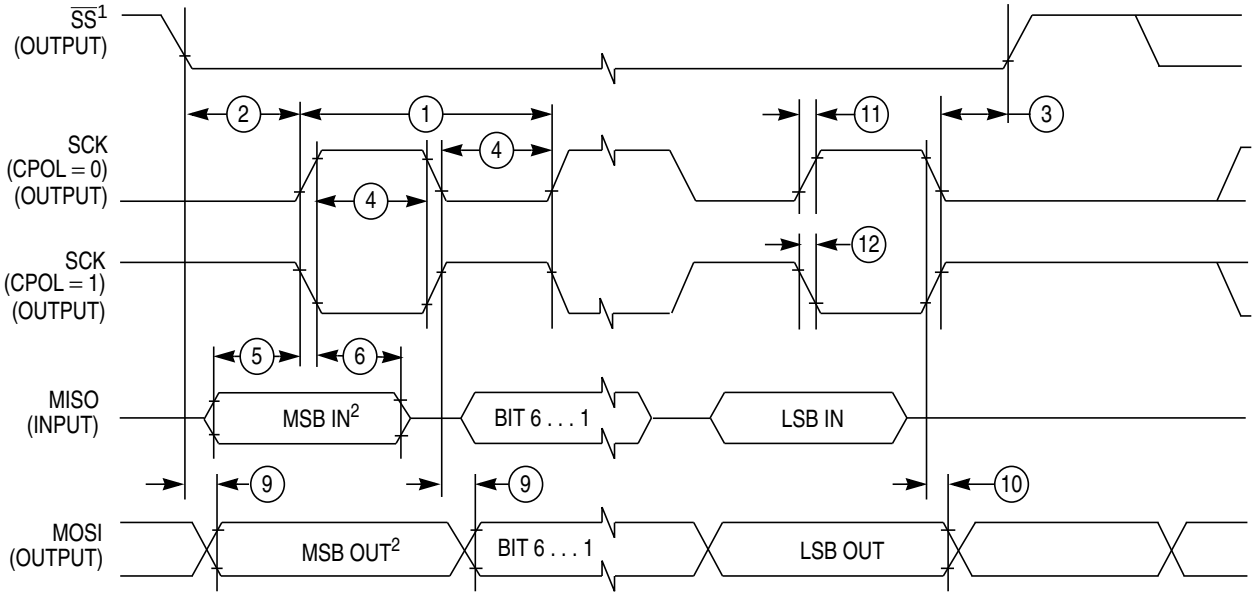
Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		32	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [2]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}		0.2		ms
10	P	Fitting parameter VCO loop gain[3]	K_1		–120	-224	MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		75		MHz
12	P	Charge pump current acquisition mode	$\| i_{ch} \|$	20	38.5	60	µA
13	P	Charge pump current tracking mode	$\| i_{ch} \|$	2	3.5	6	µA
14	C	Jitter fit parameter 1[2]	j_1			1.1	%
15	C	Jitter fit parameter 2[2]	j_2			0.13	%

NOTES:
1. % deviation from target frequency
2. f_{REF} = 4MHz, f_{BUS} = 16MHz equivalent f_{VCO} = 32MHz: REFDV = #$03, SYNR = #$0F, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.
3. K_1 is measured with V_{XFC} = 1.4V and V_{XFC} = 1.7V @ VDD5 = 5.25V

A.6 SPI

A.6.1 Master Mode

Figure A-5 and **Figure A-6** illustrate the master mode timing. Timing values are shown in **Table A-17**.



1. If configured as output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-5 SPI Master Timing (CPHA = 0)

Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
34	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	22			ns
35	D	IPIPO[1:0] delay time[1] (PW_{EH}–t_{P1V})	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	22			ns

NOTES:

1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.