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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	99
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12h256vfve

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	07 MAR 2001	03 APR 2001		Initial version.
V01.01	10 MAI 2001	10 MAY 2001		- Minor formal corrections - Changed ATD coupling ratio to10^{-2} - Changed V_{DD5} to 4.5V
V01.02	14 MAY 2001	14 MAY 2001		- Removed 112-pin package references - Changed ATD Electrical Characteristics separate coupling ratio for positive and negative bulk current injection
V01.03	30 MAY 2001	30 MAY 2001		- Reinserted 112-pin package information.
V01.04	11 JUN 2001	11 JUN 2001		- Removed SRSv2 comment from preface - Corrected RESET pin to active low in table 2-1
V01.05	18 JUN 2001	18 JUN 2001		- Adapted style and wording to 9DP256 device user guide - Minor format and wording improvements - Added SRAM data retention disclaimer
V01.06	28 JUN 2001	28 JUN 2001		- Changed Oscillator Characteristics t_{CQOUT} max 2.5s and replaced Clock Monitor Time-out by Clock Monitor Failure Assert Frequency - Changed Self Clock Mode Frequency min 1MHz and max 5.5MHz - Changed I_{DDPS} (RTI and COP disabled) to 400µA - Corrected typo in Figure 2-1 pin 76: PK3 -> PK2
V01.07	12 JUL 2001	12 JUL 2001		- Added t_{EXTR} and t_{EXTF} to Oscillator Characteristics - Added typ value for t_{UPOSC} - Corrected t_{EXTL} and t_{EXTH} values - Updated thermal resistances as per Thermal Simulation Report, July 10, 2001
V01.08	16 JUL 2001	16 JUL 2001		- updated EEPROM size - added DC cutoff capacitor into layout proposals
V01.09	03 AUG 2001	03 AUG 2001		- minor updates
V01.10	29 AUG 2001	29 AUG 2001		- updated electrical spec

Appendix B Package Information

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 is a block diagram of the MC9S12H256 device.

Table 1-1 and **Figure 1-3** show the device memory map of the MC9S12H256.

Table 1-1 Device Memory Map MC9S12H256

Address	Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 – $0019	Reserved	2
$001A – $001B	Device ID register (PARTID)	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	8
$0028 – $002F	CORE (Background Debug Mode)	8
$0030 – $0033	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $006F	Standard Timer Module 16-bit 8 channels (TIM)	48
$0070 – $007F	Reserved	16
$0080 – $00AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
$00B0 – $00BF	Reserved	16
$00C0 – $00C7	Inter Integrated Circuit (IIC)	8
$00C8 – $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 – $00D7	Serial Communications Interface 1 (SCI1)	8
$00D8 – $00DF	Serial Peripheral Interface (SPI)	8
$00E0 – $00FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
$0100 – $010F	Flash control registers	16
$0110 – $011B	EEPROM control registers	12
$011C – $011F	Reserved	4
$0120 – $0137	Liquid Crystal Display Driver 32x4 (LCD)	24
$0140 – $017F	Freescale Scalable Controller Area Network 0 (MSCAN0)	64
$0180 – $01BF	Freescale Scalable Controller Area Network 1 (MSCAN1)	64
$01C0 – $01FF	Motor Control Module (MC)	64
$0200 – $027F	Port Integration Module (PIM)	128
$0280 – $03FF	Reserved	384
$0000 – $0FFF	EEPROM array	4096
$1000 – $3FFF	RAM array	12288
$4000 – $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 – $BFFF	Flash EEPROM Page Window	16384
$C000 – $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 – $FFFF	16384

Table 1-2 Device Memory Map MC9S12H128

Address	Module	Size (Bytes)
$00C8 – $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 – $00D7	Reserved	8
$00D8 – $00DF	Serial Peripheral Interface (SPI)	8
$00E0 – $00FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
$0100 – $010F	Flash control registers	16
$0110 – $011B	EEPROM control registers	12
$011C – $011F	Reserved	4
$0120 – $0137	Liquid Crystal Display Driver 32x4 (LCD)	24
$0140 – $017F	Freescale Scalable Controller Area Network 0 (MSCAN0)	64
$0180 – $01BF	Freescale Scalable Controller Area Network 1 (MSCAN1)	64
$01C0 – $01FF	Motor Control Module (MC)	64
$0200 – $027F	Port Integration Module (PIM)	128
$0280 – $03FF	Reserved	384
$0000 – $07FF	EEPROM array	2048
$1000 – $3FFF	RAM array	12288
$4000 – $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 – $BFFF	Flash EEPROM Page Window	16384
$C000 – $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 – $FFFF	16384

1.5.1 Detailed Register Map

$0000 - $000F MEBI map 1 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0010 - $0014 MMC map 1 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								
$0012	INITEE	Read:	EE15	EE14	EE13	EE12	0	0	0	EEON
		Write:								
$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
$0014	MTST0 Test Only	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0120 - $0137 LCD (Liquid Crystal Display 32 frontplanes, 4 backplanes)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0130	LCDRAM8	Read:	FP17BP3	FP17BP2	FP17BP1	FP17BP0	FP16BP3	FP16BP2	FP16BP1	FP16BP0
		Write:								
$0131	LCDRAM9	Read:	FP19BP3	FP19BP2	FP19BP1	FP19BP0	FP18BP3	FP18BP2	FP18BP1	FP18BP0
		Write:								
$0132	LCDRAM10	Read:	FP21BP3	FP21BP2	FP21BP1	FP21BP0	FP20BP3	FP20BP2	FP20BP1	FP20BP0
		Write:								
$0133	LCDRAM11	Read:	FP23BP3	FP23BP2	FP23BP1	FP23BP0	FP22BP3	FP22BP2	FP22BP1	FP22BP0
		Write:								
$0134	LCDRAM12	Read:	FP25BP3	FP25BP2	FP25BP1	FP25BP0	FP24BP3	FP24BP2	FP24BP1	FP24BP0
		Write:								
$0135	LCDRAM13	Read:	FP27BP3	FP27BP2	FP27BP1	FP27BP0	FP26BP3	FP26BP2	FP26BP1	FP26BP0
		Write:								
$0136	LCDRAM14	Read:	FP29BP3	FP29BP2	FP29BP1	FP29BP0	FP28BP3	FP28BP2	FP28BP1	FP28BP0
		Write:								
$0137	LCDRAM15	Read:	FP31BP3	FP31BP2	FP31BP1	FP31BP0	FP30BP3	FP30BP2	FP30BP1	FP30BP0
		Write:								

$0140 - $017F CAN0 (Freescale Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	CAN0CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0141	CAN0CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0142	CAN0BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
$0143	CAN0BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
$0144	CAN0RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
$0145	CAN0RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
$0146	CAN0TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
$0147	CAN0TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0148	CAN0TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0149	CAN0TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$014A	CAN0TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$014B	CAN0IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$014C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$014E	CAN0RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								

Table 1-3 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0172	Extended ID CAN0TIDR2	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		Write:								
	Standard ID	Read:								
		Write:								
$0173	Extended ID CAN0TIDR3	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		Write:								
	Standard ID	Read:								
		Write:								
$0174-$017B	CAN0TDSR0 - CAN0TDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
$017C	CAN0TDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
$017D	CON0TTBPR	Read:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
		Write:								
$017E	CAN0TTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$017F	CAN0TTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

$0180 - $01BF CAN1 (Freescale Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0180	CAN1CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0181	CAN1CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0182	CAN1BTR0	Read:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Write:								
$0183	CAN1BTR1	Read:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Write:								
$0184	CAN1RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
$0185	CAN1RIER	Read:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		Write:								
$0186	CAN1TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
$0187	CAN1TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0188	CAN1TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0189	CAN1TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$018A	CAN1TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$018B	CAN1IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$018C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$018D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-6** shows the read-only values of these registers. Refer to section Module Mapping and Control (MMC) of HCS12 Core User Guide for further details.

Table 1-6 Memory size registers

Register name	Value
MEMSIZ0	$25
MEMSIZ1	$81

even if it is located in an external slow memory device. The PE6/MODB/IPIPE1 and PE5/MODA/IPIPE0 pins act as high-impedance mode select inputs during reset.

The following paragraphs discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

4.2.1 Normal Operating Modes

These modes provide three operating configurations. Background debug is available in all three modes, but must first be enabled for some operations by means of a BDM background command, then activated.

4.2.1.1 Normal Single-Chip Mode

There is no external expansion bus in this mode. All pins of Ports A, B and E are configured as general purpose I/O pins Port E bits 1 and 0 are available as general purpose input only pins with internal pull-ups enabled. All other pins of Port E are bidirectional I/O pins that are initially configured as high-impedance inputs with internal pull-ups enabled. Ports A and B are configured as high-impedance inputs with their internal pull-ups disabled.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE, and RDWE are reset to zero. Writing the opposite state into them in single chip mode does not change the operation of the associated Port E pins.

In normal single chip mode, the MODE register is writable one time. This allows a user program to change the bus mode to narrow or wide expanded mode and/or turn on visibility of internal accesses.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

4.2.1.2 Normal Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E bit 4 is configured as the E clock output signal. These signals allow external memory and peripheral devices to be interfaced to the MCU.

Port E pins other than PE4/ECLK are configured as general purpose I/O pins (initially high-impedance inputs with internal pull-up resistors enabled). Control bits PIPOE, NECLK, LSTRE, and RDWE in the PEAR register can be used to configure Port E pins to act as bus control outputs instead of general purpose I/O pins.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. Development systems where pipe status signals are monitored would typically use the special variation of this mode.

The Port E bit 2 pin can be reconfigured as the R/$\overline{\text{W}}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded system includes external devices that can be written, such as RAM, the RDWE bit

completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode.

There are two MSCAN modules (CAN0 and CAN1) implemented on the MC9S12H256 device. Consult the MSCAN Block User Guide for information on each MSCAN.

Section 19 PWM Motor Control (MC) Block Description

Consult the MC_10B12C Block User Guide for information about the PWM Motor Control module.

Section 20 Port Integration Module (PIM) Block Description

Consult the PIM_9H256 Block User Guide for information about the Port Integration Module.

Section 21 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

21.1 Device-specific information

21.1.1 VREGEN

There is no VREGEN pin implemented on this device.

21.1.2 Modes of Operation

21.1.2.1 Run Mode

VREG enters run mode whenever the CPU is neither in Stop nor in Pseudo Stop mode. Both regulating loops operate in Run mode with full performance.

21.1.2.2 Standby Mode

VREG enters Standby mode when the CPU operates either in Stop or in Pseudo Stop mode. The supply of the core logic as well as the oscillators are derived from two voltage clamps. Standby mode minimizes quiescent current drawn by the voltage regulator block.

21.1.2.3 Shutdown Mode

VREG Shutdown mode is not available on MC9S12H family devices.

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX1,2 and VDDM1,2,3.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	°C/W
3	T	Thermal Resistance LQFP 144, single sided PCB	θ_{JA}	–	–	45	°C/W
4	T	Thermal Resistance LQFP 144, double sided PCB with 2 internal planes	θ_{JA}	–	–	37	°C/W

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table A-12 NVM Reliability Characteristics

Conditions are shown in **Table A-4** unless otherwise noted					
Num	**C**	**Rating**	**Cycles**	**Data Retention Lifetime**	**Unit**
1	C	Flash/EEPROM (-40˚C to +125˚C)	10	15	Years
2	C	EEPROM (-40˚C to +125˚C)	10,000	5	Years

NOTE: *Flash cycling performance is 10 cycles at -40˚C to +125˚C. Data retention is specified for 15 years.*

NOTE: *EEPROM cycling performance is 10K cycles at -40˚C to 125˚C. Data retention is specified for 5 years on words after cycling 10K times. However if only 10 cycles are executed on a word the data retention is specified for 15 years.*

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-15 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		32	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [2]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}		0.2		ms
10	P	Fitting parameter VCO loop gain[3]	K_1		–120	-224	MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		75		MHz
12	P	Charge pump current acquisition mode	$\| i_{ch} \|$	20	38.5	60	µA
13	P	Charge pump current tracking mode	$\| i_{ch} \|$	2	3.5	6	µA
14	C	Jitter fit parameter 1[2]	j_1			1.1	%
15	C	Jitter fit parameter 2[2]	j_2			0.13	%

NOTES:
1. % deviation from target frequency
2. f_{REF} = 4MHz, f_{BUS} = 16MHz equivalent f_{VCO} = 32MHz: REFDV = #$03, SYNR = #$0F, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.
3. K_1 is measured with V_{XFC} = 1.4V and V_{XFC} = 1.7V @ VDD5 = 5.25V

A.5 MSCAN

Table A-16 MSCAN Wake-up Pulse Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			µs