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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12
Core Size	16-Bit
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12h256vpve

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  - BDM (Background Debug Mode)
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- 8-bit and 4-bit ports with interrupt functionality
  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 128K, 256K Flash EEPROM
  - 2K, 4K byte EEPROM
  - 6K, 12K byte RAM
- Analog-to-Digital Converter
  - 8, 16 channels, 10-bit resolution
  - External conversion trigger capability
- Two 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 2, 6 PWM channels
  - Programmable period and duty cycle
  - 8-bit 2, 6-channel or 16-bit 1, 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Synchronous Serial Peripheral Interface (SPI)

$0020 - $0027 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020 - $0027	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0028 - $002F BKP (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0028	BKPCT0	Read:	BKEN	BKFULL	BKBDM	BKTAG	0	0	0	0
		Write:								
$0029	BKPCT1	Read:	BK0MBH	BK0MBL	BK1MBH	BK1MBL	BK0RWE	BK0RW	BK1RWE	BK1RW
		Write:								
$002A	BKP0X	Read:	0	0	BK0V5	BK0V4	BK0V3	BK0V2	BK0V1	BK0V0
		Write:								
$002B	BKP0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002C	BKP0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$002D	BKP1X	Read:	0	0	BK1V5	BK1V4	BK1V3	BK1V2	BK1V1	BK1V0
		Write:								
$002E	BKP1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002F	BKP1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0030 - $0031 MMC map 4 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0030	PPAGE	Read:	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		Write:								
$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0032 - $0033 MEBI map 3 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0032	PORTK	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0033	DDRK	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0040 - $006F TIM (Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0063	PACNT (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0064	Reserved	Read: Write:								
$0065	Reserved	Read: Write:								
$0066	Reserved	Read: Write:								
$0067	Reserved	Read: Write:								
$0068	Reserved	Read: Write:								
$0069	Reserved	Read: Write:								
$006A	Reserved	Read: Write:								
$006B	Reserved	Read: Write:								
$006C	Reserved	Read: Write:								
$006D	TIMTST Test Only	Read: Write:	0	0	0	0	0	0	TCBYP	PCBYP
$006E	Reserved	Read: Write:								
$006F	Reserved	Read: Write:								

$0070 - $007F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0070 - $007F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATDCTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATDCTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0082	ATDCTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATDCTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATDCTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATDCTL5	Read:	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
		Write:								

$01C0 - $01FF MC (Motor Controller 10bit 12 channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01FD	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01FE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0200	PTT	Read:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		Write:								
$0201	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
$0202	DDRT	Read:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		Write:								
$0203	RDRT	Read:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		Write:								
$0204	PERT	Read:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		Write:								
$0205	PPST	Read:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		Write:								
$0206	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0207	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0208	PTS	Read:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		Write:								
$0209	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
$020A	DDRS	Read:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								
$020B	RDRS	Read:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								
$020C	PERS	Read:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		Write:								
$020D	PPSS	Read:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
$020E	WOMS	Read:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
$020F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0210	PTM	Read:	0	0	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		Write:								
$0211	PTIM	Read:	0	0	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0212	DDRM	Read:	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0213	RDRM	Read:	0	0	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		Write:								
$0214	PERM	Read:	0	0	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		Write:								
$0215	PPSM	Read:	0	0	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		Write:								
$0216	WOMM	Read:	0	0	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		Write:								
$0217	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0218	PTP	Read:	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								
$0219	PTIP	Read:	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$021A	DDRP	Read:	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$021B	RDRP	Read:	0	0	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$021C	PERP	Read:	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$021D	PPSP	Read:	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		Write:								
$021E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$021F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0220	PTH	Read:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0221	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0222	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								
$0223	RDRH	Read:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
		Write:								
$0224	PERH	Read:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		Write:								
$0225	PPSH	Read:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		Write:								
$0226	PIEH	Read:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
		Write:								
$0227	PIFH	Read:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
		Write:								
$0228	PTJ	Read:	0	0	0	0	PTJ3	PTJ2	PTJ1	PTJ0
		Write:								
$0229	PTIJ	Read:	0	0	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
		Write:								
$022A	DDRJ	Read:	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
		Write:								
$022B	RDRJ	Read:	0	0	0	0	RDRJ3	RDRJ2	RDRJ1	RDRJ0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$022C	PERJ	Read:	0	0	0	0	PERJ3	PERJ2	PERJ1	PERJ0
		Write:								
$022D	PPSJ	Read:	0	0	0	0	PPSJ3	PPSJ2	PPSJ1	PPSJ0
		Write:								
$022E	PIEJ	Read:	0	0	0	0	PIEJ3	PIEJ2	PIEJ1	PIEJ0
		Write:								
$022F	PIFJ	Read:	0	0	0	0	PIFJ3	PIFJ2	PIFJ1	PIFJ0
		Write:								
$0230	PTL	Read:	PTL7	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
		Write:								
$0231	PTIL	Read:	PTIL7	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
		Write:								
$0232	DDRL	Read:	DDRL7	DDRL7	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
		Write:								
$0233	RDRL	Read:	RDRL7	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
		Write:								
$0234	PERL	Read:	PERL7	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
		Write:								
$0235	PPSL	Read:	PPSL7	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
		Write:								
$0236	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0237	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0238	PTU	Read:	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		Write:								
$0239	PTIU	Read:	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		Write:								
$023A	DDRU	Read:	DDRU7	DDRU7	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		Write:								
$023B	SRRU	Read:	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
		Write:								
$023C	PERU	Read:	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		Write:								
$023D	PPSU	Read:	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		Write:								
$023E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0240	PTV	Read:	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
		Write:								
$0241	PTIV	Read:	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
		Write:								
$0242	DDRV	Read:	DDRV7	DDRV7	DDRV5	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
		Write:								
$0243	SRRV	Read:	SRRV7	SRRV6	SRRV5	SRRV4	SRRV3	SRRV2	SRRV1	SRRV0
		Write:								
$0244	PERV	Read:	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
		Write:								

2.3.22 FreescalePL[7:4] / FP[31:28] — Port L I/O Pins [7:4]

PL7-PL4 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP31-FP28 of the LCD module.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.23 PL[3:0] / FP[19:16] — Port L I/O Pins [3:0]

PL3-PL0 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP19-FP16 of the LCD module.

2.3.24 PM5 / TXCAN1 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.25 PM4 / RXCAN1 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.26 PM3 / TXCAN0 — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.27 PM2 / RXCAN0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.28 PM1 / SCL — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the serial clock pin SCL of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.29 PM0 / SDA — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the serial data pin SDA of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

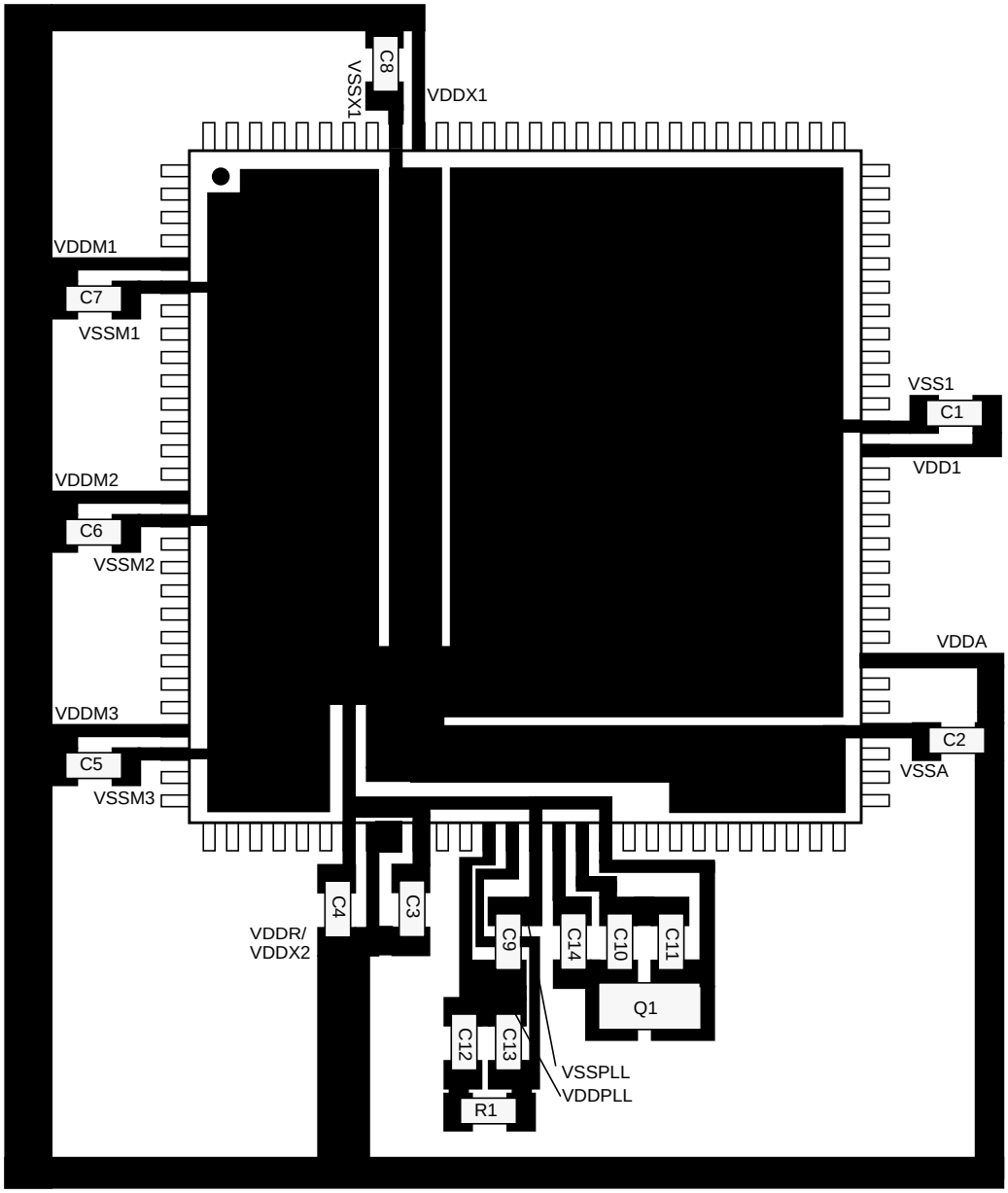
completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode.

21.2 Recommended PCB layout

Figure 21-1 LQFP112 recommended PCB layout



VDD1, VSS1 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX1, VDDX2, VDDM as well as VSSA, VSSX1, VSSX2 and VSSM are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDM, VDDR and VDDX1/2; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX1/2, VDDM and VDDR pins.*
VDD is used for VDD1 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDDPLL.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Ensure external VDD5 load will shunt current greater than maximum injection current. This will be the

A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table A-11** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Burst Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

A.6.2 Slave Mode

Figure A-7 and **Figure A-8** illustrate the slave mode timing. Timing values are shown in **Table A-18**.

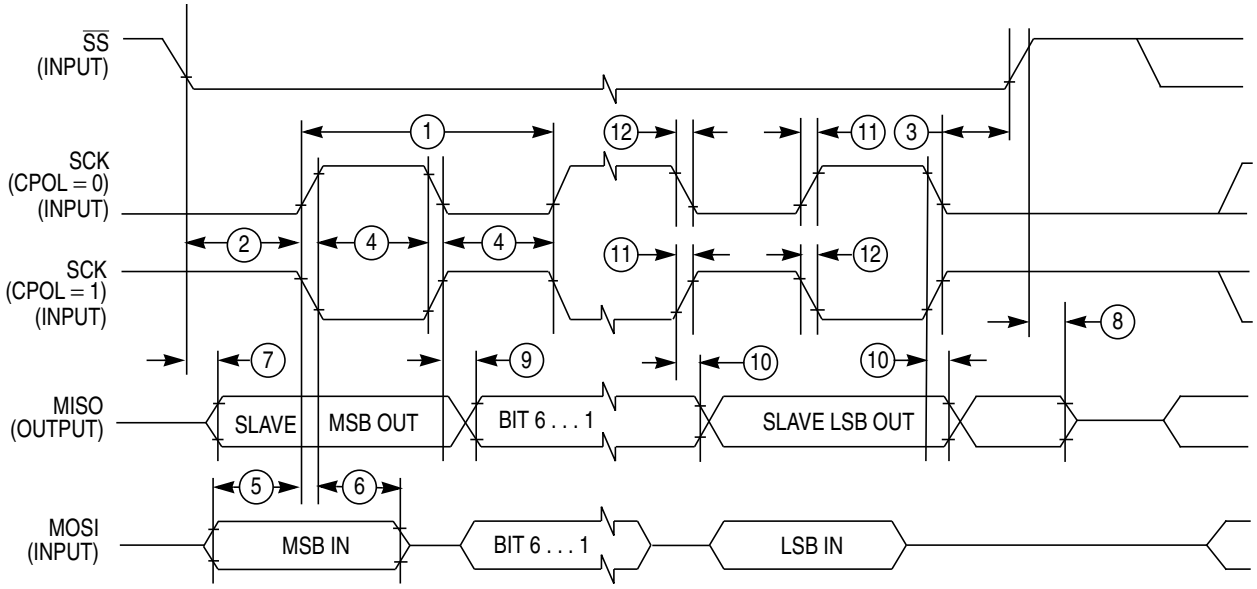


Figure A-7 SPI Slave Timing (CPHA = 0)

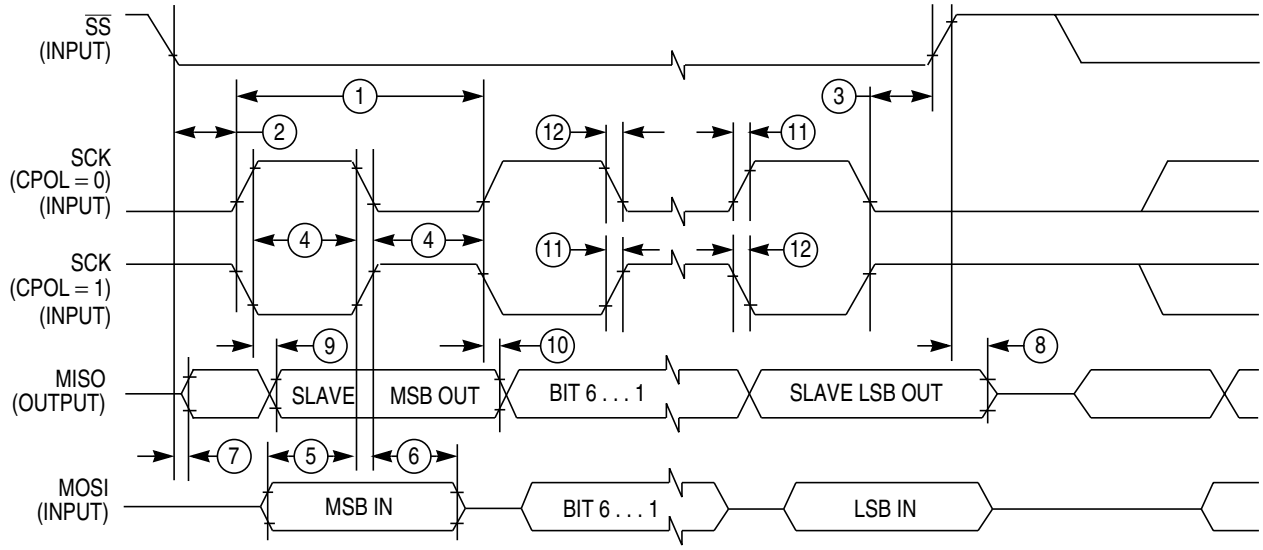


Figure A-8 SPI Slave Timing (CPHA =1)

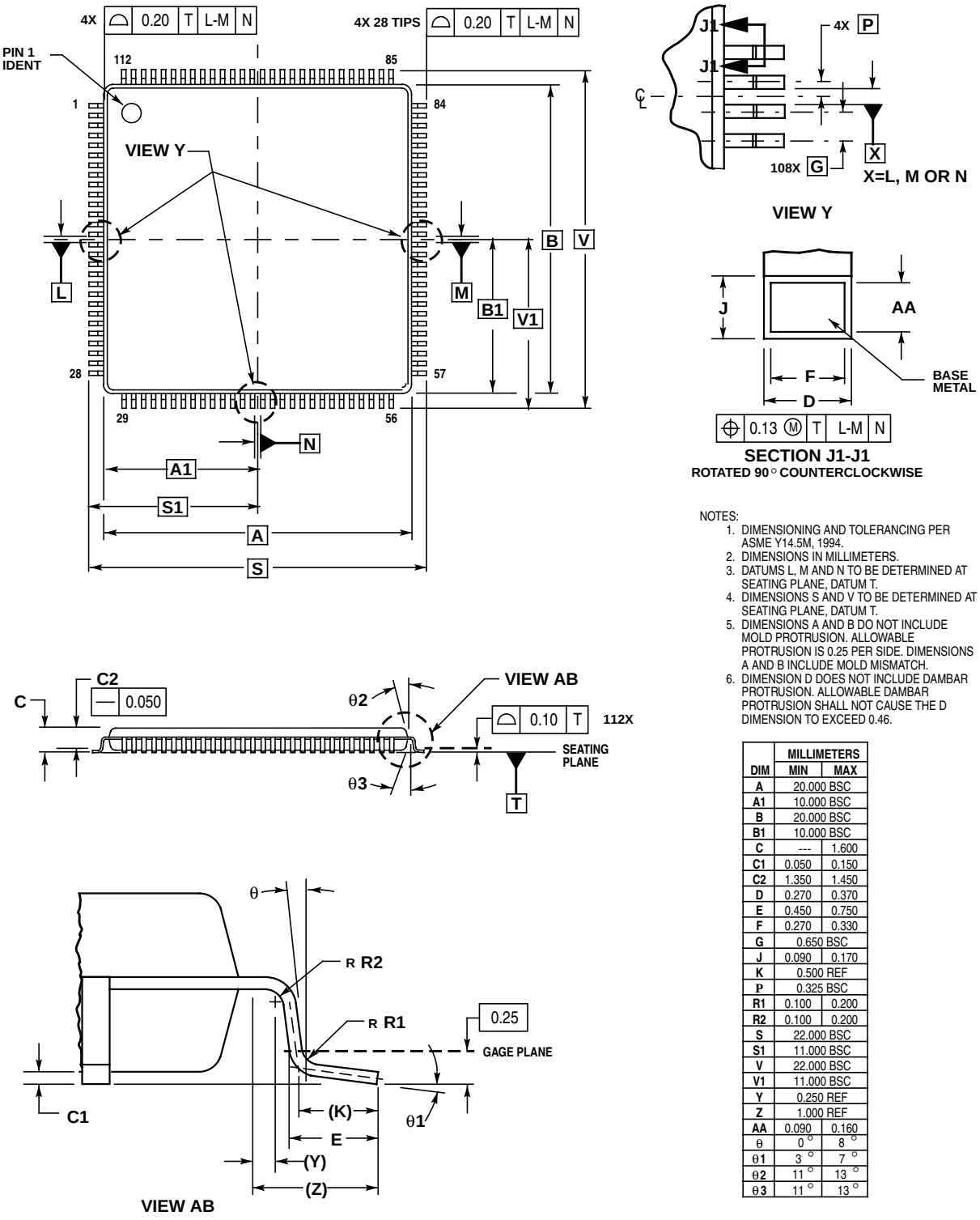
Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
34	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	22			ns
35	D	IPIPO[1:0] delay time[1] (PW_{EH}–t_{P1V})	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	22			ns

NOTES:

1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

B.2 112-pin LQFP package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure B-1 112-pin LQFP mechanical dimensions (case no. 987)