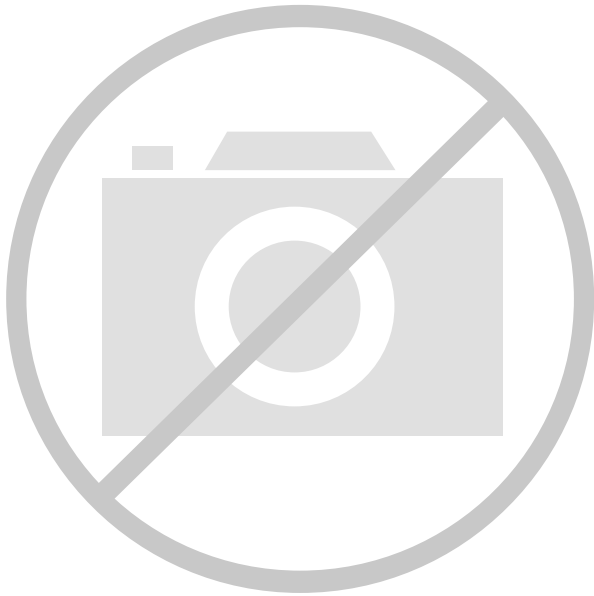




Welcome to [E-XFL.COM](#)

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	100MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t333-100dh

- ◆ 2KB of 2-way set associative data cache, capable of write-back and write-through operation.
- ◆ Cache locking per line to speed real-time systems and critical system functions
- ◆ On-chip TLB to enable multi-tasking in modern operating systems
- ◆ EJTAG interface to enable sophisticated low-cost in-circuit emulation.

Synchronous-DRAM Interface

The RC32333 integrates a SDRAM controller which provides direct control of system SyncDRAM running at speeds to 75MHz.

Key capabilities of the SDRAM controller include:

- ◆ Direct control of 4 banks of SDRAM (up to 2 64-bit wide DIMMs)
- ◆ On-chip page comparators optimize access latency.
- ◆ Speeds to 75MHz
- ◆ Programmable address map.
- ◆ Supports 16, 64, 128, 256, or 512Mb SDRAM devices
- ◆ Automatic refresh generation driven by on-chip timer
- ◆ Support for discrete devices, SODIMM, or DIMM modules.

Thus, systems can take advantage of the full range of commodity memory that is available, enabling system optimization for cost, real-estate, or other attributes.

Local Memory and I/O Controller

The local memory and I/O controller implements direct control of external memory devices, including the boot ROM as well as other memory areas, and also implements direct control of external peripherals.

The local memory controller is highly flexible, allowing a wide range of devices to be directly controlled by the RC32333 processor. For example, a system can be built using an 8-bit boot ROM, 16-bit FLASH cards (possibly on PCMCIA), a 32-bit SRAM or dual-port memory, and a variety of low-cost peripherals.

Key capabilities include:

- ◆ Direct control of EPROM, FLASH, RAM, and dual-port memories
- ◆ 6 chip-select outputs, supporting up to 8MB per memory space
- ◆ Supports mixture of 8-, 16-, and 32-bit wide memory regions
- ◆ Flexible timing protocols allow direct control of a wide variety of devices
- ◆ Programmable address map for 2 chip selects
- ◆ Automatic wait state generation.

PCI Bus Bridge

In order to leverage the wide availability of low-cost peripherals for the PC market as well as to simplify the design of add-in functions, the RC32333 integrates a full 32-bit PCI bus bridge. Key attributes of this bridge include:

- ◆ 50 MHz operation
- ◆ PCI revision 2.2 compliant
- ◆ Programmable address mappings between CPU/Local memory and PCI memory and I/O
- ◆ On-chip PCI arbiter
- ◆ Extensive buffering allows PCI to operate concurrently with local memory transfers
- ◆ Selectable byte-ordering swapper.

On-Chip DMA Controller

To minimize CPU exception handling and maximize the efficiency of system bandwidth, the RC32333 integrates a very sophisticated 4-channel DMA controller on chip.

The RC32333 DMA controller is capable of:

- ◆ Chaining and scatter/gather support through the use of a flexible, linked list of DMA transaction descriptors
- ◆ Capable of memory<->memory, memory<->I/O, and PCI<->memory DMA
- ◆ Unaligned transfer support
- ◆ Byte, halfword, word, quadword DMA support.

On-Chip Peripherals

The RC32333 also integrates peripherals that are common to a wide variety of embedded systems.

- ◆ Single 16550 compatible UART.
- ◆ SPI master mode interface for direct interface to EEPROM, A/D, etc.
- ◆ Interrupt Controller to speed interrupt decode and management
- ◆ Four 32-bit on-chip Timer/Counters
- ◆ Programmable I/O module

Debug Support

To facilitate rapid time to market, the RC32333 provides extensive support for system debug.

First and foremost, this product integrates an EJTAG in-circuit emulation module, allowing a low-cost emulator to interoperate with programs executing on the controller. By using an augmented JTAG interface, the RC32333 is able to reuse the same low-cost emulators developed around the RC32364 CPU.

Name	Type	Reset State Status	Drive Strength Capability	Description
mem_wait_n	Input		—	Memory Wait Negated Requires an external pull-up. SRAM/IO/IOM modes: Allows external wait-states to be injected during the last cycle before data is sampled. DPM (dual-port) mode: Allows dual-port busy signal to restart memory transaction. Alternate function: sdram_wait_n.
mem_245_oe_n	Output	H	Low	Memory FCT245 Output Enable Negated Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank.
mem_245_dt_r_n	Output	Z	High	Memory FCT245 Direction Xmit/Rcv Negated Recommend an external pull-up. Alternate function: cpu_dt_r_n. See CPU Core Specific Signals below.
output_clk	Output	cpu_masterclk	High	Output Clock Optional clock output.

PCI Interface

pci_ad[31:0]	I/O	Z	PCI	PCI Multiplexed Address/Data Bus Address driven by Bus Master during initial frame_n assertion, and then the Data is driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads.
pci_cbe_n[3:0]	I/O	Z	PCI	PCI Multiplexed Command/Byte Enable Bus Command (not negated) Bus driven by the Bus Master during the initial frame_n assertion. Byte Enable Negated Bus driven by the Bus Master during the data phase(s).
pci_par	I/O	Z	PCI	PCI Parity Even parity of the pci_ad[31:0] bus. Driven by Bus Master during Address and Write Data phases. Driven by the Bus Slave during the Read Data phase.
pci_frame_n	I/O	Z	PCI	PCI Frame Negated Driven by the Bus Master. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last datum.
pci_trdy_n	I/O	Z	PCI	PCI Target Ready Negated Driven by the Bus Slave to indicate the current datum can complete.
pci_irdy_n	I/O	Z	PCI	PCI Initiator Ready Negated Driven by the Bus Master to indicate that the current datum can complete.
pci_stop_n	I/O	Z	PCI	PCI Stop Negated Driven by the Bus Slave to terminate the current bus transaction.
pci_idsel_n	Input		—	PCI Initialization Device Select Uses pci_req_n[2] pin. See the PCI subsection.
pci_perr_n	I/O	Z	PCI	PCI Parity Error Negated Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs.
pci_serr_n	I/O Open-collector	Z	PCI	System Error Requires an external pull-up. Driven by any agent to indicate an address parity error, data parity during a Special Cycle command, or any other system error.
pci_clk	Input		—	PCI Clock Clock for PCI Bus transactions. Uses the rising edge for all timing references.
pci_rst_n	Input	L	—	PCI Reset Negated Host mode: Resets all PCI related logic. Satellite mode: Resets all PCI related logic and also warm resets the 32333.
pci_devsel_n	I/O	Z	PCI	PCI Device Select Negated Driven by the target to indicate that the target has decoded the present address as a target address.

Table 1 Pin Descriptions (Part 2 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
pci_req_n[2]	Input	Z	—	PCI Bus Request #2 Negated Requires an external pull-up. Host mode: pci_req_n[2] is an input indicating a request from an external device. Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write. Alternate function: pci_idsel (satellite).
pci_req_n[1]	Input	Z	—	PCI Bus Request #1 Negated Requires external pull-up. Host mode: pci_req_n[1] is an input indicating a request from an external device. Alternate function: Unused (satellite).
pci_req_n[0]	I/O	Z	High	PCI Bus Request #0 Negated Requires an external pull-up for burst mode. Host mode: pci_req_n[0] is an input indicating a request from an external device. Satellite mode: pci_req_n[0] is an output indicating a request from this device.
pci_gnt_n[2]	Output	Z ¹	High	PCI Bus Grant #2 Negated Recommend an external pull-up. Host mode: pci_gnt_n[2] is an output indicating a grant to an external device. Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. External pull-up is required. Alternate function: pci_inta_n (satellite).
pci_gnt_n[1] / pci_eeeprom_cs	I/O	X for 1 pci clock then H ²	High	PCI Bus Grant #1 Negated Recommend external pull-up. Host mode: pci_gnt_n[1] is an output indicating a grant to an external device. Satellite mode: Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32333 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time. 1st Alternate function: pci_eeeprom_cs (satellite). 2nd Alternate function: PIO[7].
pci_gnt_n[0]	I/O	Z	High	PCI Bus Grant #0 Negated Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up. Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Requires external pull-up.
pci_inta_n	Output Open- collec- tor	Z	PCI	PCI Interrupt #A Negated Uses pci_gnt_n[2]. See the PCI subsection.
pci_lock_n	Input		—	PCI Lock Negated Driven by the Bus Master to indicate that an exclusive operation is occurring.
¹ Z in host mode; L in satellite non-boot mode; Z in satellite boot mode. ² H in host mode, L in satellite non-boot and boot modes. X = unknown.				

SDRAM Control Interface

sdram_addr_12	Output	L	High	SDRAM Address Bit 12 and Precharge All SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command.
sdram_ras_n	Output	H	High	SDRAM RAS Negated SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.
sdram_cas_n	Output	H	High	SDRAM CAS Negated SDRAM mode: Provides SDRAM CAS control signal to all SDRAM banks.
sdram_we_n	Output	H	High	SDRAM WE Negated SDRAM mode: Provides SDRAM WE control signal to all SDRAM banks.
sdram_cke	Output	H	High	SDRAM Clock Enable SDRAM mode: Provides clock enable to all SDRAM banks.

Table 1 Pin Descriptions (Part 3 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
sdram_cs_n[3:0]	Output	H	High	SDRAM Chip Select Negated Bus Recommend an external pull-up. SDRAM mode: Provides chip select to each SDRAM bank. SODIMM mode: Provides upper select byte enables [7:4].
sdram_s_n[1:0]	Output	H	High	SDRAM SODIMM Select Negated Bus SDRAM mode: Not used. SDRAM SODIMM mode: Upper and lower chip selects.
sdram_bemask_n[3:0]	Output	H	High	SDRAM Byte Enable Mask Negated Bus (DQM) SDRAM mode: Provides byte enables for each byte lane of all DRAM banks. SODIMM mode: Provides lower select byte enables [3:0].
sdram_245_oe_n	Output	H	Low	SDRAM FCT245 Output Enable Negated Recommend an external pull-up. SDRAM mode: Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank.
sdram_245_dt_r_n	Output	Z	High	SDRAM FCT245 Direction Transmit/Receive Recommend an external pull-up. Uses cpu_dt_r_n. See CPU Core Specific Signals below.

On-Chip Peripherals

dma_ready_n[0]	I/O	Z	Low	DMA Ready Negated Bus Requires an external pull-up. Ready mode: Input pin for general purpose DMA channel 0 that can initiate the next datum in the current DMA descriptor frame. Done mode: Input pin for general purpose DMA channel 0 that can terminate the current DMA descriptor frame. dma_ready_n[0] 1st Alternate function PIO[0]; 2nd Alternate function: dma_done_n[0].
pio[7:0]	I/O	See related pins	Low	Programmable Input/Output General purpose pins that can each can be configured as a general purpose input or general purpose output. These pins are multiplexed with other pin functions: pci_gnt_n[1] (pci_eeprom_cs), spi_mosi, spi_sck, spi_ss_n, spi_miso, uart_rx[0], uart_tx[0], dma_ready_n[0]. Note that pci_gnt_n[1], spi_mosi, spi_sck, and spi_ss_n default to outputs at reset time. The others default to inputs.
uart_rx[0]	I/O	Z	Low	UART Receive Data Bus UART mode: UART channel receive data. uart_rx[0] Alternate function: PIO[2].
uart_tx[0]	I/O	Z	Low	UART Transmit Data Bus Recommend an external pull-up. UART mode: UART channel send data. Note that this pin defaults to an input at reset time and must be programmed via the PIO interface before being used as a UART output. uart_tx[0] Alternate function: PIO[1].
spi_mosi	I/O	L	Low	SPI Data Output Serial mode: Output pin from RC32333 as an Input to a Serial Chip for the Serial data input stream. In PCI satellite mode, acts as an Output pin from RC32333 that connects as an Input to a Serial Chip for the Serial data input stream for loading PCI Configuration Registers in the RC32333 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[6]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeprom_mdo.
spi_miso	I/O	Z	Low	SPI Data Input Serial mode: Input pin to RC32333 from the Output of a Serial Chip for the Serial data output stream. In PCI satellite mode, acts as an Input pin from RC32333 that connects as an output to a Serial Chip for the Serial data output stream for loading PCI Configuration Registers in the RC32333 Reset Initialization Vector PCI boot mode. Defaults to input direction at reset time. 1st Alternate function: PIO[3]. 2nd Alternate function: pci_eeprom_mdi.

Table 1 Pin Descriptions (Part 4 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
spi_sck	I/O	L	Low	SPI Clock Serial mode: Output pin for Serial Clock. In PCI satellite mode, acts as an Output pin for Serial Clock for loading PCI Configuration Registers in the RC323333 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[5]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeeprom_sk.
spi_ss_n	I/O	H	Low	SPI Chip Select Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device. Alternate function: PIO[4]. Defaults to the output direction at reset time.

CPU Core Specific Signals

cpu_nmi_n	Input		—	CPU Non-Maskable Interrupt Requires an external pull-up. This interrupt input is active low to the CPU.
cpu_masterclk	Input		—	CPU Master System Clock Provides the basic system clock.
cpu_int_n[1:0]	Input		—	CPU Interrupt Requires an external pull-up. These interrupt inputs are active low to the CPU.
cpu_coldreset_n	Input	L	—	CPU Cold Reset This active-low signal is asserted to the RC32333 after V_{CC} becomes valid on the initial power-up. The Reset initialization vectors for the RC32333 are latched by cold reset.
cpu_dt_r_n	Output	Z	—	CPU Direction Transmit/Receive This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations. 1st Alternate function: mem_245_dt_r_n. 2nd Alternate function: sdram_245_dt_r_n.

JTAG Interface Signals

jtag_tck	Input		—	JTAG Test Clock Requires an external pull-down. An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.
jtag_tdi, ejtag_dint_n	Input		—	JTAG Test Data In Requires an external pull-up. On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode.
jtag_tdo, ejtag_tpc	Output	Z	High	JTAG Test Data Out The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.
jtag_tms	Input		—	JTAG Test Mode Select Requires an external pull-up. The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.
jtag_trst_n	Input	L	—	JTAG Test Reset When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.
ejtag_dclk	Output	Z	—	EJTAG Test Clock Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.

Table 1 Pin Descriptions (Part 5 of 6)

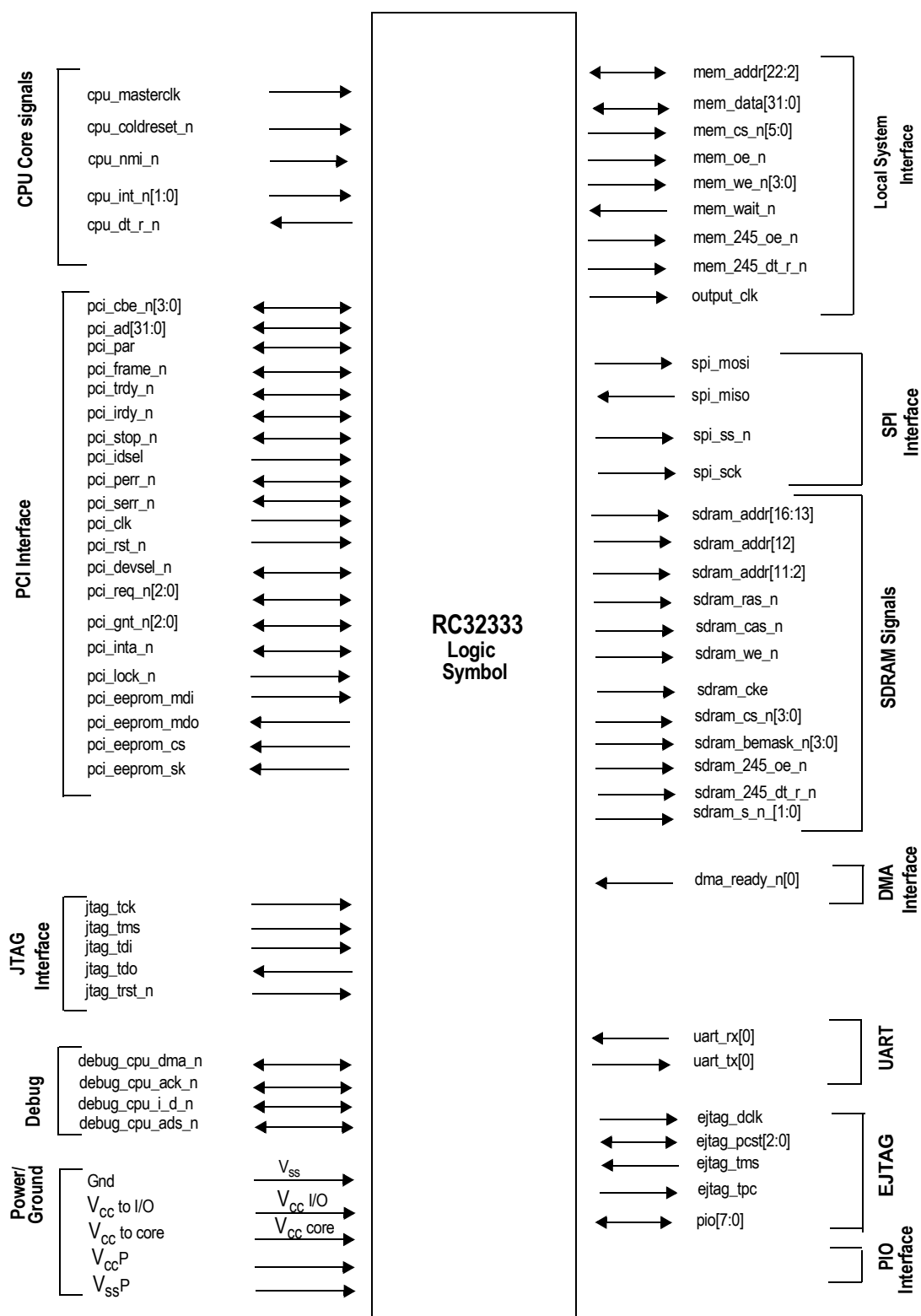
Name	Type	Reset State Status	Drive Strength Capability	Description
ejtag_pcst[2:0]	I/O	Z	Low	EJTAG PC Trace Status Information 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode Alternate function: modebit[2:0].
ejtag_tms	Input		—	EJTAG Test Mode Select Requires an external pull-up. The ejtag_tms is sampled on the rising edge of jtag_tck.

Debug Signals

debug_cpu_dma_n	I/O	Z	Low	Debug CPU versus DMA Negated De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU. Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA. Alternate function: modebit[6].
debug_cpu_ack_n	I/O	Z	Low	Debug CPU Acknowledge Negated Indicates either a data acknowledge to the CPU or DMA. Alternate function: modebit[4].
debug_cpu_ads_n	I/O	Z	Low	Debug CPU Address/Data Strobe Negated Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address. Alternate function: modebit[5].
debug_cpu_i_d_n	I/O	Z	Low	Debug CPU Instruction versus Data Negated Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction. De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction. Alternate function: modebit[3].

Table 1 Pin Descriptions (Part 6 of 6)

Logic Diagram — RC32333



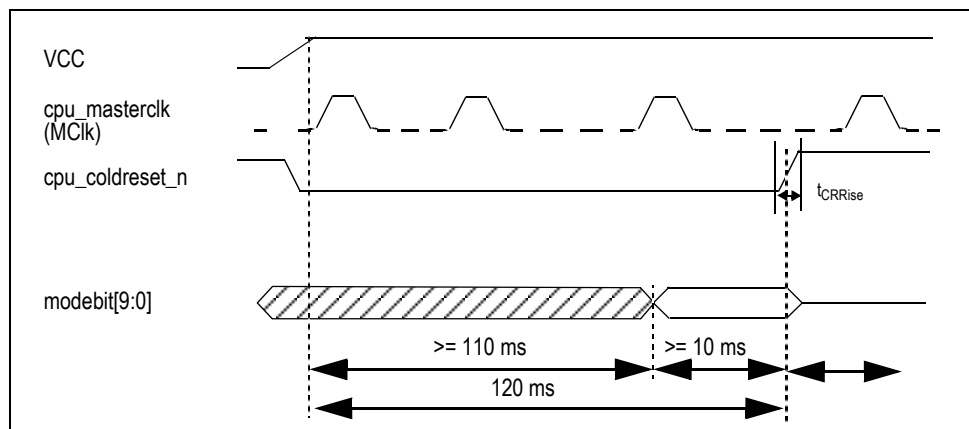
Reset Specification

Figure 3 Mode Configuration Interface Cold Reset Sequence

AC Timing Characteristics — RC32333

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{cc} Core = +3.3V±5%; V_{cc} I/O = +3.3V±5%2.5V version: V_{cc} Core = +2.5V±5%; V_{cc} I/O = +3.3V±5%

Signal	Symbol	Reference Edge	RC32333 ¹ 100MHz		RC32333 ¹ 133MHz		RC32333 ¹ 150MHz		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		

Local System Interface

mem_data[31:0] (data phase)	Tsu2	cpu_masterclk rising	6	—	5	—	4.8	—	ns	Chapter 9, Figures 9.2 and 9.3 Chapter 10, Figures 10.6 through 10.8
mem_data[31:0] (data phase)	Thld2	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	
cpu_dt_r_n	Tdo3	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_data[31:0]	Tdo4	cpu_masterclk rising	—	12	—	10	—	9.3	ns	
mem_data[31:0] output hold time	Tdoh1	cpu_masterclk rising	1	—	1	—	1	—	ns	
mem_data[31:0] (tristate disable time)	Tdz	cpu_masterclk rising	—	12 ²	—	10 ²	—	9.3 ²	ns	
mem_data[31:0] (tristate to data time)	Tzd	cpu_masterclk rising	—	12 ²	—	10 ²	—	9.3 ²	ns	
mem_wait_n	Tsu6	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_wait_n	Thld8	cpu_masterclk rising	1	—	1	—	1	—	ns	
mem_addr[22:2]	Tdo5	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_cs_n[5:0]	Tdo6	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_oe_n, mem_245_oe_n	Tdo7	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_we_n[3:0]	Tdo7a	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_addr[25:2] mem_cs_n[5:0] mem_oe_n, mem_we_n[3:0], mem_245_dt_r_n, mem_245_oe_n	Tdoh3	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	

PCI for 3.3V Device³

pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsels_n, pci_lock_n	Tsu	pci_clk rising	3	—	3	—	3	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_gnt_n[0]	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsels_n, pci_lock_n ⁴	Thld	pci_clk rising	0	—	0	—	0	—	ns	

Table 6 AC Timing Characteristics - RC32333 (Part 1 of 4)

Signal	Symbol	Reference Edge	RC32333 ¹ 100MHz		RC32333 ¹ 133MHz		RC32333 ¹ 150MHz		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdo, pci-eeprom_cs	Tdo	pci_clk rising, pci_eeprom_sk falling	—	15	—	12	—	10	ns	
pci_eeprom_sk	Tdo	pci_clk rising	—	15	—	12	—	10	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
pci_req_n[0], pci_gnt_n[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	

PCI for 2.5V Device³

pci_ad[31:0], pci_par, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n ⁴	Tsu	pci_clk rising	3	—	3	—	3	—	ns	
pci_cbe_n[3:0], pci_frame_n, pci_trdy_n, pci_irdy_n	Tsu	pci_clk rising	4	—	4	—	4	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_gnt_n[0]	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n ⁴	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdo, pci-eeprom_cs	Tdo	pci_clk rising, pci_eeprom_sk falling	—	15	—	12	—	10	ns	
pci_eeprom_sk	Tdo	pci_clk rising	—	15	—	12	—	10	ns	

Table 6 AC Timing Characteristics - RC32333 (Part 2 of 4)

Signal	Symbol	Reference Edge	RC32333 ¹ 100MHz		RC32333 ¹ 133MHz		RC32333 ¹ 150MHz		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
pci_req_n[0], pci_gnt_2[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	

SDRAM Controller

sdram_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	Chapter 11, Figures 11.4 and 11.5
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0], sdram_cke	Tdo9	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_addr_12	Tdo10	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_oe_n	Tdo11	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_dt_r_n	Tdoh4	cpu_masterclk rising	1	—	1	—	1	—	ns	
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0] sdram_cke, sdram_addr_12, sdram_245_oe_n	Tdoh4	cpu_masterclk rising	2.5	—	2.5	—	2.5	—	ns	

DMA

dma_ready_n[0], dma_done_n[0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 13, Figure 13.4
dma_ready_n[0], dma_done_n[0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	

Interrupt Handling

cpu_int_n[1:0], cpu_nmi_n	Tsu9	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 14, Figure 14.12
cpu_int_n[1:0], cpu_nmi_n	Thld13	cpu_masterclk rising	1	—	1	—	1	—	ns	

PIO

PIO[7:0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 15, Figures 15.9 and 15.10
PIO[7:0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[7:6], PIO[4:0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[5]	Tdo19	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[7:6], PIO[4:0]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[5]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	

UARTs

uart_rx[0], uart_tx[0]	Tsu7	cpu_masterclk rising	15	—	12	—	10	—	ns	Chapter 17, Figure 17.16
uart_rx[0], uart_tx[0]	Thld9	cpu_masterclk rising	15	—	12	—	10	—	ns	
uart_rx[0], uart_tx[0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
uart_rx[0], uart_tx[0]	Tdoh8	cpu_masterclk rising	1	—	1	—	1	—	ns	

Table 6 AC Timing Characteristics - RC32333 (Part 3 of 4)

Signal	Symbol	Reference Edge	RC32333 ¹ 100MHz		RC32333 ¹ 133MHz		RC32333 ¹ 150MHz		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Reset										
mem_addr[19:17]	Tsu10	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figures 19.8 and 19.9
mem_addr[19:17]	Thld10	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
mem_addr[22:20]	Tsu22	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_addr[22:20]	Thld22	cpu_masterclk rising	1	—	1	—	1	—	ns	
Debug Interface										
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Tsu20	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figure 19.9 and Chapter 9, Figure 9.2
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Thld20	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdo20	cpu_masterclk rising	—	15	—	12	—	10	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdoh20	cpu_masterclk rising	1	—	1	—	1	—	ns	
JTAG Interface										
jtag_tms, jtag_tdi, jtag_trst_n	t ₅	jtag_tck rising	10	—	10	—	10	—	ns	See Figure 4 below.
jtag_tms, jtag_tdi, jtag_trst_n	t ₆	jtag_tck rising	10	—	10	—	10	—	ns	
jtag_tdo	t ₄	jtag_tck falling	—	10	—	10	—	10	ns	
EJTAG Interface										
ejtag_tms	t ₅	jtag_tclk rising	4	—	4	—	4	—	ns	See Figure 4 below.
ejtag_tms	t ₆	jtag_clk rising	2	—	2	—	2	—	ns	
jtag_tdo Output Delay Time	t _{TDODO} , t ₄	jtag_tck falling	—	6	—	6	—	6	ns	
jtag_tdi Input Setup Time	t _{TDIS} , t ₅	jtag_tck rising	4	—	4	—	4	—	ns	
jtag_tdi Input Hold Time	t _{TDIH} , t ₆	jtag_tck rising	2	—	2	—	2	—	ns	
jtag_trst_n Low Time	t _{TRSTLow} , t ₁₂	—	100	—	100	—	100	—	ns	
jtag_trst_n Removal Time	t _{TRSTR} , t ₁₃	jtag_tck rising	3	—	3	—	3	—	ns	
ejtag_tpc Output Delay Time	t _{TPCDO} , t ₈	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	
ejtag_pcst Output Delay Time	t _{PCSTDO} , t ₇	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	

Table 6 AC Timing Characteristics - RC32333 (Part 4 of 4)

¹. At all pipeline frequencies.². Guaranteed by design.³. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2 at 33MHz.⁴. pci_rst_n is tested per PCI 2.2 as an asynchronous signal.

Standard EJTAG Timing — RC32333

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC3233x User Reference Manual for connector pinout and mechanical specifications.

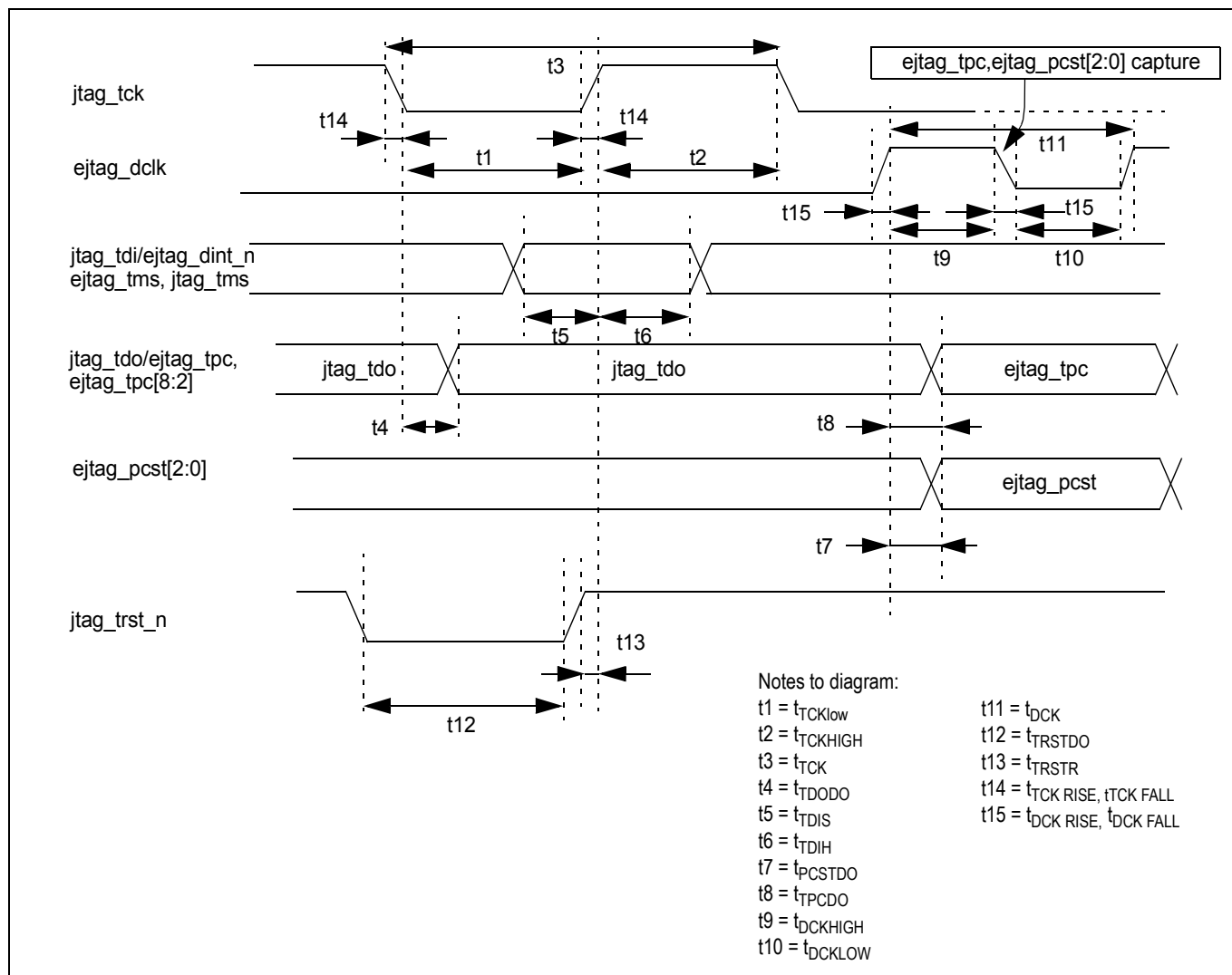
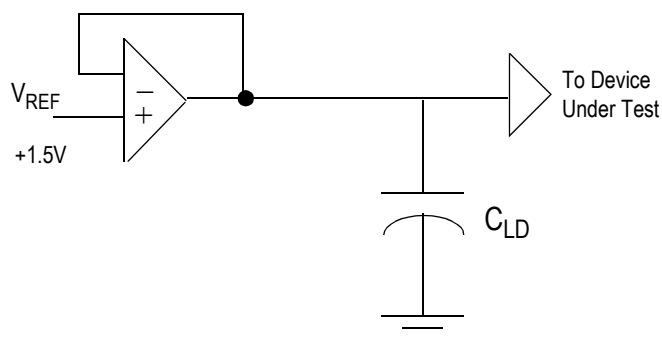


Figure 4 Standard EJTAG Timing

Output Loading for AC Testing



Signal	C _{ld}
All High Drive Signals	50 pF
All Low Drive Signals	25 pF

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

Recommended Operation Temperature and Supply Voltage

3.3V Device

Grade	Ambient Temperature	Gnd	V _{ccIO}	V _{ccCore}	V _{ccP}
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%

Table 7 Temperature and Voltage — 3.3V Device

2.5V Device

Grade	Ambient Temperature	Gnd	V _{ccIO}	V _{ccCore}	V _{ccP}
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%

Table 8 Temperature and Voltage — 2.5V Device

DC Electrical Characteristics — RC32333

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{CC} Core = +3.3V±5%; V_{CC} I/O = +3.3V±5%

2.5V version: V_{CC} Core = +2.5V±5%; V_{CC} I/O = +3.3V±5%

	Parameter	RC32333 ¹		Pin Numbers	Conditions
		Minimum	Maximum		
Input Pads	V_{IL}	—	0.8V	52, 64, 95, 161, 162, 165, 167-170, 191	—
	V_{IH}	2.0V	—		—
LOW Drive Output-Pads	V_{OL}	—	0.4V	41-45, 48, 171, 172, 175, 176, 177-180, 185-190, 195-200, 207, 208	$ I_{OUT} = 6mA$
	V_{OH}	$V_{CC} - 0.4V$	—		$ I_{OUT} = 8mA$
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
HIGH Drive Output Pads	V_{OL}	—	0.4V	1- 5, 8, 13-15, 18-25, 28-35, 38-40, 49-51, 53- 57, 60, 61, 63, 65-67, 70-76, 79, 80, 83-87, 90-94, 153, 154, 156, 159, 166, 194, 201, 204, 205, 206	$ I_{OUT} = 7mA$
	V_{OH}	$V_{CC} - 0.4V$	—		$ I_{OUT} = 16mA$
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
PCI Drive Input Pads	V_{IL}	—	—	123, 155, 157, 158, 160	Per PCI 2.2
	V_{IH}	—	—		
PCI Drive Output pads	V_{OL}	—	—	96, 97, 100-109, 112-119, 122, 124-129, 132-139, 142-149, 152	Per PCI 2.2
	V_{OH}	—	—		
	V_{IL}	—	—		
	V_{IH}	—	—		
All Pads	C_{IN}	—	10pF	All input pads except 155 and 156	—
	C_{IN}^2	5pf	12pF	155	Per PCI 2.2
	C_{IN}^3		8pF	156	Per PCI 2.2
	C_{OUT}	—	10pF	All output pads	—
	I/O_{LEAK}	—	10μA	All non-internal pull-up pins	Input/Output Leakage
	I/O_{LEAK}	—	50μA	All internal pull-up pins	Input/Output Leakage

Table 9 DC Electrical Characteristics - RC32333

¹. At all pipeline frequencies.

². Applies only to pad 155.

³. Applies only to pad 156.

Capacitive Load Deration — RC32333

Refer to the IDT document [79RC32333 IBIS Model](#) which can be found on the company's web site at www.idt.com.

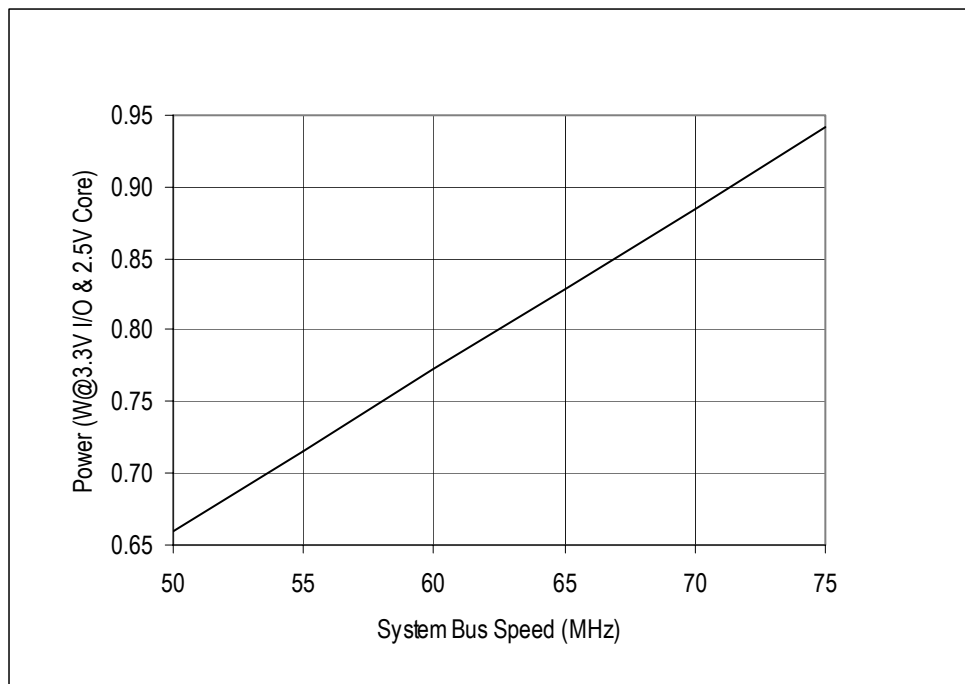


Figure 8 Typical Power Usage — RC32T333 Device

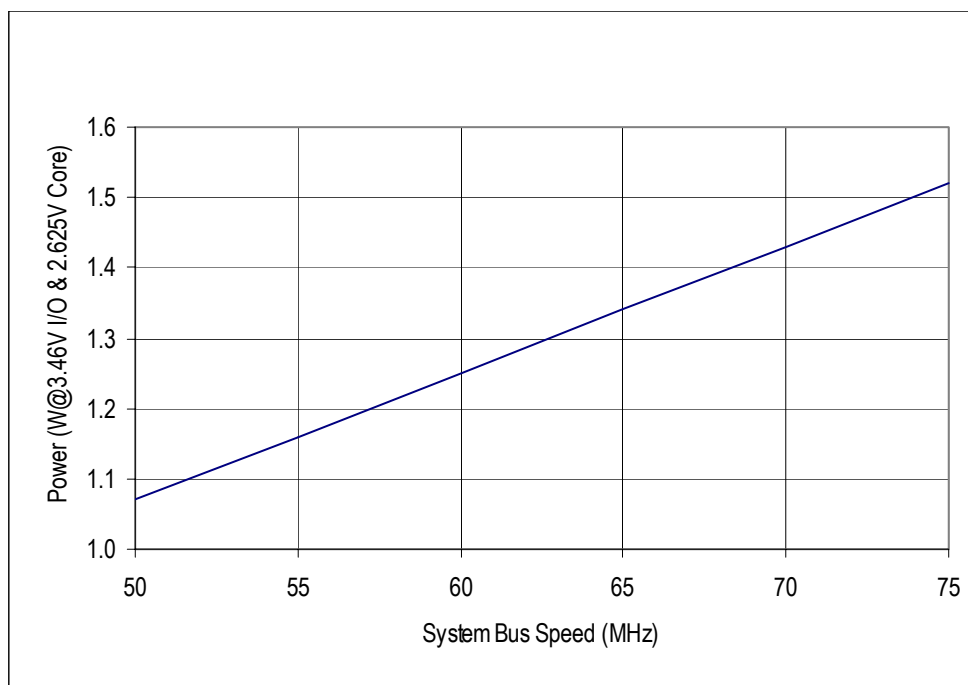


Figure 9 Maximum Power Usage — RC32T333 Device

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
19	mem_addr[6]	1	71	mem_data[29]		123	pci_lock_n		175	ejtag_pcst[2]	1
20	mem_addr[7]	1	72	mem_data[2]		124	pci_stop_n		176	ejtag_dclk	
21	mem_addr[8]	1	73	mem_data[28]		125	pci_devsel_n		177	debug_cpu_i_d_n	1
22	mem_addr[9]	1	74	mem_data[3]		126	pci_trdy_n		178	debug_cpu_ads_n	1
23	mem_addr[10]	1	75	mem_data[27]		127	pci_irdy_n		179	debug_cpu_ack_n	1
24	mem_addr[11]	1	76	mem_data[4]		128	pci_frame_n		180	debug_cpu_dma_n	1
25	output_clk		77	V _{cc} p		129	pci_cbe_n[2]		181	V _{cc} I/O	
26	V _{ss}		78	V _{ss} p		130	V _{ss}		182	V _{ss}	
27	V _{cc} core		79	mem_data[26]		131	V _{cc} core		183	V _{cc} core	
28	mem_addr_12		80	mem_data[5]		132	pci_ad[16]		184	V _{cc} I/O	
29	sdram_addr_12		81	V _{ss}		133	pci_ad[17]		185	spi_ss_n	1
30	sdram_cke		82	V _{cc} core		134	pci_ad[18]		186	spi_sck	2
31	sdram_cs_n[2]		83	cpu_dt_r_n	2	135	pci_ad[19]		187	spi_miso	2
32	sdram_cs_n[3]		84	mem_data[25]		136	pci_ad[20]		188	spi_mosi	2
33	sdram_bemask_n[2]		85	mem_data[6]		137	pci_ad[21]		189	dma_ready_n[0]	2
34	sdram_bemask_n[3]		86	mem_data[24]		138	pci_ad[22]		190	mem_245_oe_n	
35	mem_addr[13]		87	mem_data[7]		139	pci_ad[23]		191	mem_wait_n	2
36	V _{ss}		88	V _{ss}		140	V _{ss}		192	V _{ss}	
37	V _{cc} I/O		89	V _{cc} I/O		141	V _{cc} I/O		193	V _{cc} I/O	
38	mem_addr[14]		90	mem_data[23]		142	pci_cbe_n[3]		194	mem_oe_n	
39	mem_addr[15]	1	91	mem_data[8]		143	pci_ad[24]		195	mem_cs_n[0]	
40	mem_addr[16]	1	92	mem_data[22]		144	pci_ad[25]		196	mem_cs_n[1]	
41	mem_addr[17]	1	93	mem_data[9]		145	pci_ad[26]		197	mem_cs_n[2]	
42	mem_addr[18]	1	94	mem_data[21]		146	pci_ad[27]		198	mem_cs_n[3]	
43	mem_addr[19]	1	95	cpu_nmi_n		147	pci_ad[28]		199	mem_cs_n[4]	
44	mem_addr[20]	1	96	pci_ad[0]		148	pci_ad[29]		200	mem_cs_n[5]	
45	mem_addr[21]	1	97	pci_ad[1]		149	pci_ad[30]		201	mem_we_n[0]	
46	V _{ss}		98	V _{ss}		150	V _{ss}		202	V _{ss}	
47	V _{cc} I/O		99	V _{cc} I/O		151	V _{cc} I/O		203	V _{cc} I/O	
48	mem_addr[22]	1	100	pci_ad[2]		152	pci_ad[31]		204	mem_we_n[1]	
49	mem_data[10]		101	pci_ad[3]		153	pci_req_n[0]		205	mem_we_n[2]	
50	mem_data[11]		102	pci_ad[4]		154	pci_gnt_n[0]		206	mem_we_n[3]	
51	mem_data[20]		103	pci_ad[5]		155	pci_clk		207	uart_tx[0]	1
52	cpu_coldreset_n		104	pci_ad[6]		156	pci_gnt_n[1]	2	208	uart_rx[0]	1

Table 13 RC32333 208-pin QFP Package Pin-Out (Part 2 of 2)



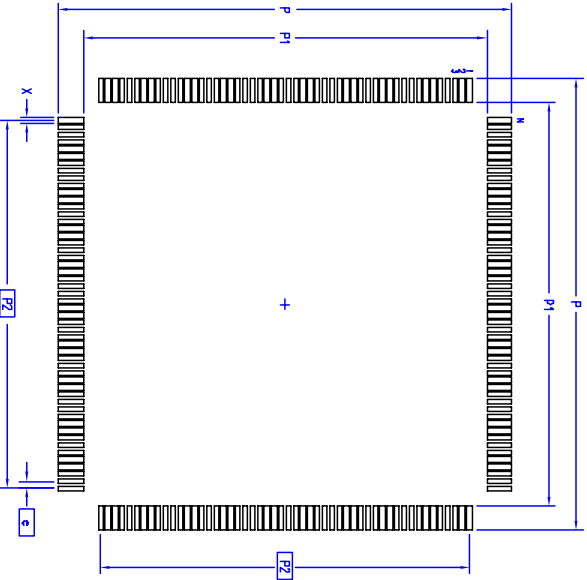
	JEDEC VARIATION			N Q T
	FA-1	MIN	MAX	
M				
B				
L				
A			4.10	
A1				
A2	3.20	3.40	3.60	
D	30.60 BSC			4
D1	28.00 BSC			5.2
E	30.60 BSC			4
E1	28.00 BSC			5.2
N	208			
e	.50 BSC			
b	.17		.27	7
b1	.17		.23	
ddd			.08	

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- DATUMS [A-B] AND [E-F] TO BE DETERMINED AT DATUM PLANE [H]
- DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [C]
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION, ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIIUS OR THE FOOT.
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

REVISIONS			
DCN	REV	DESCRIPTION	DATE
28253	00	INITIAL RELEASE	08/20/96
61478	01	ADD TOP PACKAGE OPTION	09/20/96
61829	02	ADD TOP PACKAGE OPTION	01/20/99

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	.40
X	.50	.50 BSC
N	208	

TOLERANCES			
UNLESS SPECIFIED			
DECIMAL			
FRACTIONAL			
XXX.X			
DATE	08/20/96	TITLE	DS/DH/DR PACKAGE OUTLINE
APPROVALS		DRWING	280 X 280 X 3.4 mm PQFP
ORIGD	02	SIZE	1.30/25 MIN FORM
		SIZE	PSC-4059
		REV	02
DO NOT SCALE DRAWING			
SHEET 2 OF 2			



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