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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32v333-133dhi

Secondly, the RC32333 implements additional reporting signals intended to simplify the task of system debugging when using a logic analyzer. This product allows the logic analyzer to differentiate transactions initiated by DMA from those initiated by the CPU and further allows CPU transactions to be sorted into instruction fetches vs. data fetches.

Finally, the RC32333 implements a full boundary scan capability, allowing board manufacturing diagnostics and debug.

Packaging

The RC32333 is packaged using a 208 Quad Flat Pack (QFP) package.

Thermal Considerations

The RC32333 consumes less than 2.0 W peak power. The device is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices; -40° to +85° C for industrial temperature devices.

Revision History

March 5, 2003: Initial publication of 2.5V Revision X silicon.

September 2, 2003: Added 2.5V version of device. Changed tables to include 2.5V values where appropriate. Added a Power Consumption table, Temperature and Voltage table, and Power Curves for the 2.5V device. In the PCI category of Table 6, created separate sections for 3.3V and 2.5V devices and in 2.5V section changed time to 4 ns for pci_cbe_n[3:0], pci_frame_n, pci_trdy_n, and pci_irdy_n. In Table 8, added 3 new categories (Input Pads, PCI Input Pads, and All Pads) and added footnotes 2 and 3. In Table 13, pins 181 and 184 were changed from Vcc Core to Vcc I/O.

March 24, 2004: In Table 1, changed description in Satellite Mode for pci_rst_n. Specified "cold" reset on pages 12 and 13. Changed several values in Table 12, Absolute Maximum Ratings, and changed footnote 1 to that table.

May 4, 2004: Revised values in Table 11, Power Consumption — 2.5V Device.

Name	Type	Reset State Status	Drive Strength Capability	Description
mem_wait_n	Input		—	**Memory Wait Negated** Requires an external pull-up. SRAM/IOI/IOM modes: Allows external wait-states to be injected during the last cycle before data is sampled. DPM (dual-port) mode: Allows dual-port busy signal to restart memory transaction. Alternate function: sdram_wait_n.
mem_245_oe_n	Output	H	Low	**Memory FCT245 Output Enable Negated** Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank.
mem_245_dt_r_n	Output	Z	High	**Memory FCT245 Direction Xmit/Rcv Negated** Recommend an external pull-up. Alternate function: cpu_dt_r_n. See CPU Core Specific Signals below.
output_clk	Output	cpu_masterclk	High	**Output Clock** Optional clock output.
PCI Interface				
pci_ad[31:0]	I/O	Z	PCI	**PCI Multiplexed Address/Data Bus** Address driven by Bus Master during initial frame_n assertion, and then the Data is driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads.
pci_cbe_n[3:0]	I/O	Z	PCI	**PCI Multiplexed Command/Byte Enable Bus** Command (not negated) Bus driven by the Bus Master during the initial frame_n assertion. Byte Enable Negated Bus driven by the Bus Master during the data phase(s).
pci_par	I/O	Z	PCI	**PCI Parity** Even parity of the pci_ad[31:0] bus. Driven by Bus Master during Address and Write Data phases. Driven by the Bus Slave during the Read Data phase.
pci_frame_n	I/O	Z	PCI	**PCI Frame Negated** Driven by the Bus Master. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last datum.
pci_trdy_n	I/O	Z	PCI	**PCI Target Ready Negated** Driven by the Bus Slave to indicate the current datum can complete.
pci_irdy_n	I/O	Z	PCI	**PCI Initiator Ready Negated** Driven by the Bus Master to indicate that the current datum can complete.
pci_stop_n	I/O	Z	PCI	**PCI Stop Negated** Driven by the Bus Slave to terminate the current bus transaction.
pci_idsel_n	Input		—	**PCI Initialization Device Select** Uses pci_req_n[2] pin. See the PCI subsection.
pci_perr_n	I/O	Z	PCI	**PCI Parity Error Negated** Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs.
pci_serr_n	I/O Open-collector	Z	PCI	**System Error** Requires an external pull-up. Driven by any agent to indicate an address parity error, data parity during a Special Cycle command, or any other system error.
pci_clk	Input		—	**PCI Clock** Clock for PCI Bus transactions. Uses the rising edge for all timing references.
pci_rst_n	Input	L	—	**PCI Reset Negated** Host mode: Resets all PCI related logic. Satellite mode: Resets all PCI related logic and also warm resets the 32333.
pci_devsel_n	I/O	Z	PCI	**PCI Device Select Negated** Driven by the target to indicate that the target has decoded the present address as a target address.

Table 1 Pin Descriptions (Part 2 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
pci_req_n[2]	Input	Z	—	**PCI Bus Request #2 Negated** Requires an external pull-up. Host mode: pci_req_n[2] is an input indicating a request from an external device. Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write. Alternate function: pci_idsel (satellite).
pci_req_n[1]	Input	Z	—	**PCI Bus Request #1 Negated** Requires external pull-up. Host mode: pci_req_n[1] is an input indicating a request from an external device. Alternate function: Unused (satellite).
pci_req_n[0]	I/O	Z	High	**PCI Bus Request #0 Negated** Requires an external pull-up for burst mode. Host mode: pci_req_n[0] is an input indicating a request from an external device. Satellite mode: pci_req_n[0] is an output indicating a request from this device.
pci_gnt_n[2]	Output	Z[1]	High	**PCI Bus Grant #2 Negated** Recommend an external pull-up. Host mode: pci_gnt_n[2] is an output indicating a grant to an external device. Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. External pull-up is required. Alternate function: pci_inta_n (satellite).
pci_gnt_n[1] / pci_eeprom_cs	I/O	X for 1 pci clock then H[2]	High	**PCI Bus Grant #1 Negated** Recommend external pull-up. Host mode: pci_gnt_n[1] is an output indicating a grant to an external device. Satellite mode: Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32333 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time. 1st Alternate function: pci_eeprom_cs (satellite). 2nd Alternate function: PIO[7].
pci_gnt_n[0]	I/O	Z	High	**PCI Bus Grant #0 Negated** Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up. Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Requires external pull-up.
pci_inta_n	Output Open-collector	Z	PCI	**PCI Interrupt #A Negated** Uses pci_gnt_n[2]. See the PCI subsection.
pci_lock_n	Input		—	**PCI Lock Negated** Driven by the Bus Master to indicate that an exclusive operation is occurring.

[1] Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.
[2] H in host mode, L in satellite non-boot and boot modes. X = unknown.

SDRAM Control Interface

Name	Type	Reset State Status	Drive Strength Capability	Description
sdram_addr_12	Output	L	High	**SDRAM Address Bit 12 and Precharge All** SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command.
sdram_ras_n	Output	H	High	**SDRAM RAS Negated** SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.
sdram_cas_n	Output	H	High	**SDRAM CAS Negated** SDRAM mode: Provides SDRAM CAS control signal to all SDRAM banks.
sdram_we_n	Output	H	High	**SDRAM WE Negated** SDRAM mode: Provides SDRAM WE control signal to all SDRAM banks.
sdram_cke	Output	H	High	**SDRAM Clock Enable** SDRAM mode: Provides clock enable to all SDRAM banks.

Table 1 Pin Descriptions (Part 3 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
sdram_cs_n[3:0]	Output	H	High	**SDRAM Chip Select Negated Bus** Recommend an external pull-up. SDRAM mode: Provides chip select to each SDRAM bank. SODIMM mode: Provides upper select byte enables [7:4].
sdram_s_n[1:0]	Output	H	High	**SDRAM SODIMM Select Negated Bus** SDRAM mode: Not used. SDRAM SODIMM mode: Upper and lower chip selects.
sdram_bemask_n [3:0]	Output	H	High	**SDRAM Byte Enable Mask Negated Bus (DQM)** SDRAM mode: Provides byte enables for each byte lane of all DRAM banks. SODIMM mode: Provides lower select byte enables [3:0].
sdram_245_oe_n	Output	H	Low	**SDRAM FCT245 Output Enable Negated** Recommend an external pull-up. SDRAM mode: Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank.
sdram_245_dt_r_n	Output	Z	High	**SDRAM FCT245 Direction Transmit/Receive** Recommend an external pull-up. Uses cpu_dt_r_n. See CPU Core Specific Signals below.
On-Chip Peripherals				
dma_ready_n[0]	I/O	Z	Low	**DMA Ready Negated Bus** Requires an external pull-up. Ready mode: Input pin for general purpose DMA channel 0 that can initiate the next datum in the current DMA descriptor frame. Done mode: Input pin for general purpose DMA channel 0 that can terminate the current DMA descriptor frame. dma_ready_n[0] 1st Alternate function PIO[0]; 2nd Alternate function: dma_done_n[0].
pio[7:0]	I/O	See related pins	Low	**Programmable Input/Output** General purpose pins that can each can be configured as a general purpose input or general purpose output. These pins are multiplexed with other pin functions: pci_gnt_n[1] (pci_eeprom_cs), spi_mosi, spi_sck, spi_ss_n, spi_miso, uart_rx[0], uart_tx[0], dma_ready_n[0]. Note that pci_gnt_n[1], spi_mosi, spi_sck, and spi_ss_n default to outputs at reset time. The others default to inputs.
uart_rx[0]	I/O	Z	Low	**UART Receive Data Bus** UART mode: UART channel receive data. uart_rx[0] Alternate function: PIO[2].
uart_tx[0]	I/O	Z	Low	**UART Transmit Data Bus** Recommend an external pull-up. UART mode: UART channel send data. Note that this pin defaults to an input at reset time and must be programmed via the PIO interface before being used as a UART output. uart_tx[0] Alternate function: PIO[1].
spi_mosi	I/O	L	Low	**SPI Data Output** Serial mode: Output pin from RC32333 as an Input to a Serial Chip for the Serial data input stream. In PCI satellite mode, acts as an Output pin from RC32333 that connects as an Input to a Serial Chip for the Serial data input stream for loading PCI Configuration Registers in the RC32333 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[6]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeprom_mdo.
spi_miso	I/O	Z	Low	**SPI Data Input** Serial mode: Input pin to RC32333 from the Output of a Serial Chip for the Serial data output stream. In PCI satellite mode, acts as an Input pin from RC32333 that connects as an output to a Serial Chip for the Serial data output stream for loading PCI Configuration Registers in the RC32333 Reset Initialization Vector PCI boot mode. Defaults to input direction at reset time. 1st Alternate function: PIO[3]. 2nd Alternate function: pci_eeprom_mdi.

Table 1 Pin Descriptions (Part 4 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
spi_sck	I/O	L	Low	**SPI Clock** Serial mode: Output pin for Serial Clock. In PCI satellite mode, acts as an Output pin for Serial Clock for loading PCI Configuration Registers in the RC323333 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[5]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeprom_sk.
spi_ss_n	I/O	H	Low	**SPI Chip Select** Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device. Alternate function: PIO[4]. Defaults to the output direction at reset time.
CPU Core Specific Signals				
cpu_nmi_n	Input		—	**CPU Non-Maskable Interrupt** Requires an external pull-up. This interrupt input is active low to the CPU.
cpu_masterclk	Input		—	**CPU Master System Clock** Provides the basic system clock.
cpu_int_n[1:0]	Input		—	**CPU Interrupt** Requires an external pull-up. These interrupt inputs are active low to the CPU.
cpu_coldreset_n	Input	L	—	**CPU Cold Reset** This active-low signal is asserted to the RC32333 after V_{CC} becomes valid on the initial power-up. The Reset initialization vectors for the RC32333 are latched by cold reset.
cpu_dt_r_n	Output	Z	—	**CPU Direction Transmit/Receive** This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations. 1st Alternate function: mem_245_dt_r_n. 2nd Alternate function: sdram_245_dt_r_n.
JTAG Interface Signals				
jtag_tck	Input		—	**JTAG Test Clock** Requires an external pull-down. An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.
jtag_tdi, ejtag_dint_n	Input		—	**JTAG Test Data In** Requires an external pull-up. On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode.
jtag_tdo, ejtag_tpc	Output	Z	High	**JTAG Test Data Out** The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.
jtag_tms	Input		—	**JTAG Test Mode Select** Requires an external pull-up. The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.
jtag_trst_n	Input	L	—	**JTAG Test Reset** When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.
ejtag_dclk	Output	Z	—	**EJTAG Test Clock** Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.

Table 1 Pin Descriptions (Part 5 of 6)

Name	Type	Reset State Status	Drive Strength Capability	Description
ejtag_pcst[2:0]	I/O	Z	Low	**EJTAG PC Trace Status Information** 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode Alternate function: modebit[2:0].
ejtag_tms	Input		—	**EJTAG Test Mode Select** Requires an external pull-up. The ejtag_tms is sampled on the rising edge of jtag_tck.
Debug Signals				
debug_cpu_dma_n	I/O	Z	Low	**Debug CPU versus DMA Negated** De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU. Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA. Alternate function: modebit[6].
debug_cpu_ack_n	I/O	Z	Low	**Debug CPU Acknowledge Negated** Indicates either a data acknowledge to the CPU or DMA. Alternate function: modebit[4].
debug_cpu_ads_n	I/O	Z	Low	**Debug CPU Address/Data Strobe Negated** Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address. Alternate function: modebit[5].
debug_cpu_i_d_n	I/O	Z	Low	**Debug CPU Instruction versus Data Negated** Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction. De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction. Alternate function: modebit[3].

Table 1 Pin Descriptions (Part 6 of 6)

pci_host_mode Settings

During cold reset initialization, the RC32333's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32333's PCI configuration registers, including the read-only registers. If the RC32333's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

Pin	Reset Boot Mode	Description	Value	Mode Settings
mem_addr[20]	PCI host mode	PCI is in satellite mode	1	PCI_satellite
		PCI is in host mode (typical system)	0	PCI_host

Table 4 RC32333 pci_host_mode Initialization Settings

Clock Parameters — RC32333

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{cc} Core = +3.3V±5%; V_{cc} I/O = +3.3V±5%

2.5V version: V_{cc} Core = +2.5V±5%; V_{cc} I/O = +3.3V±5%

Parameter	Symbol	Test Conditions	RC32333 100MHz		RC32333 133MHz		RC32333 150MHz		Units
			Min	Max	Min	Max	Min	Max	
cpu_masterclock HIGH	t_{MCHIGH}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock LOW	t_{MCLOW}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock period[1] - 3.3V ver.	t_{MCP}	—	20	66.6	15	66.6	13.33	66.6	ns
cpu_masterclock period[1] - 2.5V ver.	t_{MCP}	—	20	40.0	15	40.0	13.33	40.0	ns
cpu_masterclock Rise & Fall Time[2]	t_{MCRise}, t_{MCFall}	—	—	3	—	3	—	3	ns
cpu_masterclock Jitter	t_{JITTER}	—	—	± 250	—	± 250	—	± 200	ps
pci_clk Rise & Fall Time	t_{PCRise}, t_{PCFall}	PCI 2.2	—	1.6	—	1.6	—	1.6	ns
pci_clk Period[1]	t_{PCP}		20	—	20	—	20	—	ns
jtag_tck Rise & Fall Time	t_{JCRise}, t_{JCFall}	—	—	5	—	5	—	5	ns
ejtag_dck period	t_{DCK}, t_{11}		10	—	10	—	10	—	ns
jtag_tck clock period	t_{TCK}, t_3		100	—	100	—	100	—	ns
ejtag_dclk High, Low Time	$t_{DCK\ High}$, t_9 $t_{DCK\ Low}$, t_{10}		4	—	4	—	4	—	ns
ejtag_dclk Rise, Fall Time	$t_{DCK\ Rise}$, t_9 $t_{DCK\ Fall}$, t_{10}		—	1	—	1	—	1	ns
output_clk[3]	t_{DO}21		N/A	N/A	N/A	N/A	N/A	N/A	—
cpu_coldreset_n Asserted during power-up		power-on sequence	120	—	120	—	120	—	ms
cpu_coldreset_n Rise Time	t_{CRRise}		—	5	—	5	—	5	ns

Table 5 Clock Parameters - RC32333

1. cpu_masterclock frequency should never be below pci_clk frequency if PCI interface is used.

2. Rise and Fall times are measured between 10% and 90%.

3. Output_clk should not be used in a system. Only the cpu_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC3233x systems. Refer to the RC3233x Device Errata for more information.

Signal	Symbol	Reference Edge	RC32333[1] 100MHz		RC32333[1] 133MHz		RC32333[1] 150MHz		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdo, pci-eeprom_cs	Tdo	pci_clk rising, pci_eeprom_sk falling	—	15	—	12	—	10	ns	
pci_eeprom_sk	Tdo	pci_clk rising	—	15	—	12	—	10	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
pci_req_n[0], pci_gnt_[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
PCI for 2.5V Device[3]										
pci_ad[31:0], pci_par, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[4]	Tsu	pci_clk rising	3	—	3	—	3	—	ns	
pci_cbe_n[3:0], pci_frame_n, pci_trdy_n, pci_irdy_n	Tsu	pci_clk rising	4	—	4	—	4	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_gnt_n[0]	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[4]	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdo, pci-eeprom_cs	Tdo	pci_clk rising, pci_eeprom_sk falling	—	15	—	12	—	10	ns	
pci_eeprom_sk	Tdo	pci_clk rising	—	15	—	12	—	10	ns	

Table 6 AC Timing Characteristics - RC32333 (Part 2 of 4)

Signal	Symbol	Reference Edge	RC32333[1] 100MHz		RC32333[1] 133MHz		RC32333[1] 150MHz		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
pci_req_n[0], pci_gnt_[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n	Tdo	pci_clk rising	2	7.5	2	7.5	2	7.5	ns	
SDRAM Controller										
sdram_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	Chapter 11, Figures 11.4 and 11.5
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0], sdram_cke	Tdo9	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_addr_12	Tdo10	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_oe_n	Tdo11	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_dt_r_n	Tdoh4	cpu_masterclk rising	1	—	1	—	1	—	ns	
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0] sdram_cke, sdram_addr_12, sdram_245_oe_n	Tdoh4	cpu_masterclk rising	2.5	—	2.5	—	2.5	—	ns	
DMA										
dma_ready_n[0], dma_done_n[0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 13, Figure 13.4
dma_ready_n[0], dma_done_n[0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	
Interrupt Handling										
cpu_int_n[1:0], cpu_nmi_n	Tsu9	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 14, Figure 14.12
cpu_int_n[1:0], cpu_nmi_n	Thld13	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO										
PIO[7:0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 15, Figures 15.9 and 15.10
PIO[7:0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[7:6], PIO[4:0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[5]	Tdo19	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[7:6], PIO[4:0]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[5]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	
UARTs										
uart_rx[0], uart_tx[0]	Tsu7	cpu_masterclk rising	15	—	12	—	10	—	ns	Chapter 17, Figure 17.16
uart_rx[0], uart_tx[0]	Thld9	cpu_masterclk rising	15	—	12	—	10	—	ns	
uart_rx[0], uart_tx[0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
uart_rx[0], uart_tx[0]	Tdoh8	cpu_masterclk rising	1	—	1	—	1	—	ns	

Table 6 AC Timing Characteristics - RC32333 (Part 3 of 4)

Signal	Symbol	Reference Edge	RC32333[1] 100MHz		RC32333[1] 133MHz		RC32333[1] 150MHz		Units	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Reset										
mem_addr[19:17]	Tsu10	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figures 19.8 and 19.9
mem_addr[19:17]	Thld10	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
mem_addr[22:20]	Tsu22	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_addr[22:20]	Thld22	cpu_masterclk rising	1	—	1	—	1	—	ns	
Debug Interface										
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Tsu20	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figure 19.9 and Chapter 9, Figure 9.2
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Thld20	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdo20	cpu_masterclk rising	—	15	—	12	—	10	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdoh20	cpu_masterclk rising	1	—	1	—	1	—	ns	
JTAG Interface										
jtag_tms, jtag_tdi, jtag_trst_n	t_5	jtag_tck rising	10	—	10	—	10	—	ns	See Figure 4 below.
jtag_tms, jtag_tdi, jtag_trst_n	t_6	jtag_tck rising	10	—	10	—	10	—	ns	
jtag_tdo	t_4	jtag_tck falling	—	10	—	10	—	10	ns	
EJTAG Interface										
ejtag_tms	t_5	jtag_tclk rising	4	—	4	—	4	—	ns	See Figure 4 below.
ejtag_tms	t_6	jtag_clk rising	2	—	2	—	2	—	ns	
jtag_tdo Output Delay Time	t_{TDODO}, t_4	jtag_tck falling	—	6	—	6	—	6	ns	
jtag_tdi Input Setup Time	t_{TDIS}, t_5	jtag_tck rising	4	—	4	—	4	—	ns	
jtag_tdi Input Hold Time	t_{TDIH}, t_6	jtag_tck rising	2	—	2	—	2	—	ns	
jtag_trst_n Low Time	$t_{TRSTLow}$, t_{12}	—	100	—	100	—	100	—	ns	
jtag_trst_n Removal Time	t_{TRSTR}, t_{13}	jtag_tck rising	3	—	3	—	3	—	ns	
ejtag_tpc Output Delay Time	t_{TPCDO}, t_8	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	
ejtag_pcst Output Delay Time	t_{PCSTDO}, t_7	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	

Table 6 AC Timing Characteristics - RC32333 (Part 4 of 4)

1. At all pipeline frequencies.
2. Guaranteed by design.
3. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2 at 33MHz.
4. pci_rst_n is tested per PCI 2.2 as an asynchronous signal.

Standard EJTAG Timing — RC32333

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC3233x User Reference Manual for connector pinout and mechanical specifications.

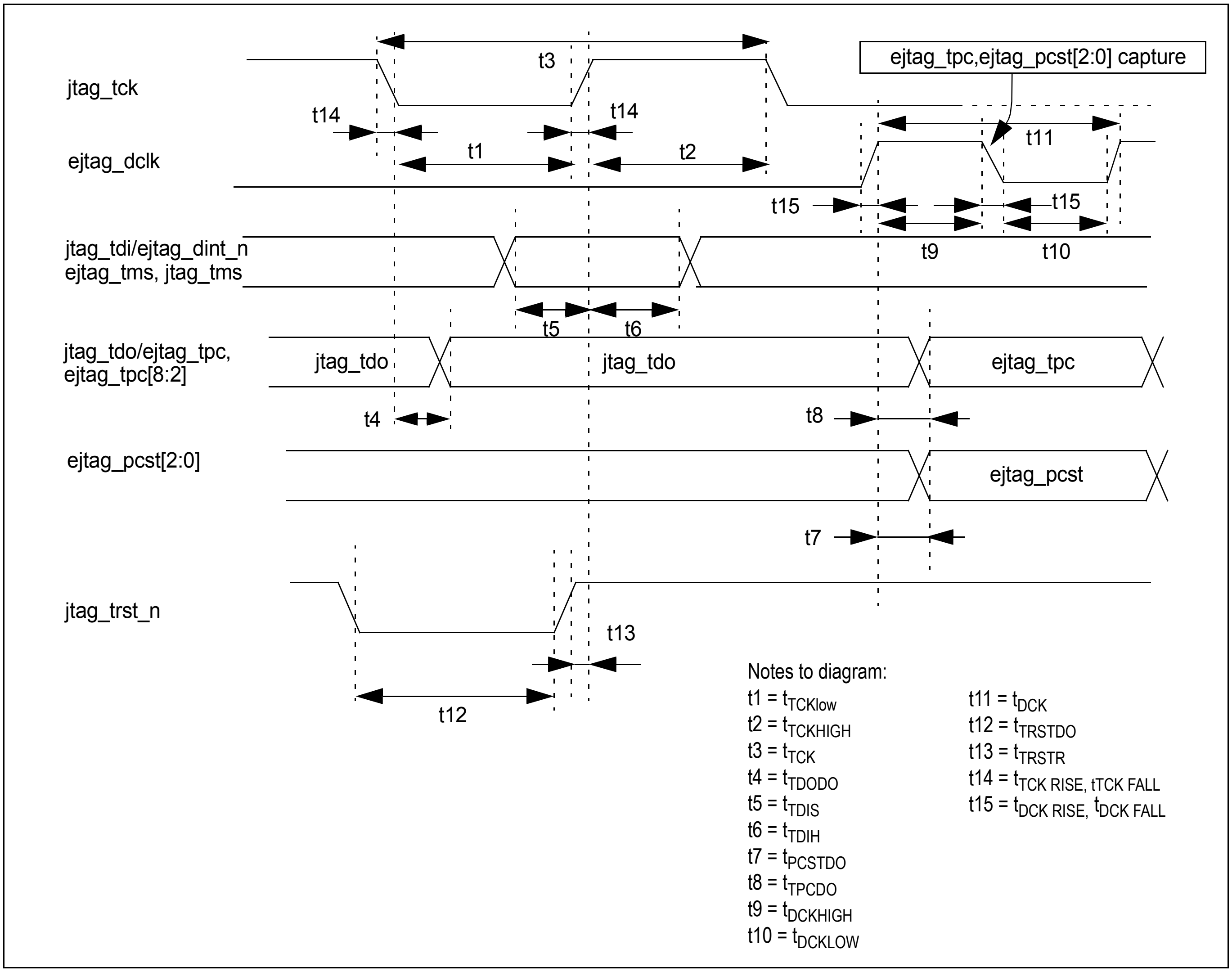
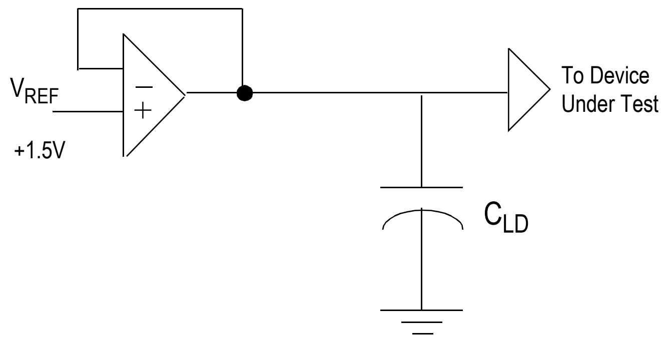


Figure 4 Standard EJTAG Timing

Output Loading for AC Testing



Signal	Cld
All High Drive Signals	50 pF
All Low Drive Signals	25 pF

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

Recommended Operation Temperature and Supply Voltage

3.3V Device

Grade	Ambient Temperature	Gnd	V_{cc}IO	V_{cc}Core	V_{cc}P
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	3.3V±5%	3.3V±5%

Table 7 Temperature and Voltage — 3.3V Device

2.5V Device

Grade	Ambient Temperature	Gnd	V_{cc}IO	V_{cc}Core	V_{cc}P
Commercial	0°C to +70°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%
Industrial	-40°C to +85°C Ambient	0V	3.3V±5%	2.5V±5%	2.5V±5%

Table 8 Temperature and Voltage — 2.5V Device

DC Electrical Characteristics — RC32333

Ta Commercial = 0°C to +70°C; Ta Industrial = -40°C to +85°C

3.3V version: V_{cc} Core = +3.3V±5%; V_{cc} I/O = +3.3V±5%

2.5V version: V_{cc} Core = +2.5V±5%; V_{cc} I/O = +3.3V±5%

	Parameter	RC32333[1]		Pin Numbers	Conditions
		Minimum	Maximum		
Input Pads	V_{IL}	—	0.8V	52, 64, 95, 161, 162, 165, 167-170, 191	—
	V_{IH}	2.0V	—		—
LOW Drive Output-Pads	V_{OL}	—	0.4V	41-45, 48, 171, 172, 175, 176, 177-180, 185-190, 195-200, 207, 208	$\|I_{OUT}\|$ = 6mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 8mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
HIGH Drive Output Pads	V_{OL}	—	0.4V	1- 5, 8, 13-15, 18-25, 28-35, 38-40, 49-51, 53- 57, 60, 61, 63, 65-67,70-76, 79, 80, 83-87, 90-94, 153, 154, 156, 159, 166, 194, 201, 204, 205, 206	$\|I_{OUT}\|$ = 7mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 16mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
PCI Drive Input Pads	V_{IL}	—	—	123, 155, 157, 158, 160	Per PCI 2.2
	V_{IH}	—	—		
PCI Drive Output pads	V_{OL}	—	—	96, 97, 100-109, 112-119, 122, 124-129, 132-139, 142-149, 152	Per PCI 2.2
	V_{OH}	—	—		
	V_{IL}	—	—		
	V_{IH}	—	—		
All Pads	C_{IN}	—	10pF	All input pads except 155 and 156	—
	C_{IN}[2]	5pf	12pF	155	Per PCI 2.2
	C_{IN}[3]		8pF	156	Per PCI 2.2
	C_{OUT}	—	10pF	All output pads	—
	I/O_{LEAK}	—	10µA	All non-internal pull-up pins	Input/Output Leakage
	I/O_{LEAK}	—	50µA	All internal pull-up pins	Input/Output Leakage

Table 9 DC Electrical Characteristics - RC32333

1. At all pipeline frequencies.

2. Applies only to pad 155.

3. Applies only to pad 156.

Capacitive Load Deration — RC32333

Refer to the IDT document 79RC32333 IBIS Model which can be found on the company's web site at www.idt.com.

Power Consumption

3.3V Device

Note: This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz		133MHz		150MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I_{CC}	Normal mode	360	480	480	630	550	700	mA	C_L = (See Figure 5, Output Loading for AC Testing) $T_a = 25^oC$ V_{cc} Core = 3.46V (for max. values) V_{cc} I/O = 3.46V (for max. values) V_{cc} Core = 3.3V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	250	370	330	480	390	540	mA	
Power Dissipation	Normal mode	1.2	1.7	1.5	2.2	1.7	2.4	W	
	Standby mode[1]	0.83	1.3	1.1	1.7	1.3	1.9	W	

Table 10 Power Consumption — 3.3V Device

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

2.5V Device

Note: This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz		133MHz		150MHz		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
I_{CC} I/O	Normal mode	24	81	32	93	35	104	mA	C_L = (See Figure 5, Output Loading for AC Testing) $T_a = 25^oC$ V_{cc} Core = 2.625V (for max. values) V_{cc} I/O = 3.46V (for max. values) V_{cc} Core = 2.5V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	2	81	2	93	2	104	mA	
I_{CC} core	Normal mode	232	301	298	392	333	438	mA	
	Standby mode[1]	120	269	151	319	168	345	mA	
Power Dissipation	Normal mode	0.66	1.07	0.85	1.35	0.95	1.51	W	
	Standby mode[1]	0.31	0.94	0.38	1.10	0.43	1.21	W	

Table 11 Power Consumption — 2.5V Device

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

Power Ramp-up

<u>3.3V Device</u>

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

<u>2.5V Device</u>

The 2.5V core supply (and 2.5V V_{cc}P supply) can be fully powered without the 3.3V I/O supply. However, the 3.3V I/O supply cannot exceed the 2.5V core supply by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the 3.3V I/O supply is powered.

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

Power Curves

The following four graphs contain the simulated power curves that show power consumption at various bus frequencies. Figures 6 and 7 apply to the 3.3V device, while Figures 8 and 9 apply to the 2.5V device.

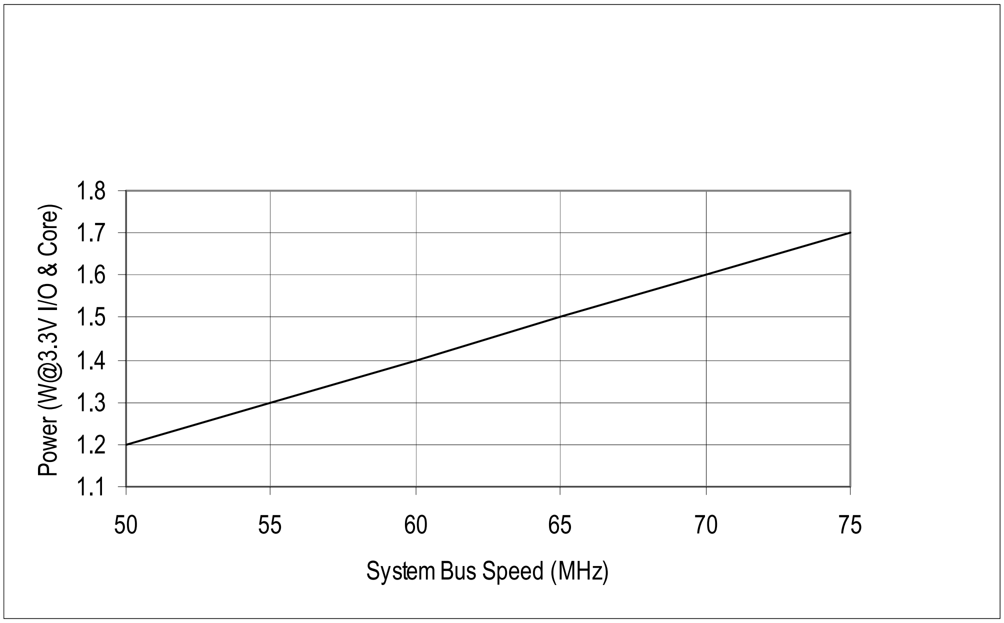


Figure 6 Typical Power Usage — RC32V333 Device

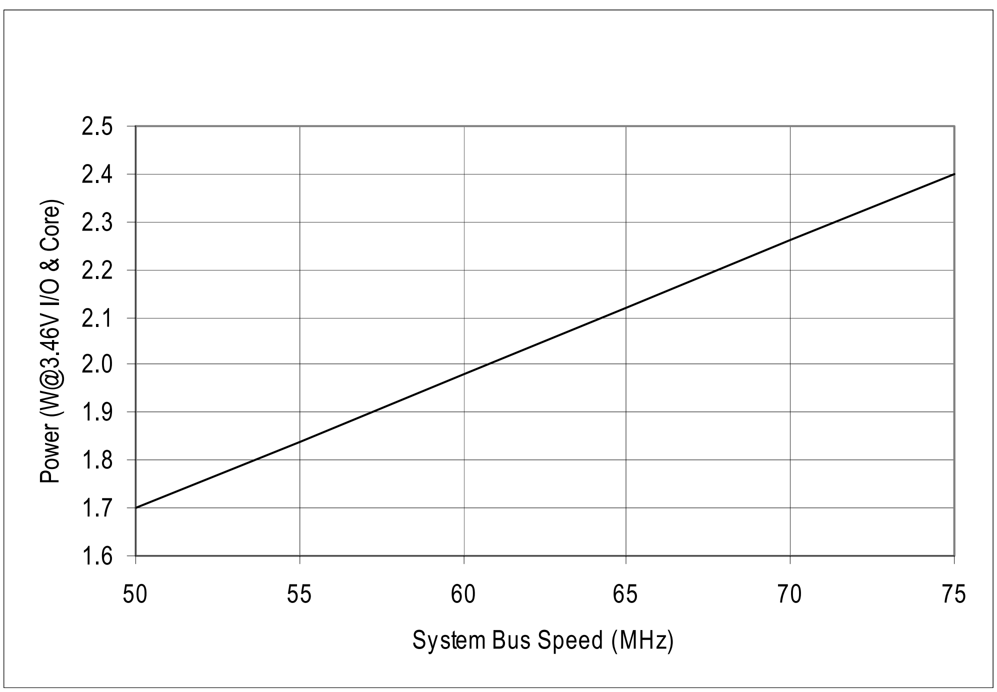


Figure 7 Maximum Power Usage — RC32V333 Device

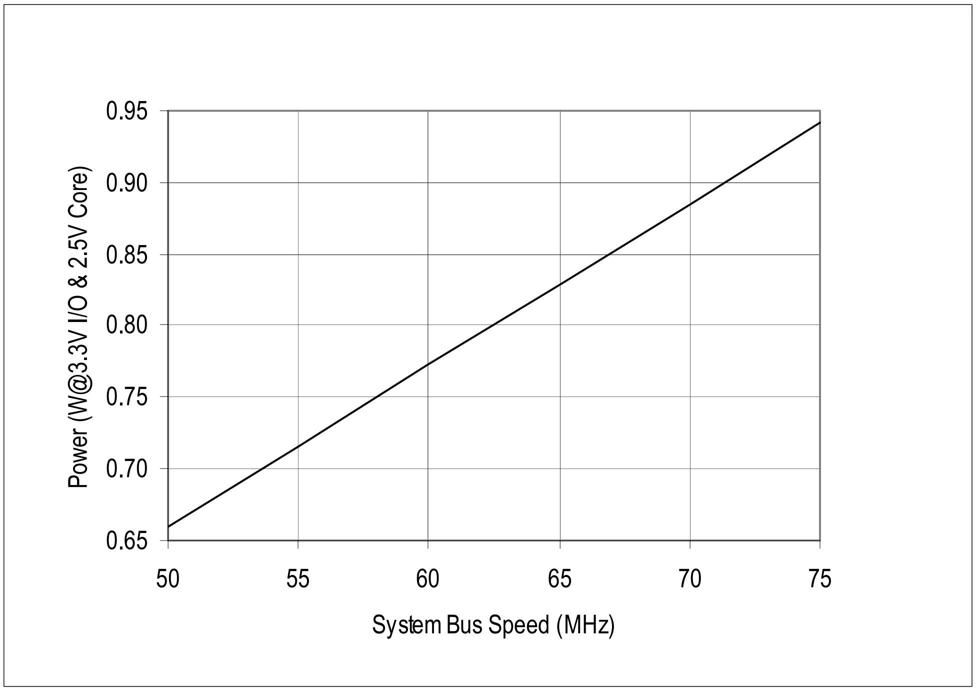


Figure 8 Typical Power Usage — RC32T333 Device

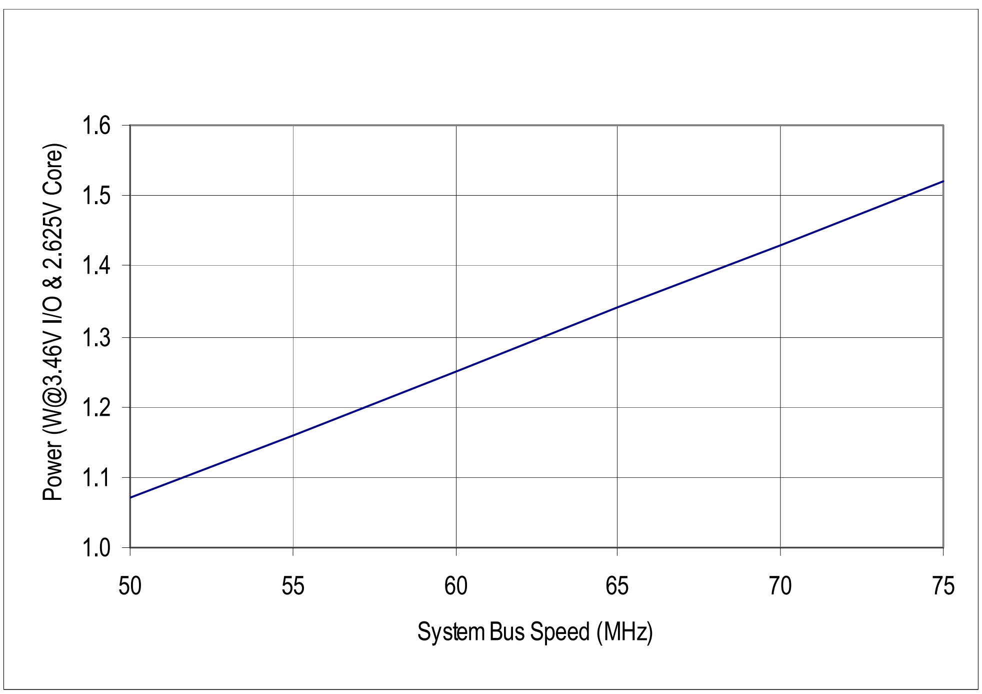


Figure 9 Maximum Power Usage — RC32T333 Device

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{cc} Core 3.3V Device	Supply Voltage	-0.3	4.0	V
V_{cc} Core 2.5V Device	Supply Voltage	-0.3	3.0	V
V_{CC} I/O	I/O Supply Voltage	-0.3	4.0	V
Vi 3.3V Device	Input Voltage	-0.3	5.5	V
Vi 2.5V Device	Input Voltage	-0.3	V_{CC}I/O+0.3	V
Vimin	Input Voltage - undershoot[2]	-0.6	—	V
Tstg	Storage Temperature	-40	125	degrees C

Table 12 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 7. Absolute maximum ratings are stress ratings only, and functional operation is not guaranteed beyond recommended operating voltages and temperatures. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. All PCI pads are fully compatible with PCI Specification version 2.2.

Package Pin-out — 208-PQFP for RC32333

The following table lists the pin numbers and signal names for the RC32333. Signal names ending with an _n are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	sdram_245_oe_n		53	mem_data[12]		105	pci_ad[7]		157	pci_req_n[1]	
2	sdram_we_n		54	mem_data[19]		106	pci_cbe_n[0]		158	pci_req_n[2]	1
3	sdram_cas_n		55	mem_data[13]		107	pci_ad[8]		159	pci_gnt_n[2]	1
4	sdram_bemask_n[0]		56	mem_data[18]		108	pci_ad[9]		160	pci_rst_n	
5	sdram_bemask_n[1]		57	mem_data[14]		109	pci_ad[10]		161	cpu_int_n[0]	
6	V_{ss}		58	V_{ss}		110	V_{ss}		162	cpu_int_n[1]	
7	V_{cc} I/O		59	V_{cc} I/O		111	V_{cc} I/O		163	V_{ss}	
8	sdram_cs_n[0]		60	mem_data[17]		112	pci_ad[11]		164	V_{cc} I/O	
9	sdram_cs_n[1]		61	mem_data[16]		113	pci_ad[12]		165	jtag_tdi	
10	sdram_ras_n		62	V_{cc} core		114	pci_ad[13]		166	jtag_tdo	
11	sdram_s_n[0]		63	mem_data[15]		115	pci_ad[14]		167	jtag_tms	
12	sdram_s_n[1]		64	cpu_masterclk		116	pci_ad[15]		168	ejtag_tms	
13	mem_addr[2]	1	65	mem_data[31]		117	pci_cbe_n[1]		169	jtag_tck	
14	mem_addr[3]	1	66	mem_data[0]		118	pci_par		170	jtag_trst_n	
15	mem_addr[4]	1	67	mem_data[30]		119	pci_serr_n		171	ejtag_pcst[0]	1
16	V_{ss}		68	V_{ss}		120	V_{ss}		172	ejtag_pcst[1]	1
17	V_{cc} I/O		69	V_{cc} I/O		121	V_{cc} I/O		173	V_{ss}	
18	mem_addr[5]	1	70	mem_data[1]		122	pci_perr_n		174	V_{cc} I/O	

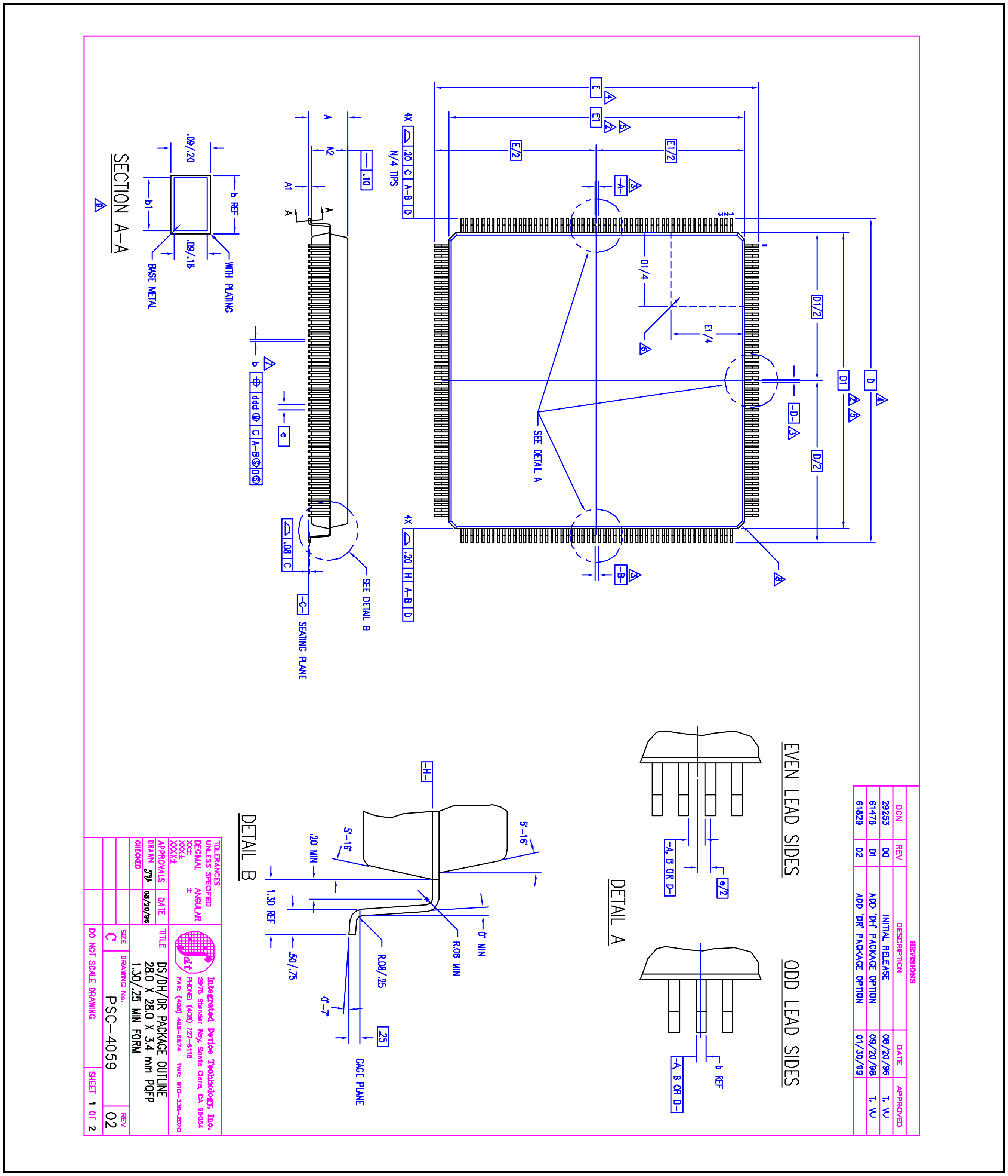
Table 13 RC32333 208-pin QFP Package Pin-Out (Part 1 of 2)

RC32333 Alternate Signal Functions

Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2
13	sdram_addr[2]		40	sdram_addr[16]		175	modebit[2]	
14	sdram_addr[3]		41	modebit[7]		177	modebit[3]	
15	sdram_addr[4]		42	modebit[8]		178	modebit[5]	
18	sdram_addr[5]		43	modebit[9]		179	modebit[4]	
19	sdram_addr[6]		44	reset_pci_host_mode		180	modebit[6]	
20	sdram_addr[7]		45	reset_boot_mode[0]		185	PIO[4]	
21	sdram_addr[8]		48	reset_boot_mode[1]		186	PIO[5]	pci_eeprom_sk
22	sdram_addr[9]		83	mem_245_dt_r_n	sdram_245_dt_r_n	187	PIO[3]	pci_eeprom_mdi
23	sdram_addr[10]		156	pci_eeprom_cs (satellite)	PIO[7]	188	PIO[6]	pci_eeprom_mdo
24	sdram_addr[11]		158	pci_idsel (satellite)		189	PIO[0]	dma_done_n[0]
35	sdram_addr[13]		159	pci_inta_n (satellite)		191	sdram_wait_n	mem_wait_n
38	sdram_addr[14]		171	modebit[0]		207	PIO[1]	
39	sdram_addr[15]		172	modebit[1]		208	PIO[2]	

Table 14 RC32333 Alternate Signal Functions

RC32333 Package Drawing — 208-pin PQFP



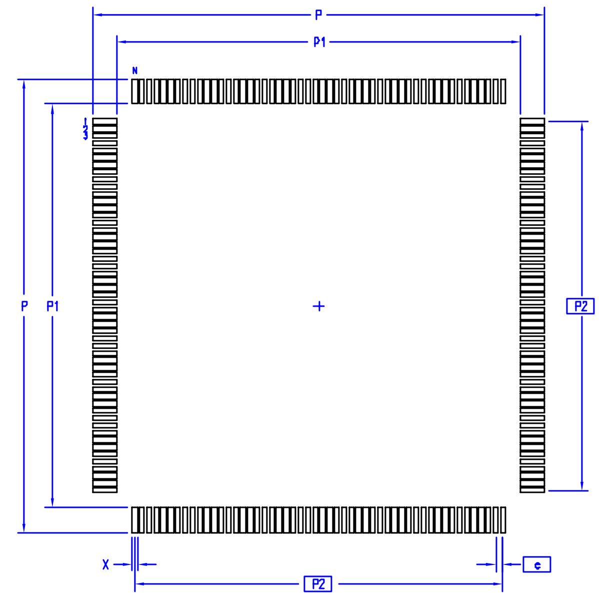
RC32333 Package Drawing — Page Two

REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
29253	00	INITIAL RELEASE	08/20/96	T. W
61478	01	ADD 'DH' PACKAGE OPTION	09/20/98	T. W
61829	02	ADD 'DR' PACKAGE OPTION	01/30/99	

SYMBOL	JEDEC VARIATION FA-1 MIN	NOM	MAX	NOTE
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D	30.60 BSC			4
D1	28.00 BSC			5,2
E	30.60 BSC			4
E1	28.00 BSC			5,2
N	208			
e	.50 BSC			
b	.17	–	.27	7
b1	.17	.20	.23	
ddd	–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A–B] AND [–D–] TO BE DETERMINED AT DATUM PLANE [–H–]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [–C–]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–143, VARIATION FA–1

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS | DATE
DRAWN JTJ | 08/20/96
CHECKED

TITLE DS/DH/DR PACKAGE OUTLINE
28.0 X 28.0 X 3.4 mm PQFP
1.30/.25 MIN FORM

SIZE C | DRAWING No. PSC–4059 | REV 02

DO NOT SCALE DRAWING | SHEET 2 OF 2