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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	102
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 46x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk30dx256zvlq10

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK30 and MK30 .

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K30
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory

Table continues on the next page...

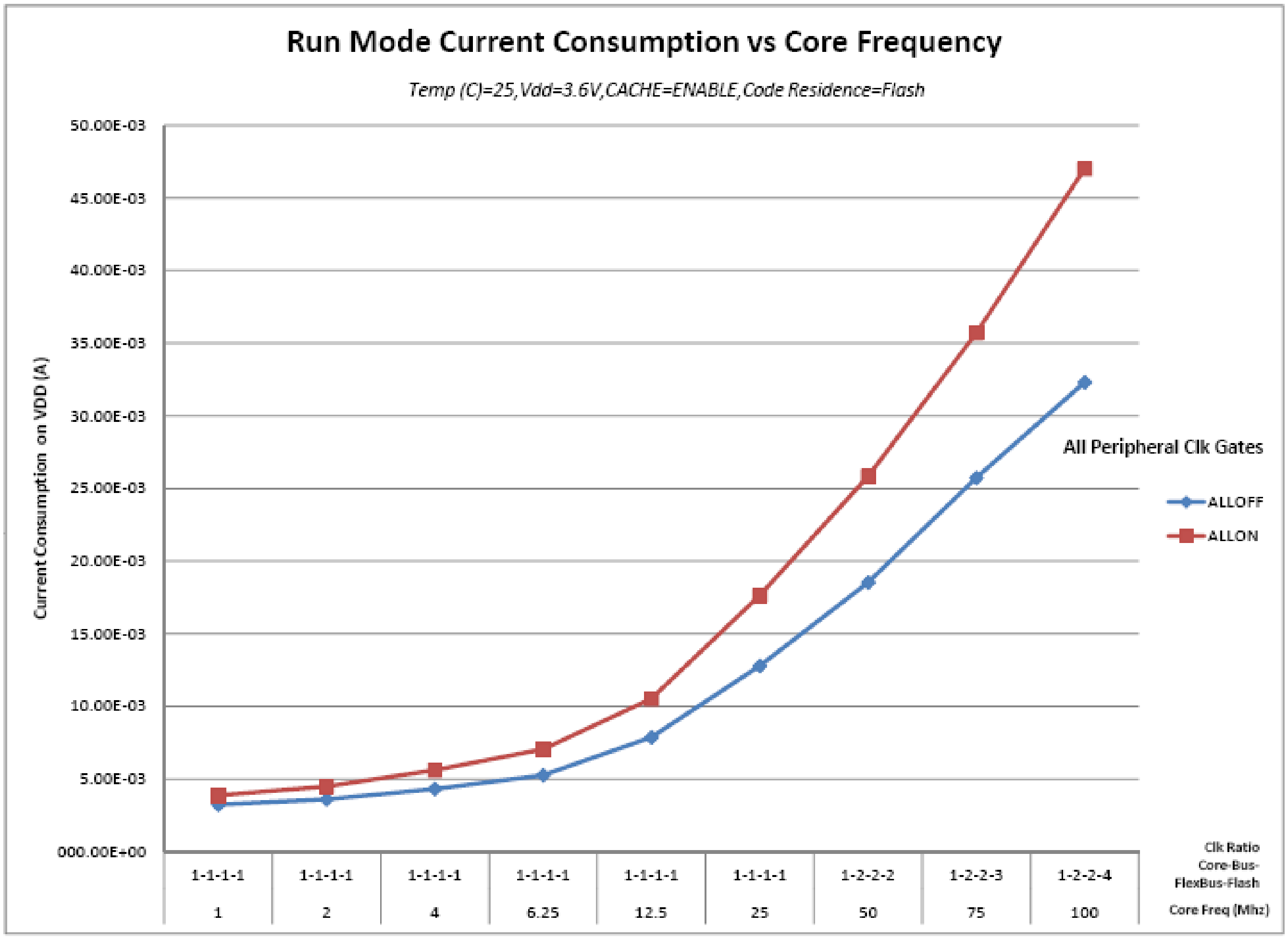

Figure 2. Run mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 144LQFP and 144MAPBGA

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	23	12	dBμV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	27	24	dBμV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	28	27	dBμV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	14	11	dBμV	
V_{RE_IEC}	IEC level	0.15–1000	K	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

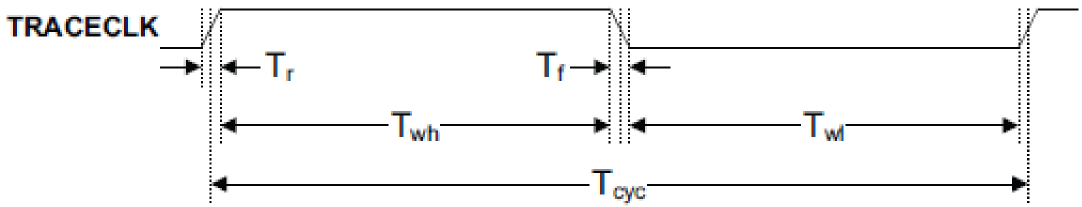

Figure 3. TRACE_CLKOUT specifications

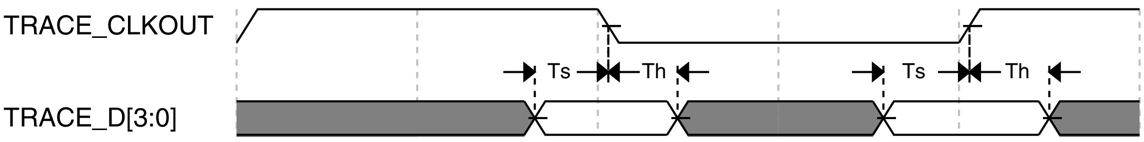

Figure 4. Trace data specifications

6.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 0 0 0	 10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 50 20 10	 — — —	 ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	

Table continues on the next page...

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 27 and Table 28 are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 29 and Table 30.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5

Table continues on the next page...

Table 27. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

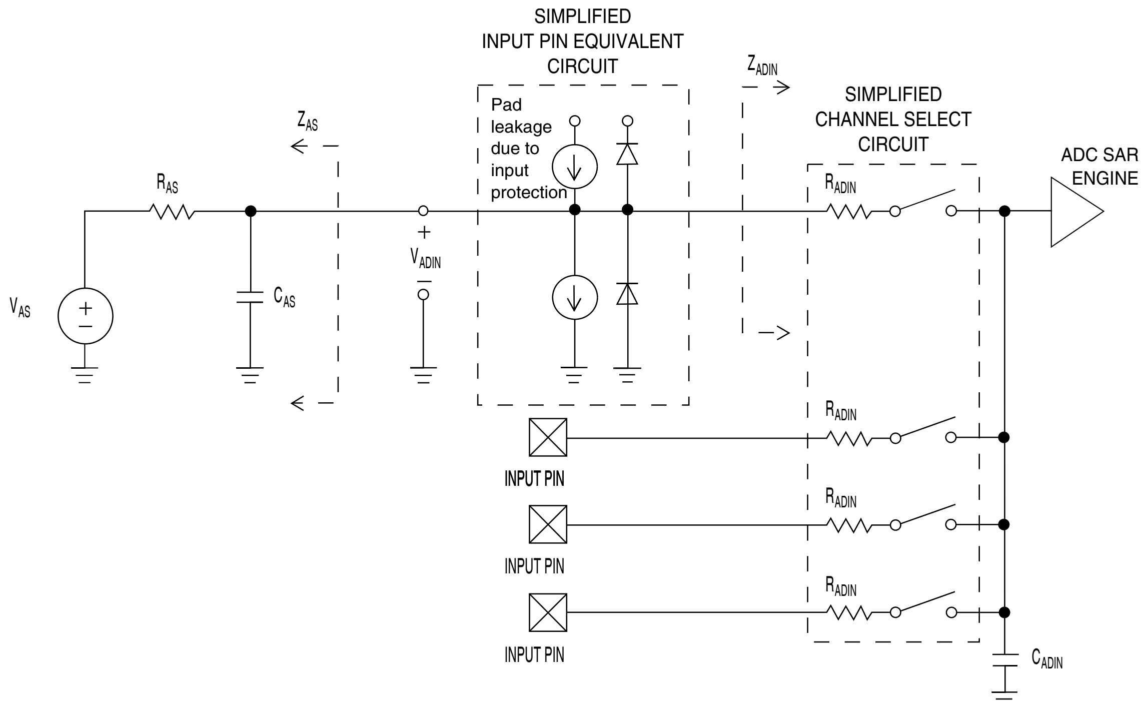

Figure 13. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

Table 30. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
G	Gain[4]	• PGAG=0 • PGAG=1 • PGAG=2 • PGAG=3 • PGAG=4 • PGAG=5 • PGAG=6	0.95 1.9 3.8 7.6 15.2 30.0 58.8	1 2 4 8 16 31.6 63.3	1.05 2.1 4.2 8.4 16.6 33.2 67.8		$R_{AS} < 100\Omega$
BW	Input signal bandwidth	• 16-bit modes • < 16-bit modes	— —	— —	4 40	kHz kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V_{DDA}= 3V ±100mV, f_{VDDA}= 50Hz, 60Hz
CMRR	Common mode rejection ratio	• Gain=1 • Gain=64	— —	-84 -85	— —	dB dB	V_{CM}= 500mVpp, f_{VCM}= 50Hz, 100Hz
V_{OFS}	Input offset voltage		—	0.2	—	mV	Output offset = V_{OFS}*(Gain+1)
T_{GSW}	Gain switching settling time		—	—	10	µs	5
dG/dT	Gain drift over full temperature range	• Gain=1 • Gain=64	— —	6 31	10 42	ppm/°C ppm/°C	
dG/dV_{DDA}	Gain drift over supply voltage	• Gain=1 • Gain=64	— —	0.07 0.14	0.21 0.31	%/V %/V	V_{DDA} from 1.71 to 3.6V
E_{IL}	Input leakage error	All modes	$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
$V_{PP,DIFF}$	Maximum differential input signal swing		$\left(\frac{\min(V_x, V_{DDA}-V_x)-0.2)\times 4}{\text{Gain}}\right)$ where $V_X = V_{REFPGA} \times 0.583$			V	6
SNR	Signal-to-noise ratio	• Gain=1 • Gain=64	80 52	90 66	— —	dB dB	16-bit differential mode, Average=32
THD	Total harmonic distortion	• Gain=1 • Gain=64	85 49	100 95	— —	dB dB	16-bit differential mode, Average=32, f_{in}=100Hz

Table continues on the next page...

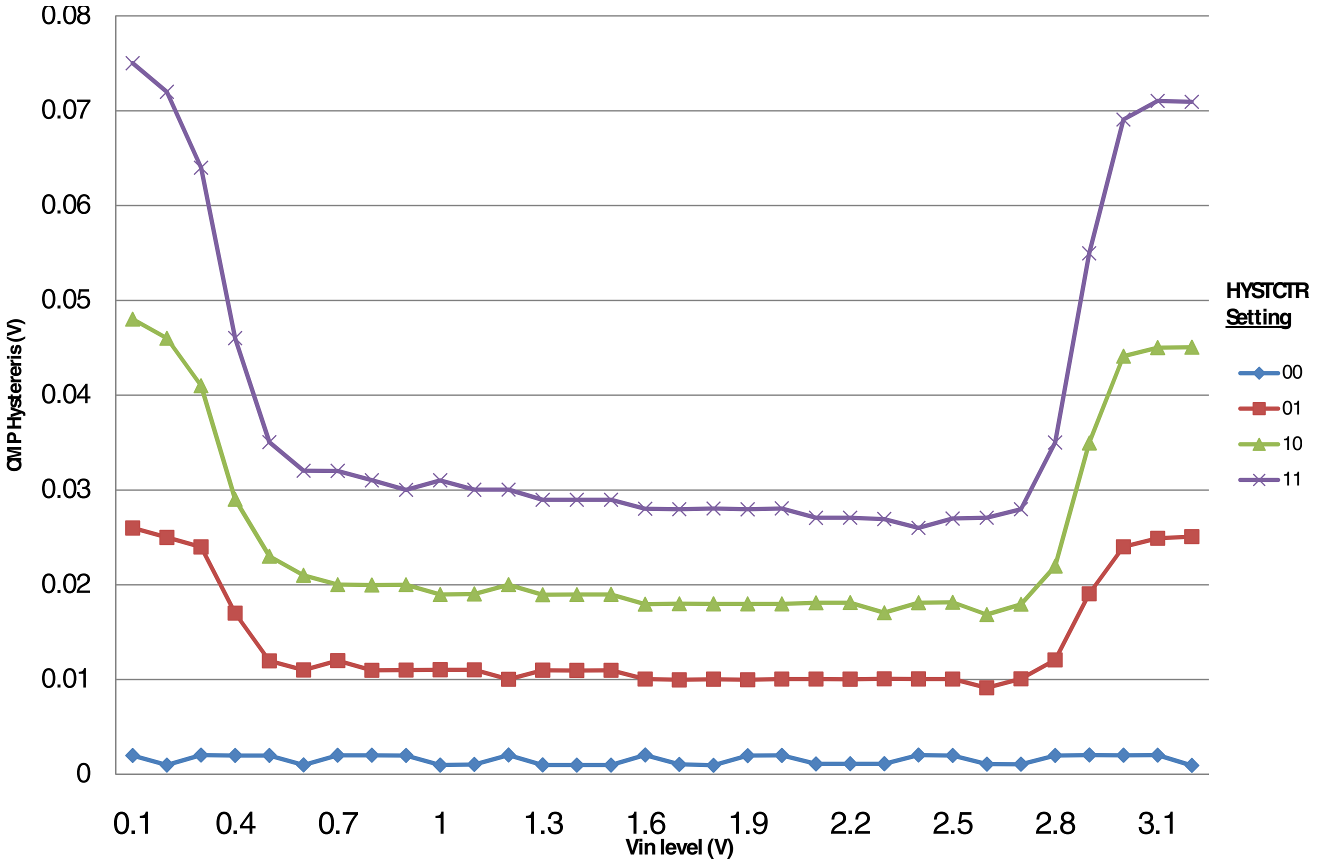

Figure 16. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

Table 39. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

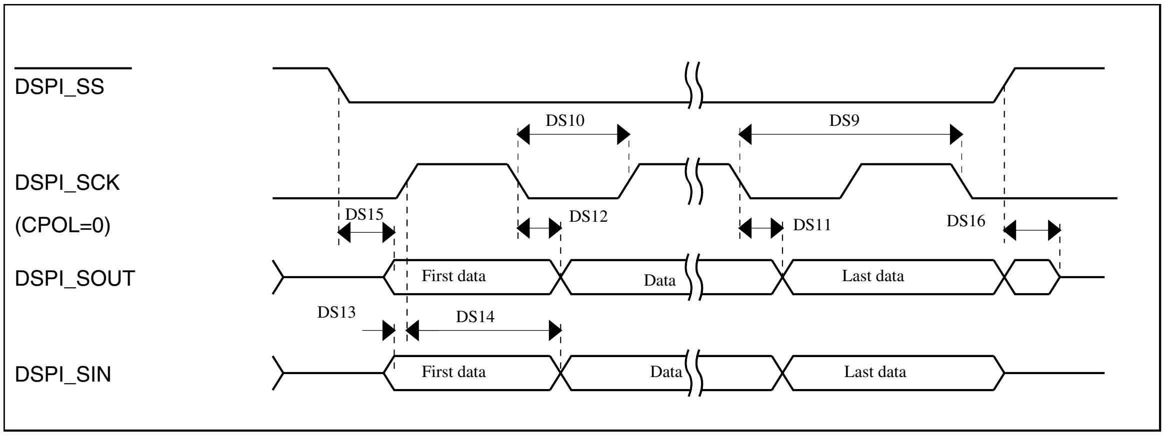

Figure 21. DSPI classic SPI timing — slave mode

6.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 40. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	

Table continues on the next page...

6. C_b = total capacitance of the one bus line in pF.

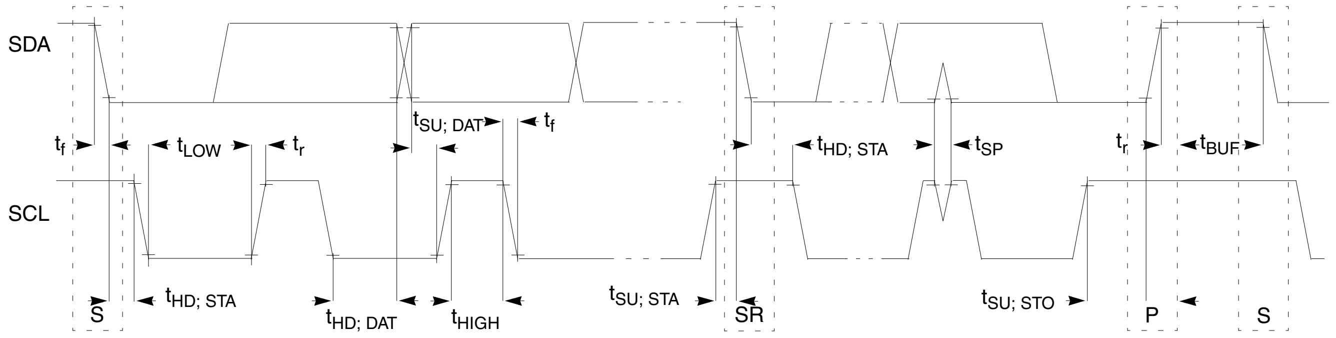

Figure 24. Timing definition for fast and standard mode devices on the I2C bus

6.8.5 UART switching specifications

See General switching specifications.

6.8.6 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 43. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	8.3	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

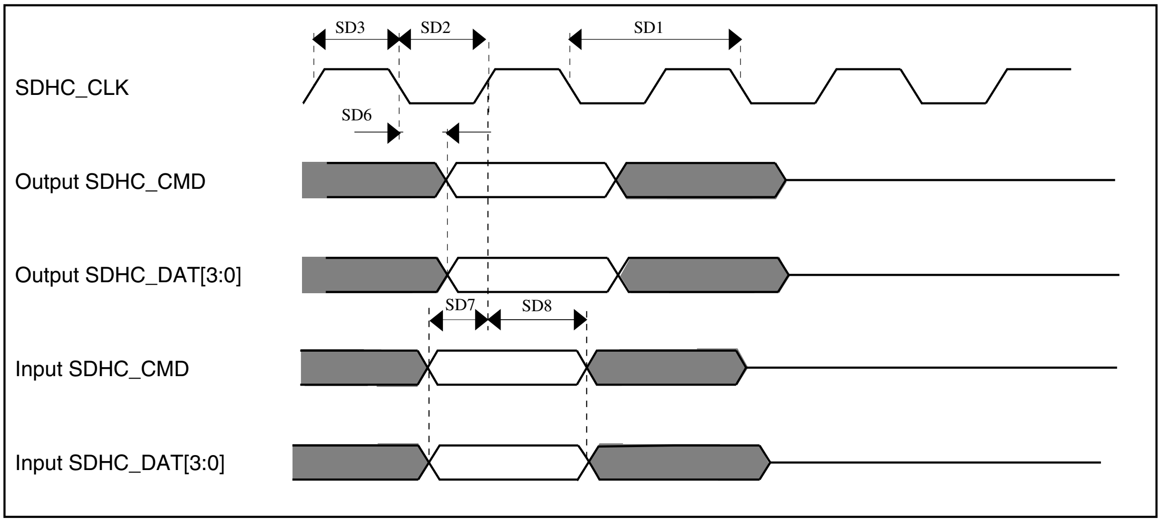

Figure 25. SDHC timing

6.8.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.7.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Table 44. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns

Table continues on the next page...

Table 44. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

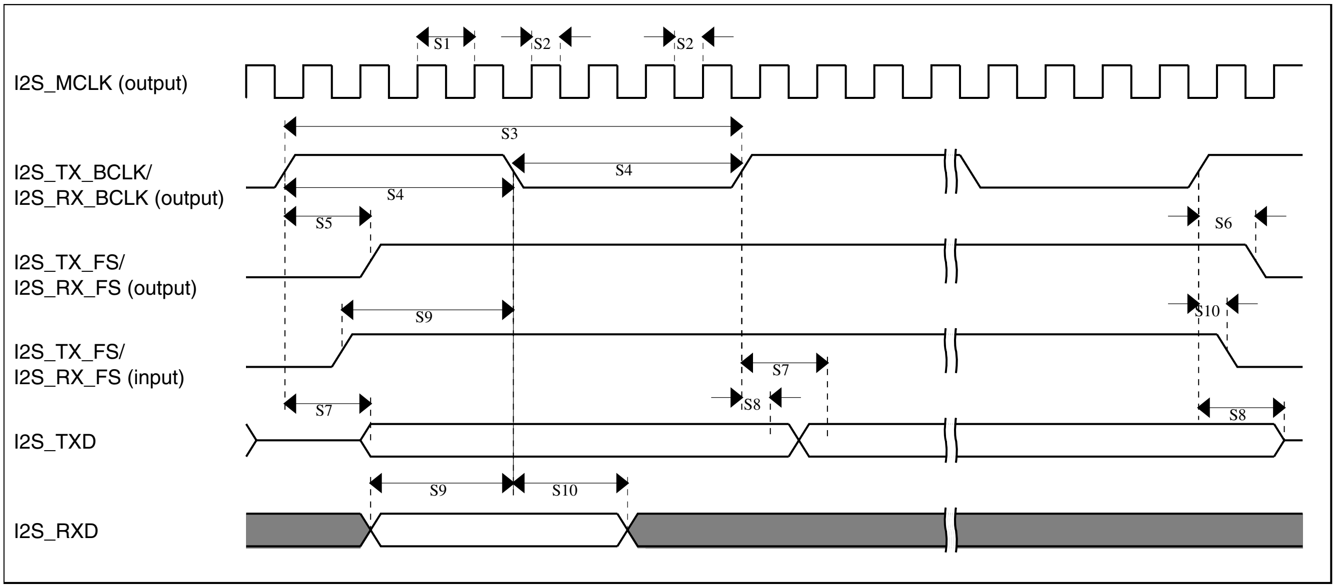

Figure 26. I2S/SAI timing — master modes

Table 45. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid • Multiple SAI Synchronous mode • All other modes	 — —	 21 15	ns

Table continues on the next page...

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. REFCHRG = 2, EXTCHRG=0.
4. REFCHRG = 0, EXTCHRG = 10.
5. V_{DD} = 3.0 V.
6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN)

    The typical value is calculated with the following configuration:

    $I_{ext} = 6$ µA (EXTCHRG = 2), PS = 128, NSCN = 2, $I_{ref} = 16$ µA (REFCHRG = 7), C_{ref} = 1.0 pF

    The minimum value is calculated with the following configuration:

    $I_{ext} = 2$ µA (EXTCHRG = 0), PS = 128, NSCN = 32, $I_{ref} = 32$ µA (REFCHRG = 15), C_{ref} = 0.5 pF

    The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.
12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

6.9.2 LCD electrical characteristics

Table 51. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}					3
	• HREFSEL=0, RVTRIM=1111	—	1.11	—	V	
	• HREFSEL=0, RVTRIM=1000	—	1.01	—	V	
	• HREFSEL=0, RVTRIM=0000	—	0.91	—	V	
	• HREFSEL=1, RVTRIM=1111	—	1.84	—	V	
	• HREFSEL=1, RVTRIM=1000	—	1.69	—	V	
	• HREFSEL=1, RVTRIM=0000	—	1.54	—	V	
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
—	V_{IREG} ripple					
	• HREFSEL = 0	—	—	30	mV	
	• HREFSEL = 1	—	—	50	mV	

Table continues on the next page...

Table 51. LCD electricals (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	μA	4
I_{RBIAS}	RBIAS current adder • LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF) • LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	— —	10 1	— —	μA μA	
R_{RBIAS}	RBIAS resistor values • LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF) • LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	— —	0.28 2.98	— —	MΩ MΩ	
VLL2	VLL2 voltage • HREFSEL = 0 • HREFSEL = 1	2.0 – 5% 3.3 – 5%	2.0 3.3	— —	V V	
VLL3	VLL3 voltage • HREFSEL = 0 • HREFSEL = 1	3.0 – 5% 5 – 5%	3.0 5	— —	V V	

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. 2000 pF load LCD, 32 Hz frame frequency

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
144-pin MAPBGA	98ASA00222D

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
39	L4	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23								
40	M7	XTAL32	XTAL32	XTAL32								
41	M6	EXTAL32	EXTAL32	EXTAL32								
42	L6	VBAT	VBAT	VBAT								
43	—	VDD	VDD	VDD								
44	—	VSS	VSS	VSS								
45	M4	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX			EWM_OUT_b		
46	K5	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	UART4_RX		FB_AD23	EWM_IN		
47	K4	PTE26	DISABLED		PTE26		UART4_CTS_ b		FB_AD22	RTC_CLKOUT		
48	J4	PTE27	DISABLED		PTE27		UART4_RTS_ b		FB_AD21			
49	H4	PTE28	DISABLED		PTE28				FB_AD20			
50	J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
54	L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_TX_ BCLK	JTAG_TRST_ b	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	DISABLED		PTA6		FTM0_CH3		CLKOUT		TRACE_ CLKOUT	
59	J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7		FTM0_CH4		FB_AD18		TRACE_D3	
60	K8	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0		FB_AD17	FTM1_QD_ PHA	TRACE_D2	
61	L8	PTA9	DISABLED		PTA9		FTM1_CH1		FB_AD16	FTM1_QD_ PHB	TRACE_D1	
62	M9	PTA10	DISABLED		PTA10		FTM2_CH0		FB_AD15	FTM2_QD_ PHA	TRACE_D0	
63	L9	PTA11	DISABLED		PTA11		FTM2_CH1		FB_OE_b	FTM2_QD_ PHB		
64	K9	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0		FB_CS5_b/ FB_TSIZ1/	I2S0_TXD0	FTM1_QD_ PHA	

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
									FB_BE23_16_b			
65	J9	PTA13/LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/LLWU_P4	CAN0_RX	FTM1_CH1		FB_CS4_b/FB_TSIZ0/FB_BE31_24_b	I2S0_TX_FS	FTM1_QD_PHB	
66	L10	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX		FB_AD31	I2S0_RX_BCLK	I2S0_TXD1	
67	L11	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX		FB_AD30	I2S0_RXD0		
68	K10	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b/UART0_COL_b		FB_AD29	I2S0_RX_FS	I2S0_RXD1	
69	K11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b		FB_AD28	I2S0_MCLK		
70	E8	VDD	VDD	VDD								
71	G8	VSS	VSS	VSS								
72	M12	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
73	M11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
74	L12	RESET_b	RESET_b	RESET_b								
75	K12	PTA24	DISABLED		PTA24				FB_AD14			
76	J12	PTA25	DISABLED		PTA25				FB_AD13			
77	J11	PTA26	DISABLED		PTA26				FB_AD12			
78	J10	PTA27	DISABLED		PTA27				FB_AD11			
79	H12	PTA28	DISABLED		PTA28				FB_AD10			
80	H11	PTA29	DISABLED		PTA29				FB_AD19			
81	H10	PTB0/LLWU_P5	LCD_P0/ADC0_SE8/ADC1_SE8/TSI0_CH0	LCD_P0/ADC0_SE8/ADC1_SE8/TSI0_CH0	PTB0/LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA	LCD_P0	
82	H9	PTB1	LCD_P1/ADC0_SE9/ADC1_SE9/TSI0_CH6	LCD_P1/ADC0_SE9/ADC1_SE9/TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB	LCD_P1	
83	G12	PTB2	LCD_P2/ADC0_SE12/TSI0_CH7	LCD_P2/ADC0_SE12/TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3	LCD_P2	
84	G11	PTB3	LCD_P3/ADC0_SE13/TSI0_CH8	LCD_P3/ADC0_SE13/TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_b/UART0_COL_b			FTM0_FLT0	LCD_P3	
85	G10	PTB4	LCD_P4/ADC1_SE10	LCD_P4/ADC1_SE10	PTB4					FTM1_FLT0	LCD_P4	
86	G9	PTB5	LCD_P5/ADC1_SE11	LCD_P5/ADC1_SE11	PTB5					FTM2_FLT0	LCD_P5	

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
87	F12	PTB6	LCD_P6/ ADC1_SE12	LCD_P6/ ADC1_SE12	PTB6						LCD_P6	
88	F11	PTB7	LCD_P7/ ADC1_SE13	LCD_P7/ ADC1_SE13	PTB7						LCD_P7	
89	F10	PTB8	LCD_P8	LCD_P8	PTB8		UART3_RTS_ b				LCD_P8	
90	F9	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_PCS1	UART3_CTS_ b				LCD_P9	
91	E12	PTB10	LCD_P10/ ADC1_SE14	LCD_P10/ ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1	LCD_P10	
92	E11	PTB11	LCD_P11/ ADC1_SE15	LCD_P11/ ADC1_SE15	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2	LCD_P11	
93	H7	VSS	VSS	VSS								
94	F5	VDD	VDD	VDD								
95	E10	PTB16	LCD_P12/ TSI0_CH9	LCD_P12/ TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX			EWM_IN	LCD_P12	
96	E9	PTB17	LCD_P13/ TSI0_CH10	LCD_P13/ TSI0_CH10	PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	LCD_P13	
97	D12	PTB18	LCD_P14/ TSI0_CH11	LCD_P14/ TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK		FTM2_QD_ PHA	LCD_P14	
98	D11	PTB19	LCD_P15/ TSI0_CH12	LCD_P15/ TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS		FTM2_QD_ PHB	LCD_P15	
99	D10	PTB20	LCD_P16	LCD_P16	PTB20	SPI2_PCS0				CMP0_OUT	LCD_P16	
100	D9	PTB21	LCD_P17	LCD_P17	PTB21	SPI2_SCK				CMP1_OUT	LCD_P17	
101	C12	PTB22	LCD_P18	LCD_P18	PTB22	SPI2_SOUT				CMP2_OUT	LCD_P18	
102	C11	PTB23	LCD_P19	LCD_P19	PTB23	SPI2_SIN	SPI0_PCS5				LCD_P19	
103	B12	PTC0	LCD_P20/ ADC0_SE14/ TSI0_CH13	LCD_P20/ ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG			I2S0_TXD1	LCD_P20	
104	B11	PTC1/ LLWU_P6	LCD_P21/ ADC0_SE15/ TSI0_CH14	LCD_P21/ ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0		I2S0_TXD0	LCD_P21	
105	A12	PTC2	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1		I2S0_TX_FS	LCD_P22	
106	A11	PTC3/ LLWU_P7	LCD_P23/ CMP1_IN1	LCD_P23/ CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK	LCD_P23	
107	H8	VSS	VSS	VSS								
108	C10	VLL3	VLL3	VLL3								
109	C9	VLL2	VLL2	VLL2								
110	B9	VLL1	VLL1	VLL1								
111	B10	VCAP2	VCAP2	VCAP2								
112	A10	VCAP1	VCAP1	VCAP1								
113	A9	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LCD_P24	

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
139	B3	PTD10	DISABLED		PTD10		UART5_RTS_b		FB_AD9			
140	B2	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_CLKIN	FB_AD8			
141	B1	PTD12	DISABLED		PTD12	SPI2_SCK		SDHC0_D4	FB_AD7			
142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5	FB_AD6			
143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6	FB_AD5			
144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7	FB_RW_b			

8.2 K30 pinouts

The figure below shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Table 52. Revision history (continued)

Rev. No.	Date	Substantial Changes
2	12/2012	Replaced TBDs throughout.
3	6/2013	• In ESD handling ratings, added a note for ILAT. • Updated "Voltage and current operating requirements" Table 1. • Updated I_{OL} data for V_{OL} row in "Voltage and current operating behaviors" Table 4. • Updated wakeup times and t_{POR} value in "Power mode transition operating behaviors" Table 5. • In "EMC radiated emissions operating behaviors . . ." Table 7, added a column for 144MAPBGA. • In "16-bit ADC operating conditions" Table 27, updated the max spec of VADIN. • In "16-bit ADC electrical characteristics" Table 28, updated the temp sensor slope and voltage specs. • Updated Inter-Integrated Circuit Interface (I^2C) timing. • In SDHC specifications, added operating voltage row.