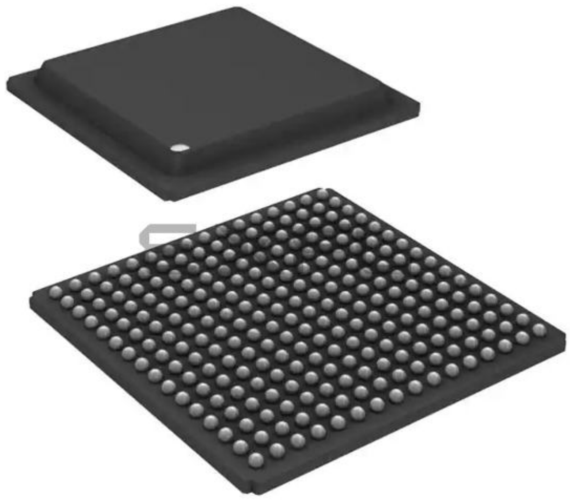

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc850decvr66bu

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I^2C port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

Table 1. MPC850 Functionality Matrix

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Additional documentation may be provided for parts listed in Table 1.

2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:

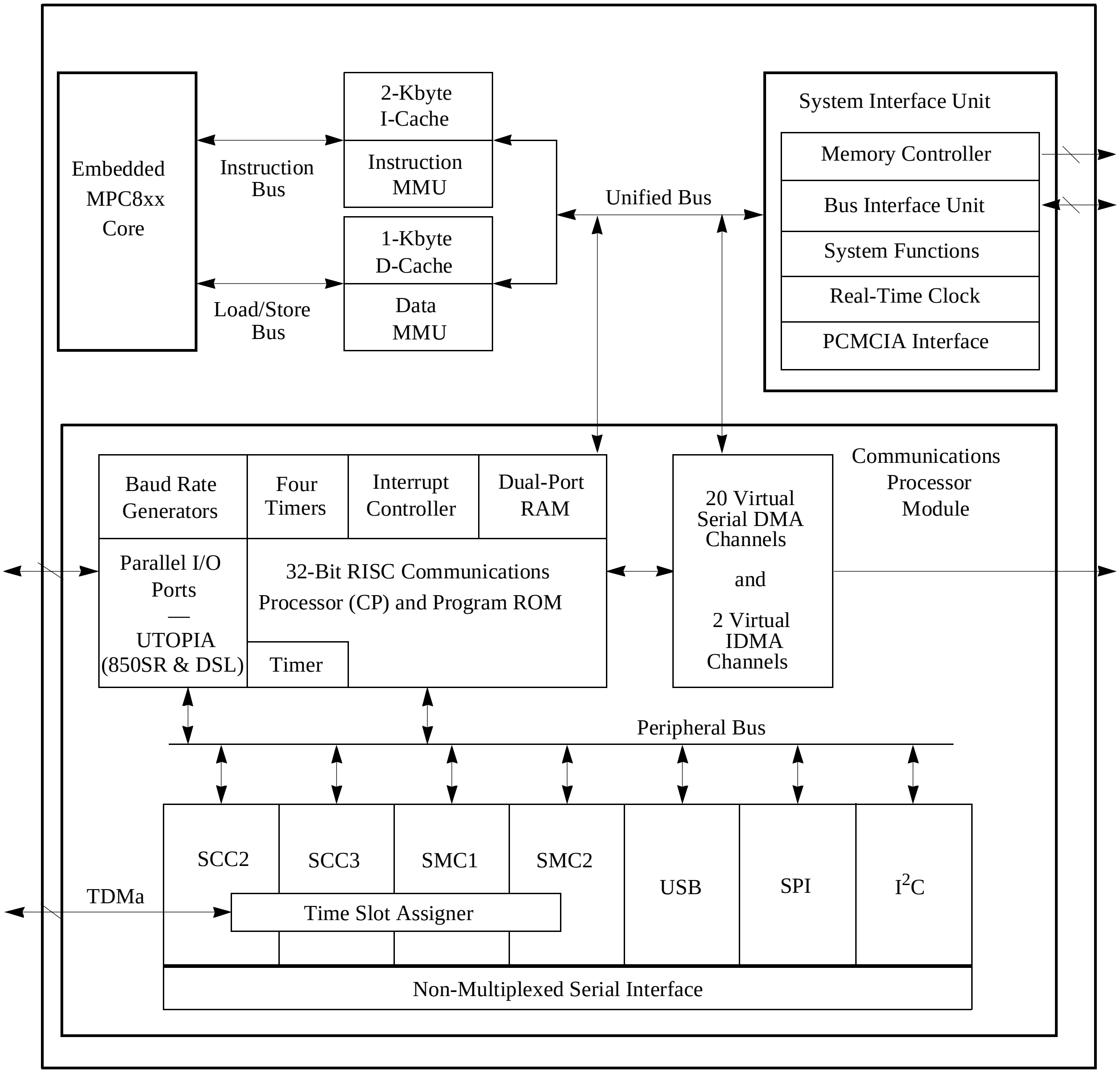

Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  — Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input low voltage	VIL	GND	0.8	V
EXTAL, EXTCLK input high voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input leakage current, Vin = 5.5 V (Except TMS, TRST, DSCK and DSDI pins)	I_{in}	—	100	µA
Input leakage current, Vin = 3.6V (Except TMS, TRST, DSCK and DSDI pins)	I_{In}	—	10	µA
Input leakage current, Vin = 0V (Except TMS, TRST, DSCK and DSDI pins)	I_{In}	—	10	µA
Input capacitance	C_{in}	—	20	pF
Output high voltage, IOH = -2.0 mA, VDDH = 3.0V except XTAL, XFC, and open-drain pins	VOH	2.4	—	V
Output low voltage CLKOUT [3] IOL = 3.2 mA [1] IOL = 5.3 mA [2] IOL = 7.0 mA PA[14]/USBOE, PA[12]/TXD2 IOL = 8.9 mA TS, TA, TEA, BI, BB, HRESET, SRESET	VOL	—	0.5	V

1 A[6:31], TSIZ0/REG, TSIZ1, D[0:31], DP[0:3]/IRQ[3:6], RD/WR, BURST, RSV/IRQ2, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, PA[15]/USBRXD, PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/TOUT1/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/TOUT2/TIN4, PB[31]/SPISEL, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/BRGO1, PB[26]/I2CSCL/BRGO2, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/SDACK1, PB[22]/SMSYN2/SDACK2, PB[19]/L1ST1, PB[18]/RTS2/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/DREQ0/L1ST5, PC[14]/DREQ1/RTS2/L1ST6, PC[13]/L1ST7/RTS3, PC[12]/L1RQa/L1ST8, PC[11]/USBRXP, PC[10]/TGATE1/USBRXN, PC[9]/CTS2, PC[8]/CD2/TGATE1, PC[7]/USBTXP, PC[6]/USBTXN, PC[5]/CTS3/L1TSYNCA/SDACK1, PC[4]/CD3/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

2 BDIP/GPL_B5, BR, BG, FRZ/IRQ6, CS[0:5], CS6/CE1_B, CS7/CE2_B, WE0/BS_AB0/IORD, WE1/BS_AB1/IOWR, WE2/BS_AB2/PCOE, WE3/BS_AB3/PCWE, GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A[2:3]/GPL_B[2:3]/CS[2:3], UPWAITA/GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/DSCK/AT1, OP2/MODCK1/STS, OP3/MODCK2/DSDO

3 The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, IOH and IOL for Clkout should be extracted from the IBIS model at any output voltage level.

5 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the equation:

$T_J = T_A + (P_D \bullet \theta_{JA})$(1)

where

T_A = Ambient temperature, °C

Table 6. Bus Operation Timing [1]

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B1	CLKOUT period	20	—	30.30	—	25	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	—	50.00	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	—	50.00	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) [2]	-0.60	0.60	-0.60	0.60	-0.60	0.60	—	50.00	ns
B1d	CLKOUT phase jitter [2]	-2.00	2.00	-2.00	2.00	-2.00	2.00	—	50.00	ns
B1e	CLKOUT frequency jitter (MF < 10) [2]	—	0.50	—	0.50	—	0.50	—	50.00	%
B1f	CLKOUT frequency jitter (10 < MF < 500) [2]	—	2.00	—	2.00	—	2.00	—	50.00	%
B1g	CLKOUT frequency jitter (MF > 500) [2]	—	3.00	—	3.00	—	3.00	—	50.00	%
B1h	Frequency jitter on EXTCLK [3]	—	0.50	—	0.50	—	0.50	—	50.00	%
B2	CLKOUT pulse width low	8.00	—	12.12	—	10.00	—	—	50.00	ns
B3	CLKOUT width high	8.00	—	12.12	—	10.00	—	—	50.00	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B7	CLKOUT to A[6–31], RD/WR, BURST, D[0–31], DP[0–3] invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3], BDIP, PTR invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS[0–1], VF[0–2] IWP[0–2], LWP[0–1], STS invalid [4]	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B8	CLKOUT to A[6–31], RD/WR, BURST, D[0–31], DP[0–3] valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3] BDIP, PTR valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8b	CLKOUT to BR, BG, VFLS[0–1], VF[0–2], IWP[0–2], FRZ, LWP[0–1], STS valid [4]	5.00	11.74	7.58	14.33	6.25	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B28c	CLKOUT falling edge to WE[0–3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	—	14.00	—	18.00	—	16.00	0.375	50.00	ns
B29	$\overline{WE[0–3]}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29a	$\overline{WE[0–3]}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29b	$\overline{CS}$ negated to D[0–31], DP[0–3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29c	$\overline{CS}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29d	$\overline{WE[0–3]}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29e	$\overline{CS}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29f	$\overline{WE[0–3]}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns
B29g	$\overline{CS}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B33	CLKOUT falling edge to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

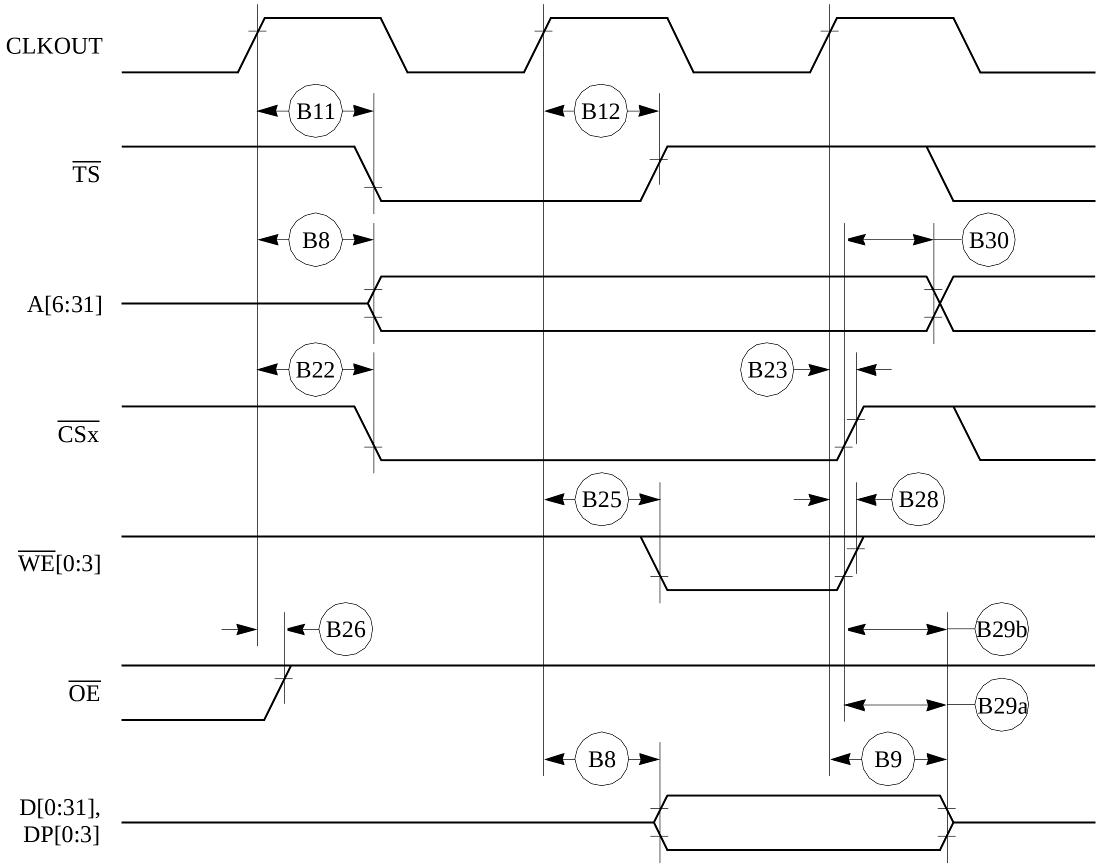

Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

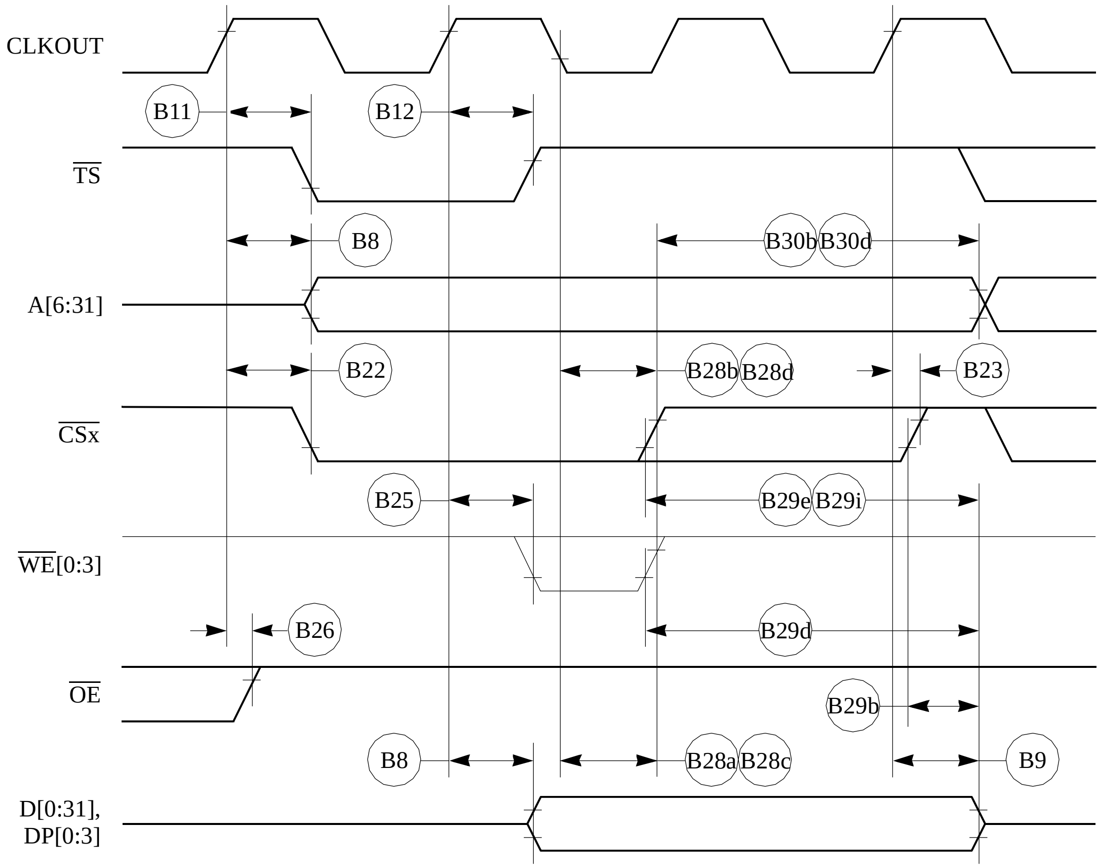

Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

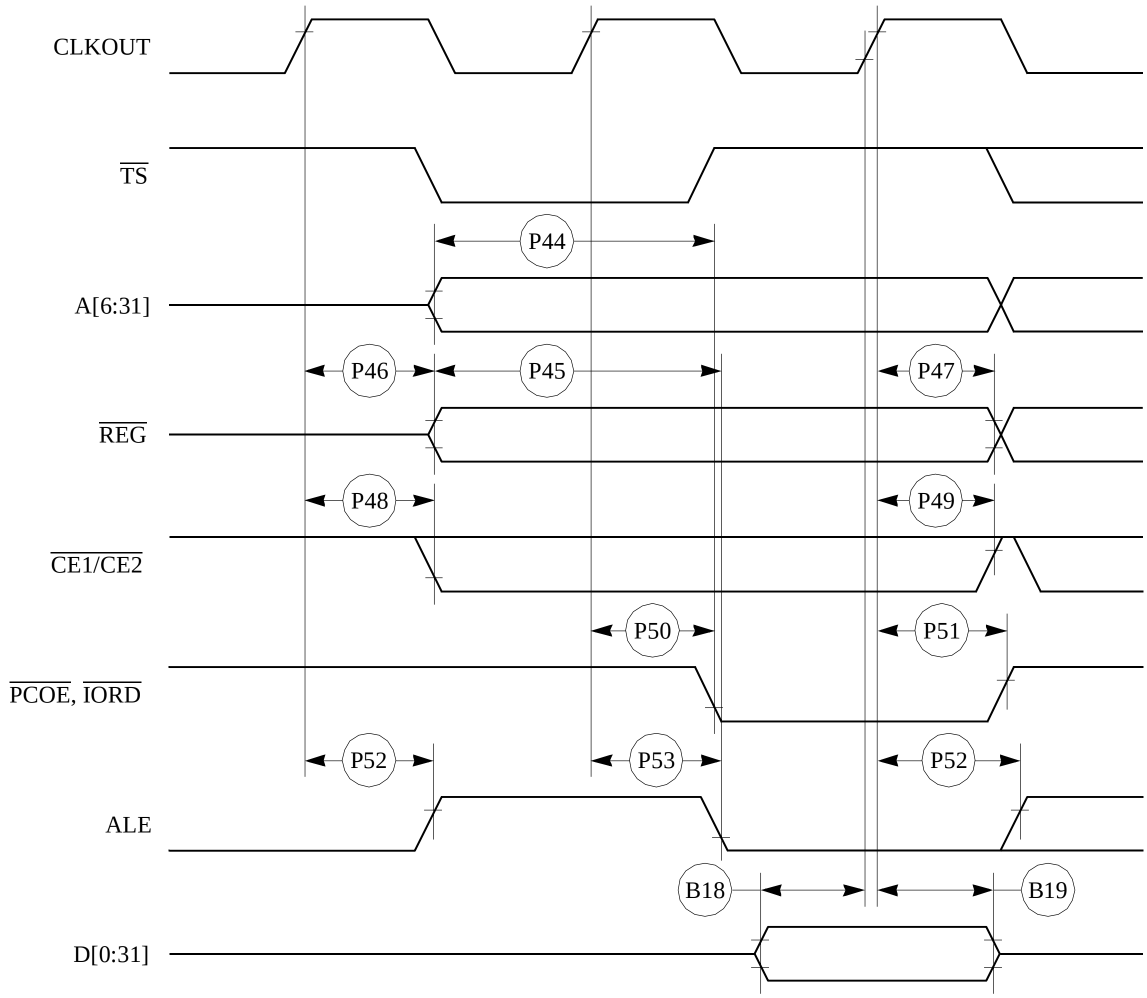

Figure 24. PCMCIA Access Cycles Timing External Bus Read

Table 9 shows the PCMCIA port timing for the MPC850.

Table 9. PCMCIA Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive [1]	18.00	—	26.00	—	22.00	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

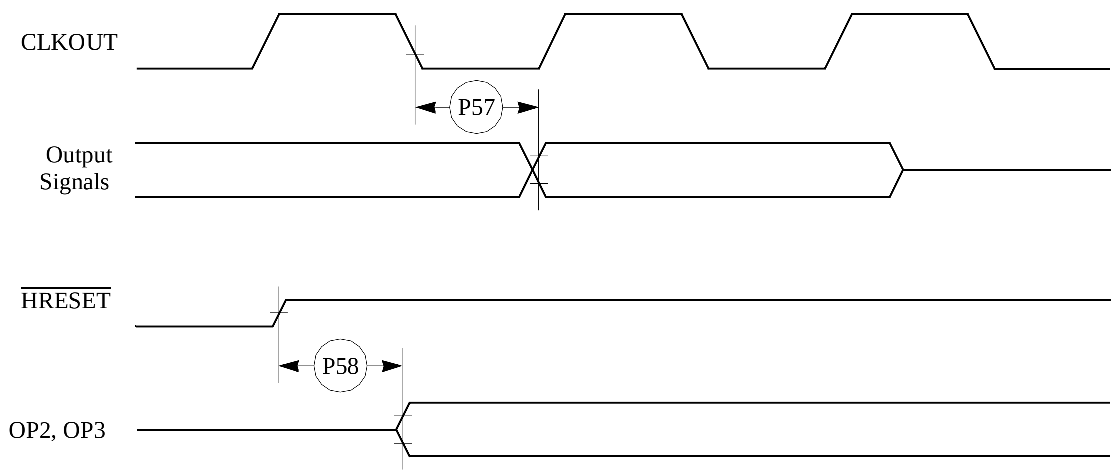

Figure 27. PCMCIA Output Port Timing

Figure 28 provides the PCMCIA output port timing for the MPC850.

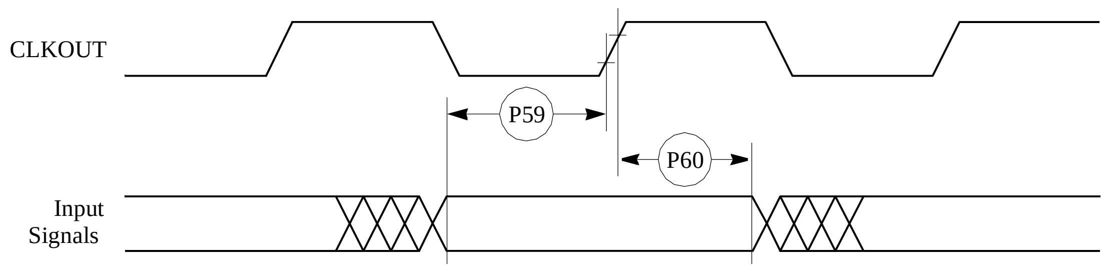

Figure 28. PCMCIA Input Port Timing

Table 11 shows the reset timing for the MPC850.

Table 11. Reset Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	340.00	—	515.00	—	425.00	—	17.000	ns
R72		—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R80	DSDI, DSCK set up	60.00	—	90.00	—	75.00	—	3.000	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns

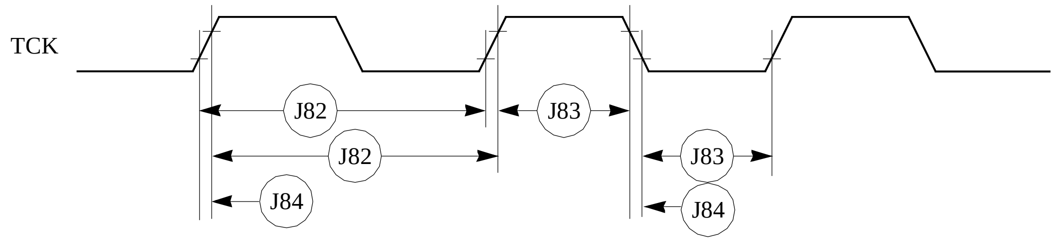

Figure 34. JTAG Test Clock Input Timing

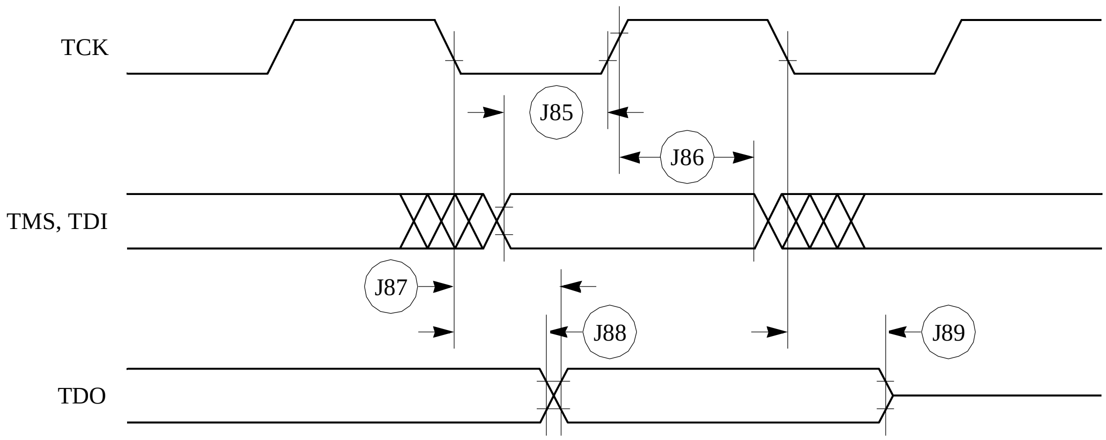

Figure 35. JTAG Test Access Port Timing Diagram

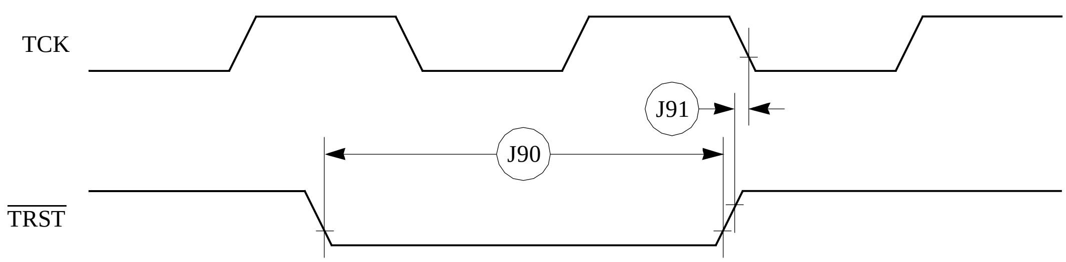

Figure 36. JTAG $\overline{\text{TRST}}$ Timing Diagram

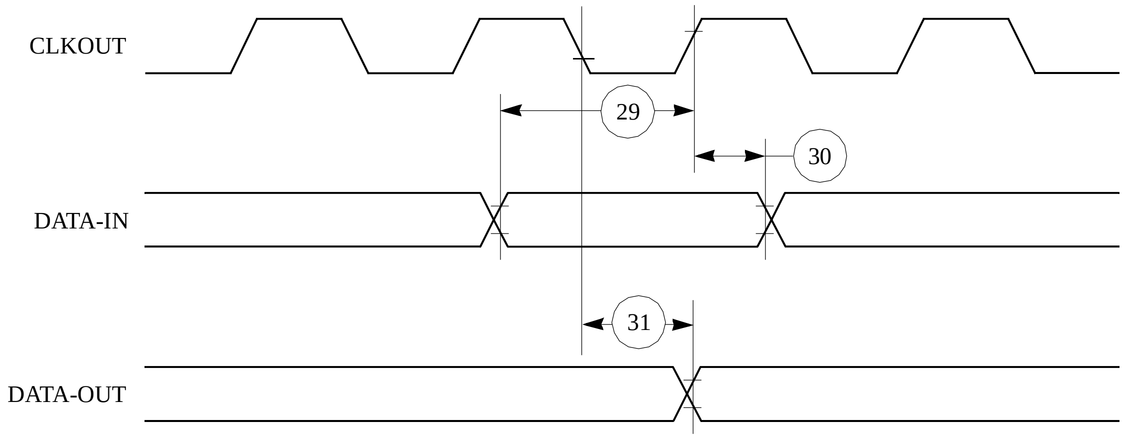

Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Table 14. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7.00	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3.00	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12.00	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12.00	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20.00	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15.00	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7.00	—	ns

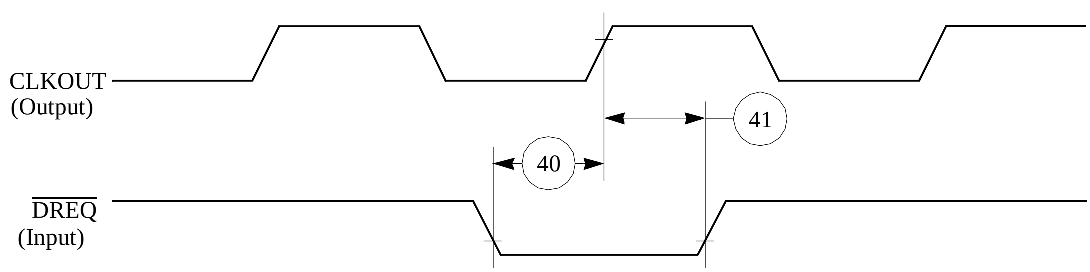

Figure 39. IDMA External Requests Timing Diagram

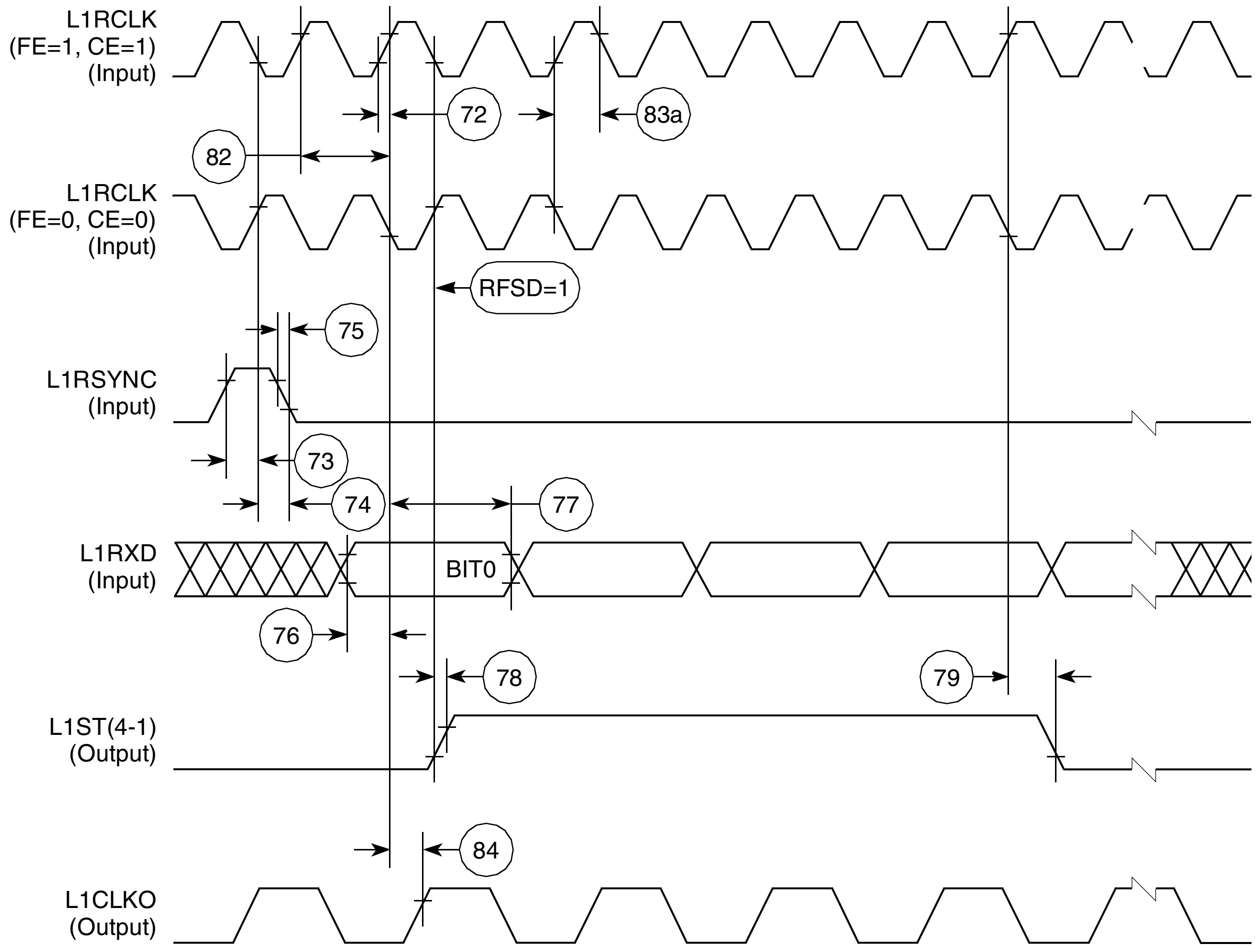

Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

Figure 50 through Figure 52 show the NMSI timings.

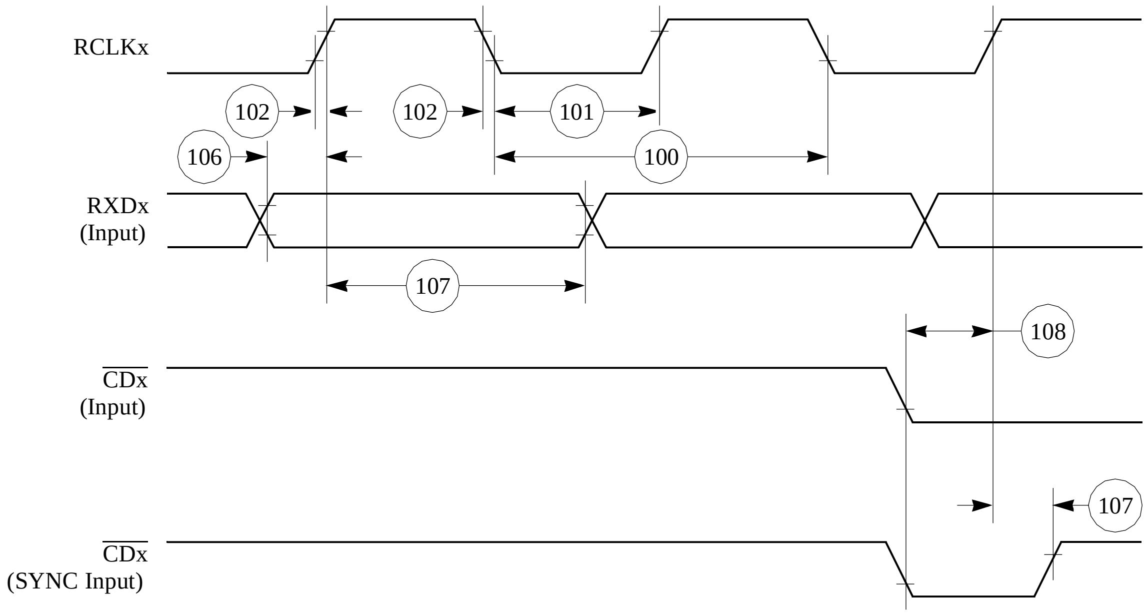

Figure 50. SCC NMSI Receive Timing Diagram

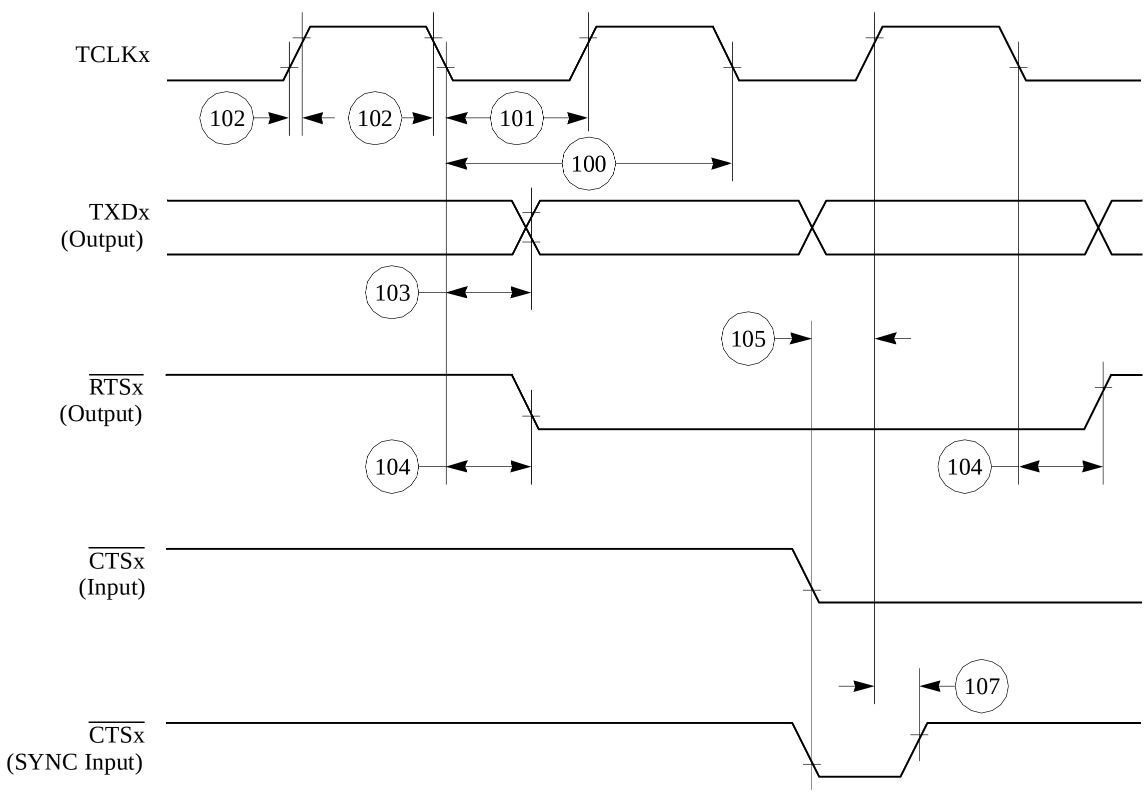

Figure 51. SCC NMSI Transmit Timing Diagram

Table 20. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to $\overline{\text{SDACK}}$ asserted [2]	—	20.00	ns
139	CLKOUT low to $\overline{\text{SDACK}}$ negated [2]	—	20.00	ns

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame destination address into memory.

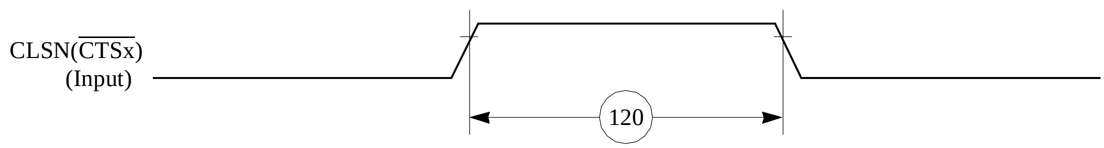

Figure 53. Ethernet Collision Timing Diagram

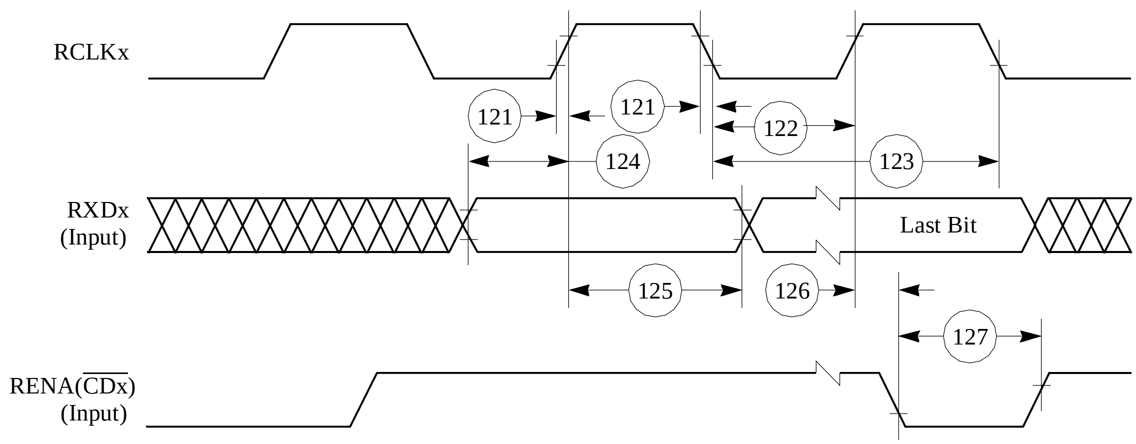

Figure 54. Ethernet Receive Timing Diagram

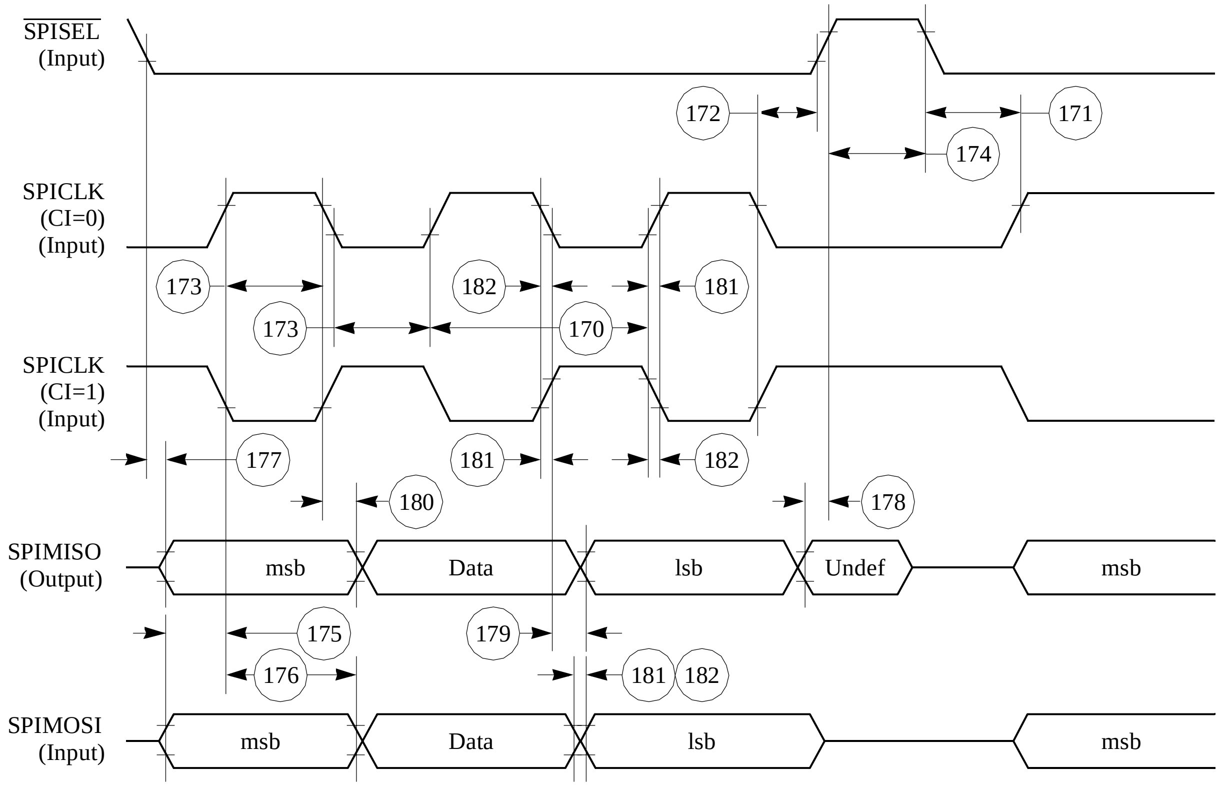

Figure 59. SPI Slave (CP = 0) Timing Diagram

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

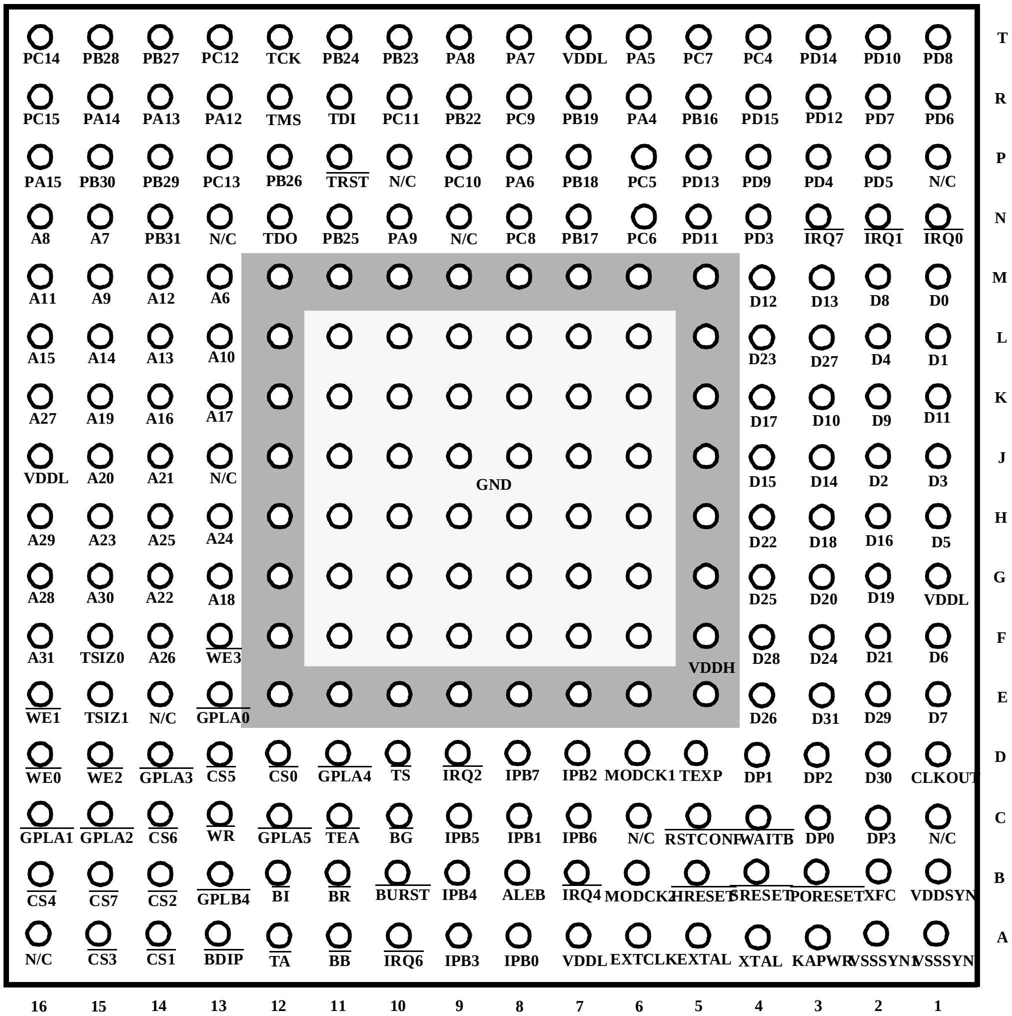

Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface.

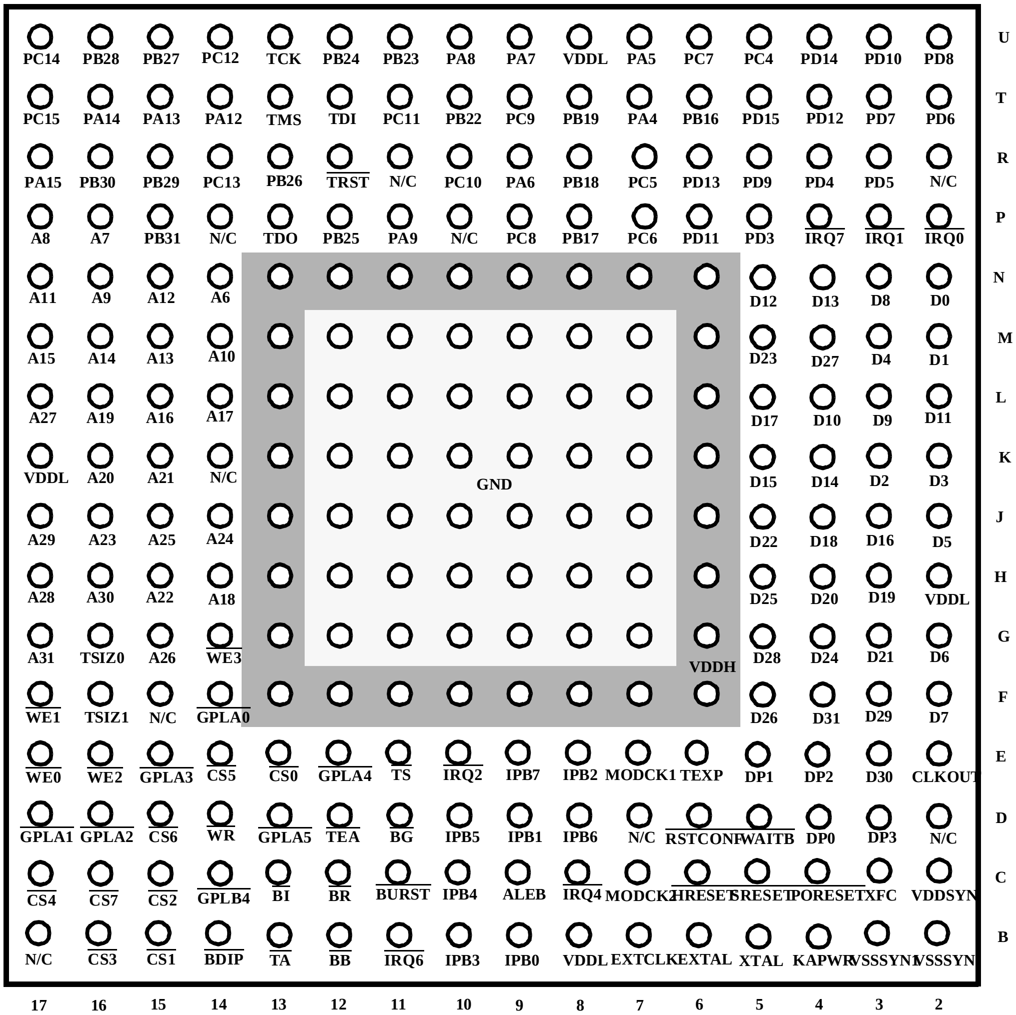

Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

10 Document Revision History

Table 28 lists significant changes between revisions of this document.

Table 28. Document Revision History

Revision	Date	Change
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.
0.2	04/2002	Updated power numbers and added Rev. C
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.