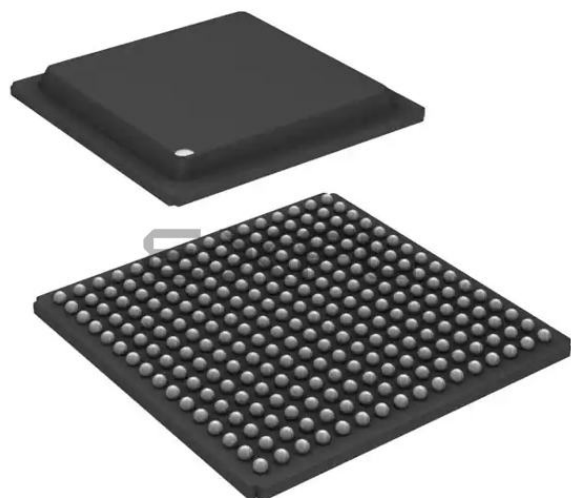




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc850devr80bu

- 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
 - Caches are two-way, set-associative
 - Physically addressed
 - Cache blocks can be updated with a 4-word line burst
 - Least-recently used (LRU) replacement algorithm
 - Lockable one-line granularity
- Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
- MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
 - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
 - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
 - Hardware bus monitor
 - Spurious interrupt monitor
 - Software watchdog
 - Periodic interrupt timer
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
 - Reset controller
 - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
 - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
 - Memory controller programmable to support most size and speed memory interfaces
 - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
 - Variable block sizes, 32 Kbytes to 256 Mbytes
 - Selectable write protection
 - On-chip bus arbiter supports one external bus master
 - Special features for burst mode support
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input low voltage	V _{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V _{IHC}	0.7*(V _{CC})	V _{CC} +0.3	V
Input leakage current, V _{in} = 5.5 V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I _{in}	—	100	μA
Input leakage current, V _{in} = 3.6V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I _{in}	—	10	μA
Input leakage current, V _{in} = 0V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I _{in}	—	10	μA
Input capacitance	C _{in}	—	20	pF
Output high voltage, I _{OH} = -2.0 mA, V _{DDH} = 3.0V except XTAL, XFC, and open-drain pins	V _{OH}	2.4	—	V
Output low voltage CLKOUT ³ I _{OL} = 3.2 mA ¹ I _{OL} = 5.3 mA ² I _{OL} = 7.0 mA PA[14]/ $\overline{\text{USBOE}}$, PA[12]/TXD2 I _{OL} = 8.9 mA $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$	V _{OL}	—	0.5	V

¹ A[6:31], TSIZ0/ $\overline{\text{REG}}$, TSIZ1, D[0:31], DP[0:3]/ $\overline{\text{IRQ}}[3:6]$, RD/ $\overline{\text{WR}}$, BURST, RSV/ $\overline{\text{IRQ2}}$, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/ $\overline{\text{IOIS16_B/AT2}}$, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/ $\overline{\text{PTR/AT3}}$, PA[15]/ $\overline{\text{USBRXD}}$, PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/TOUT1/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/TOUT2/TIN4, PB[31]/SPISEL, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/BRGO1, PB[26]/I2CSCL/BRGO2, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/SDACK1, PB[22]/SMSYN2/SDACK2, PB[19]/L1ST1, PB[18]/RTS2/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/DREQ0/L1ST5, PC[14]/DREQ1/RTS2/L1ST6, PC[13]/L1ST7/RTS3, PC[12]/L1RQa/L1ST8, PC[11]/ $\overline{\text{USBRXP}}$, PC[10]/TGATE1/ $\overline{\text{USBRXN}}$, PC[9]/CTS2, PC[8]/CD2/TGATE1, PC[7]/ $\overline{\text{USBTXP}}$, PC[6]/ $\overline{\text{USBTXN}}$, PC[5]/CTS3/L1TSYNCA/SDACK1, PC[4]/CD3/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

² $\overline{\text{BDIP/GPL_B5}}$, $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ/ $\overline{\text{IRQ6}}$, $\overline{\text{CS}}[0:5]$, $\overline{\text{CS6/CE1_B}}$, $\overline{\text{CS7/CE2_B}}$, $\overline{\text{WE0/BS_AB0/IORD}}$, $\overline{\text{WE1/BS_AB1/IOWR}}$, $\overline{\text{WE2/BS_AB2/PCOE}}$, $\overline{\text{WE3/BS_AB3/PCWE}}$, $\overline{\text{GPL_A0/GPL_B0}}$, $\overline{\text{OE/GPL_A1/GPL_B1}}$, $\overline{\text{GPL_A2:3/GPL_B2:3/CS2:3}}$, UPWAITA/GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/ $\overline{\text{DSCK/AT1}}$, OP2/MODCK1/STS, OP3/MODCK2/DSDO

³ The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, I_{OH} and I_{OL} for Clkout should be extracted from the IBIS model at any output voltage level.

5 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (P_D \cdot \theta_{JA})(1)$$

where

$$T_A = \text{Ambient temperature, } ^\circ\text{C}$$

Table 6. Bus Operation Timing ¹

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B1	CLKOUT period	20	—	30.30	—	25	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	—	50.00	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	—	50.00	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) ²	-0.60	0.60	-0.60	0.60	-0.60	0.60	—	50.00	ns
B1d	CLKOUT phase jitter ²	-2.00	2.00	-2.00	2.00	-2.00	2.00	—	50.00	ns
B1e	CLKOUT frequency jitter (MF < 10) ²	—	0.50	—	0.50	—	0.50	—	50.00	%
B1f	CLKOUT frequency jitter (10 < MF < 500) ²	—	2.00	—	2.00	—	2.00	—	50.00	%
B1g	CLKOUT frequency jitter (MF > 500) ²	—	3.00	—	3.00	—	3.00	—	50.00	%
B1h	Frequency jitter on EXTCLK ³	—	0.50	—	0.50	—	0.50	—	50.00	%
B2	CLKOUT pulse width low	8.00	—	12.12	—	10.00	—	—	50.00	ns
B3	CLKOUT width high	8.00	—	12.12	—	10.00	—	—	50.00	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B7	CLKOUT to A[6–31], RD $\overline{\text{WR}}$, BURST, D[0–31], DP[0–3] invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3], BDIP, PTR invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS[0–1], VF[0–2] IWP[0–2], LWP[0–1], STS invalid ⁴	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B8	CLKOUT to A[6–31], RD $\overline{\text{WR}}$, BURST, D[0–31], DP[0–3] valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3] BDIP, PTR valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8b	CLKOUT to BR, BG, VFLS[0–1], VF[0–2], IWP[0–2], FRZ, LWP[0–1], STS valid ⁴	5.00	11.74	7.58	14.33	6.25	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B28c	CLKOUT falling edge to $\overline{\text{WE}}[0-3]$ negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	—	14.00	—	18.00	—	16.00	0.375	50.00	ns
B29	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29a	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29b	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29c	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29d	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29e	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29f	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns
B29g	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns

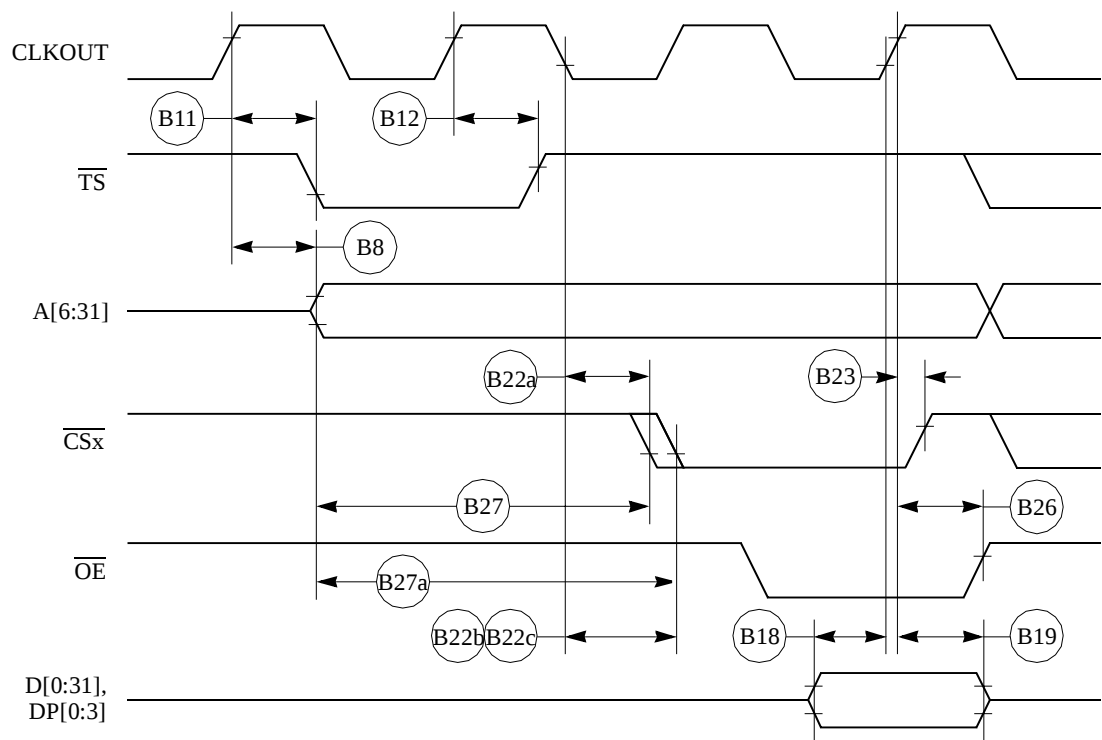


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

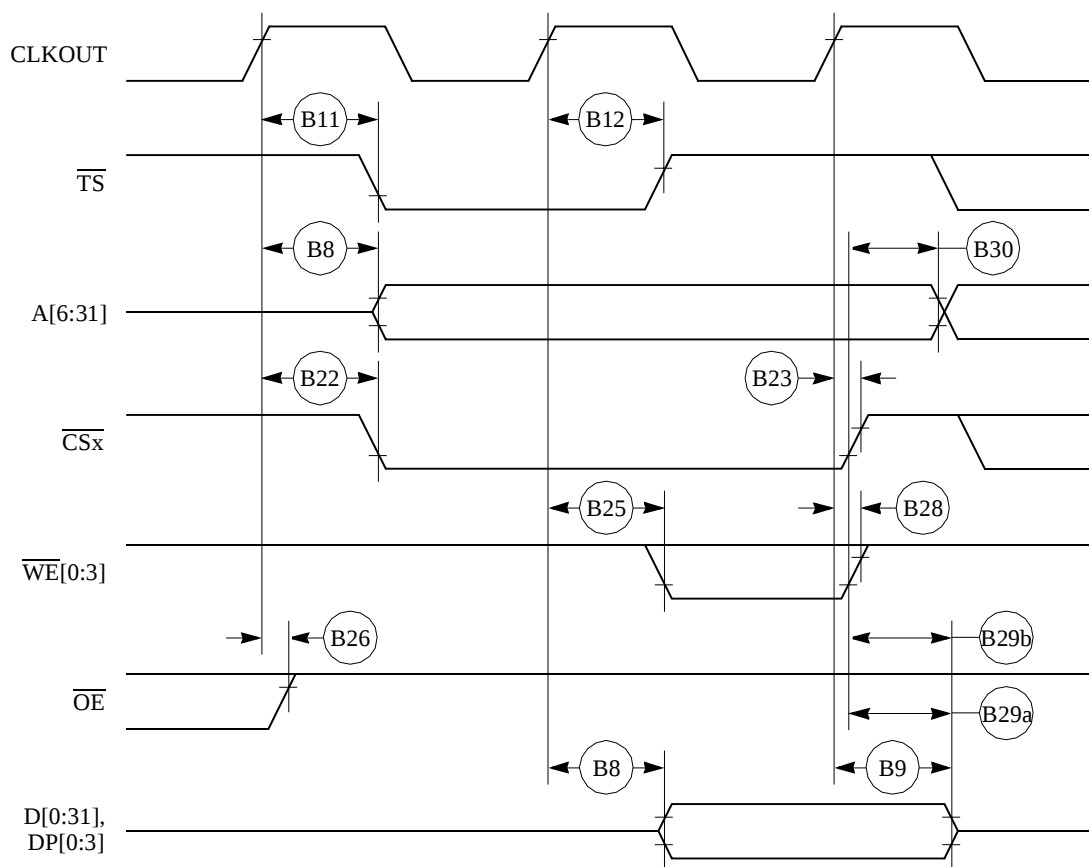


Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

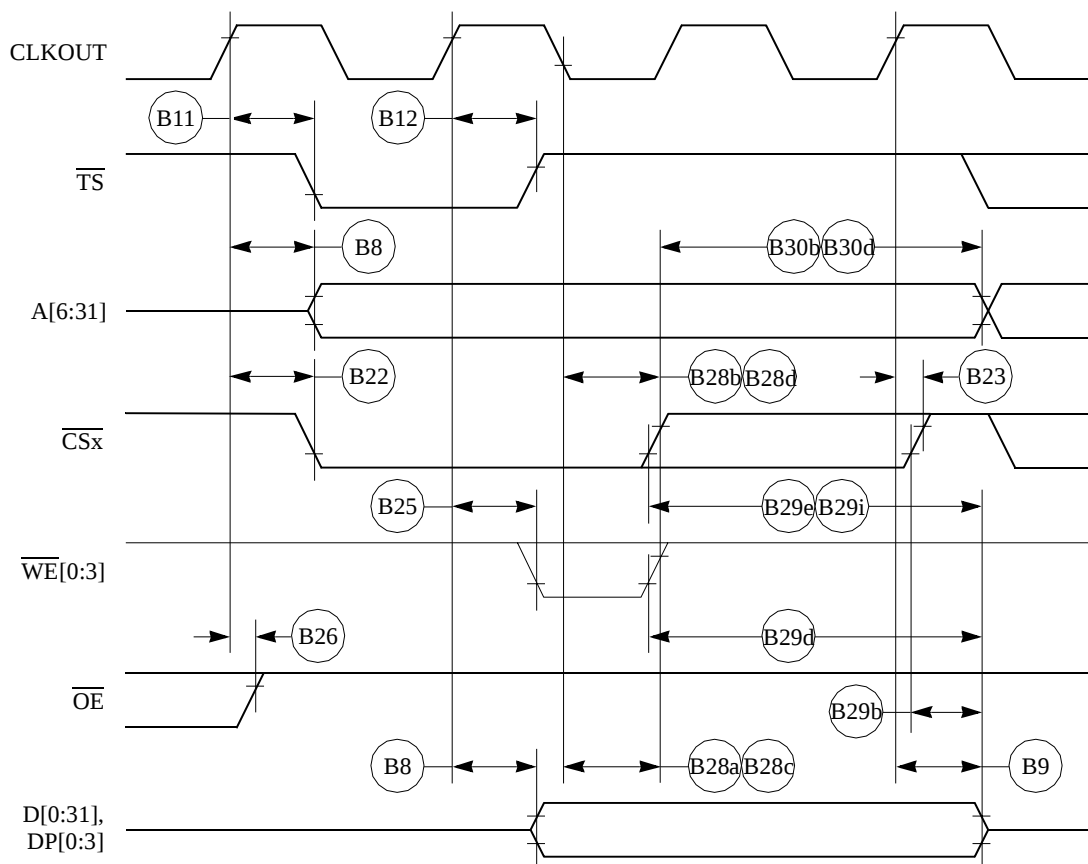


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

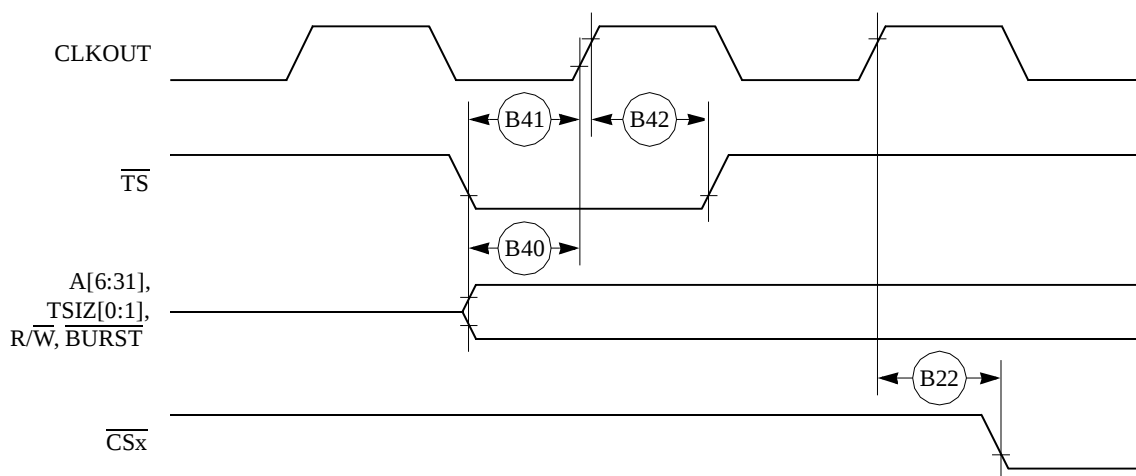


Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.

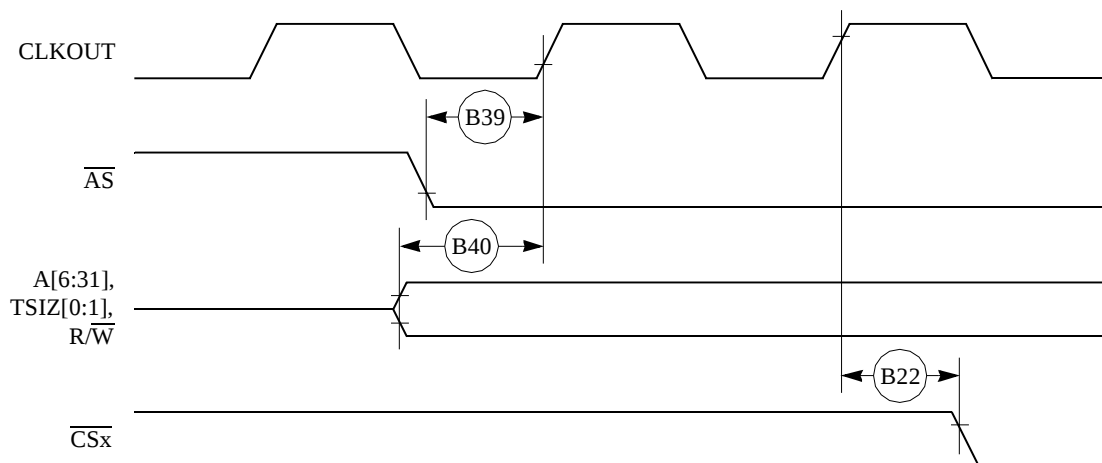


Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 21 provides the timing for the asynchronous external master control signals negation.

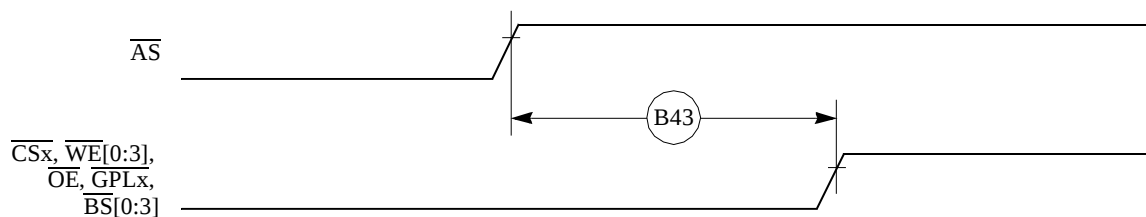


Figure 21. Asynchronous External Master—Control Signals Negation Timing

Table 8 shows the PCMCIA timing for the MPC850.

Table 8. PCMCIA Timing

Num	Characteristic	50MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
P44	A[6–31], $\overline{\text{REG}}$ valid to PCMCIA strobe asserted. ¹	13.00	—	21.00	—	17.00	—	0.750	ns
P45	A[6–31], $\overline{\text{REG}}$ valid to ALE negation. ¹	18.00	—	28.00	—	23.00	—	1.000	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid.	6.00	—	9.00	—	7.00	—	0.250	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time.	—	11.00	—	11.00	—	11.00	—	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time.	2.00	11.00	2.00	11.00	2.00	11.00	—	ns
P52	CLKOUT to ALE assert time	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P53	CLKOUT to ALE negate time	—	13.00	—	16.00	—	14.00	0.250	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D[0–31] invalid. ¹	3.00	—	6.00	—	4.00	—	0.250	ns
P55	$\overline{\text{WAIT_B}}$ valid to CLKOUT rising edge. ¹	8.00	—	8.00	—	8.00	—	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAIT_B}}$ invalid. ¹	2.00	—	2.00	—	2.00	—	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAIT_B}}$ signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAIT_B}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC850 PowerQUICC User's Manual.

Figure 31 shows the reset timing for the data bus configuration.

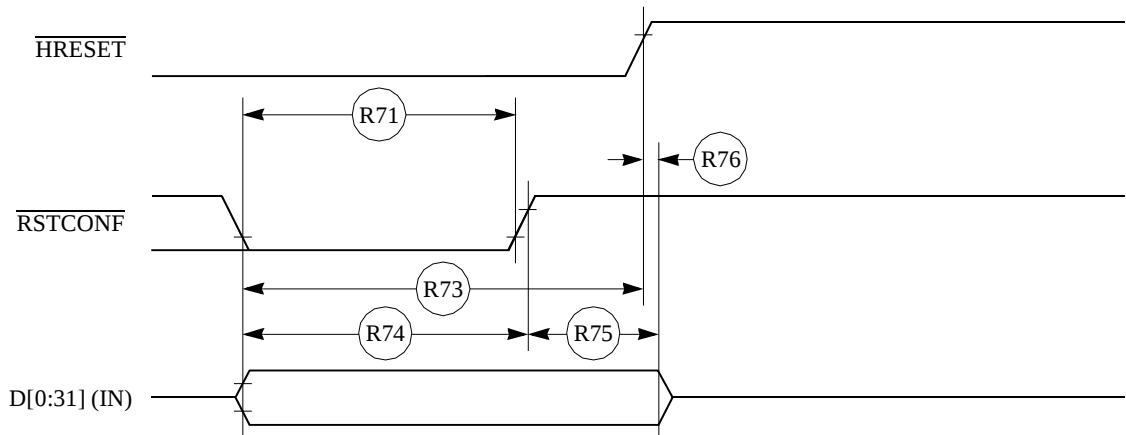


Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

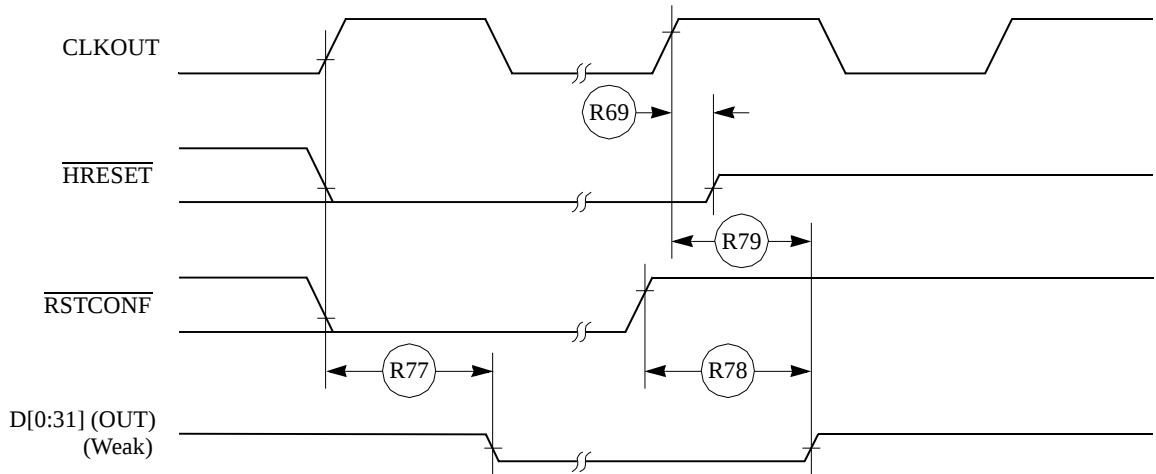


Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

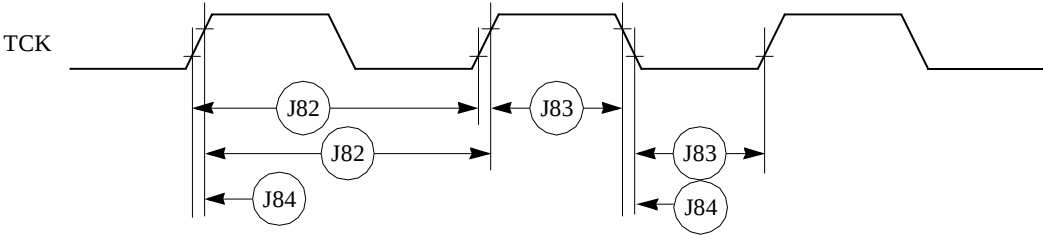


Figure 34. JTAG Test Clock Input Timing

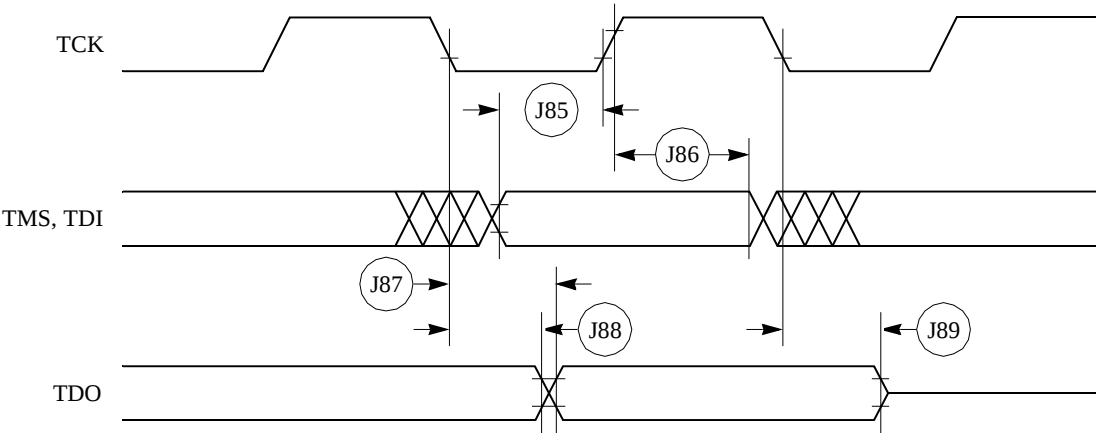


Figure 35. JTAG Test Access Port Timing Diagram

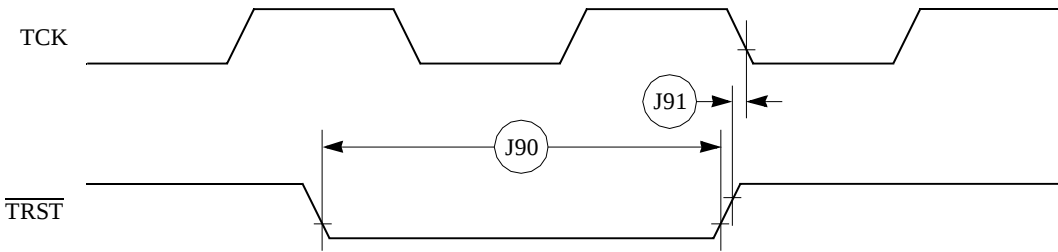


Figure 36. JTAG TRST Timing Diagram

8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns

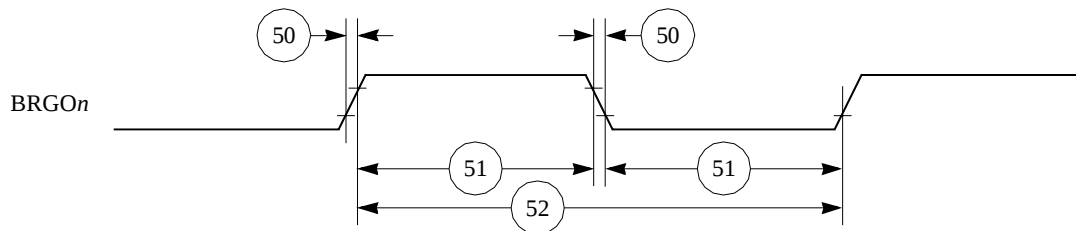


Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Table 16. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/TGATE rise and fall time	10.00	—	ns
62	TIN/TGATE low time	1.00	—	clk
63	TIN/TGATE high time	2.00	—	clk
64	TIN/TGATE cycle time	3.00	—	clk
65	CLKO high to TOUT valid	3.00	25.00	ns

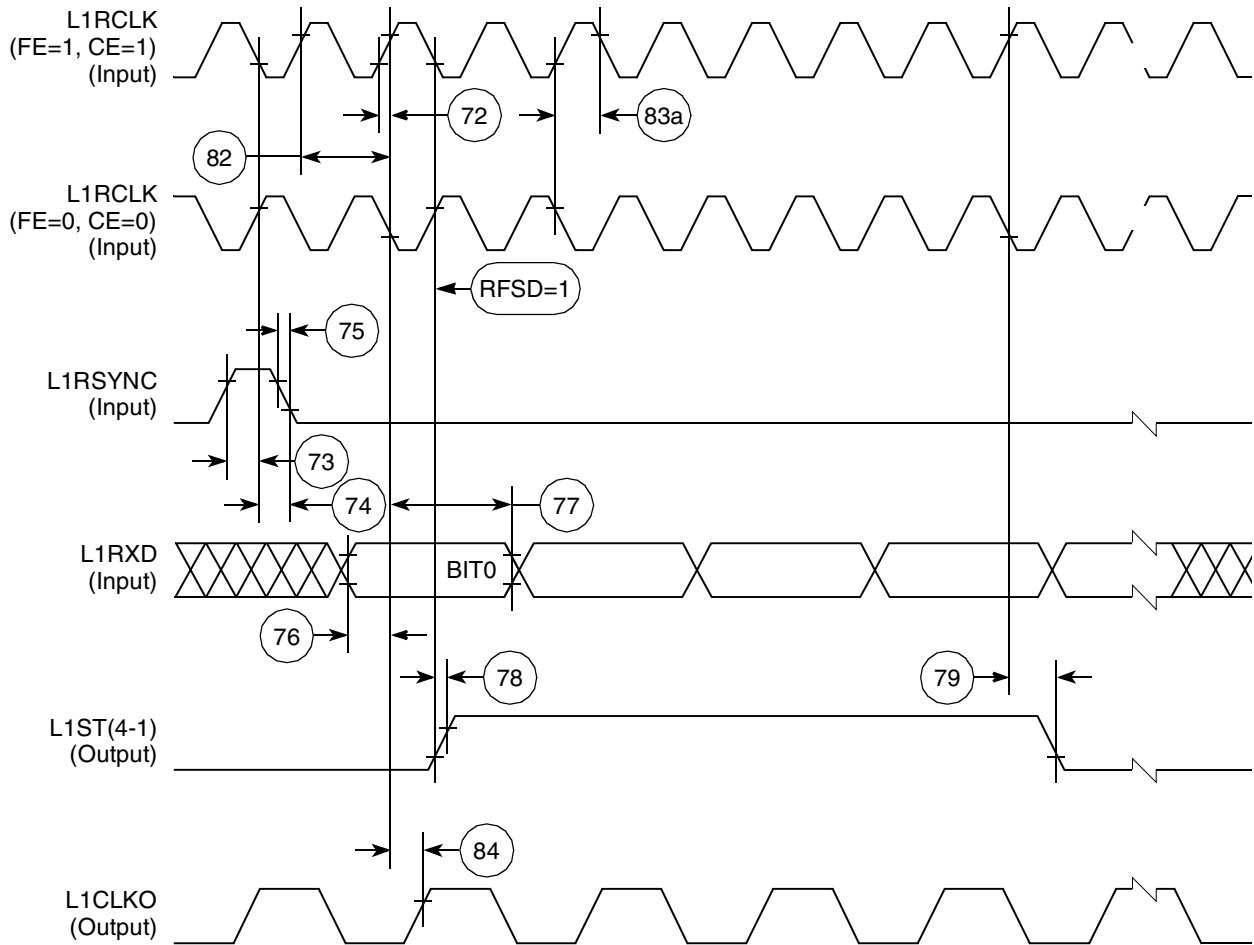


Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

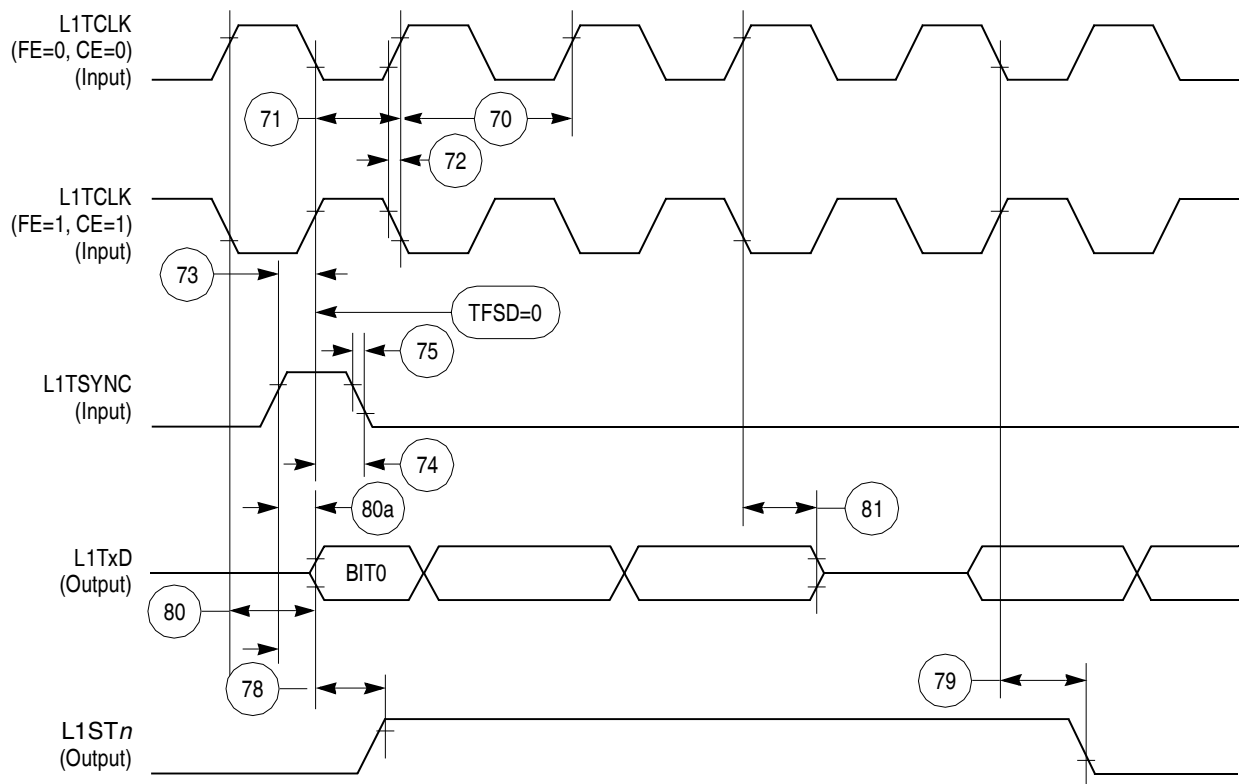


Figure 47. SI Transmit Timing Diagram

8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

Table 23. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t _{cyc}
171	Slave enable lead time	15.00	—	ns
172	Slave enable lag time	15.00	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t _{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t _{cyc}
175	Slave data setup time (inputs)	20.00	—	ns
176	Slave data hold time (inputs)	20.00	—	ns
177	Slave access time	—	50.00	ns
178	Slave SPI MISO disable time	—	50.00	ns
179	Slave data valid (after SPICLK edge)	—	50.00	ns
180	Slave data hold time (outputs)	0.00	—	ns
181	Rise time (input)	—	15.00	ns
182	Fall time (input)	—	15.00	ns

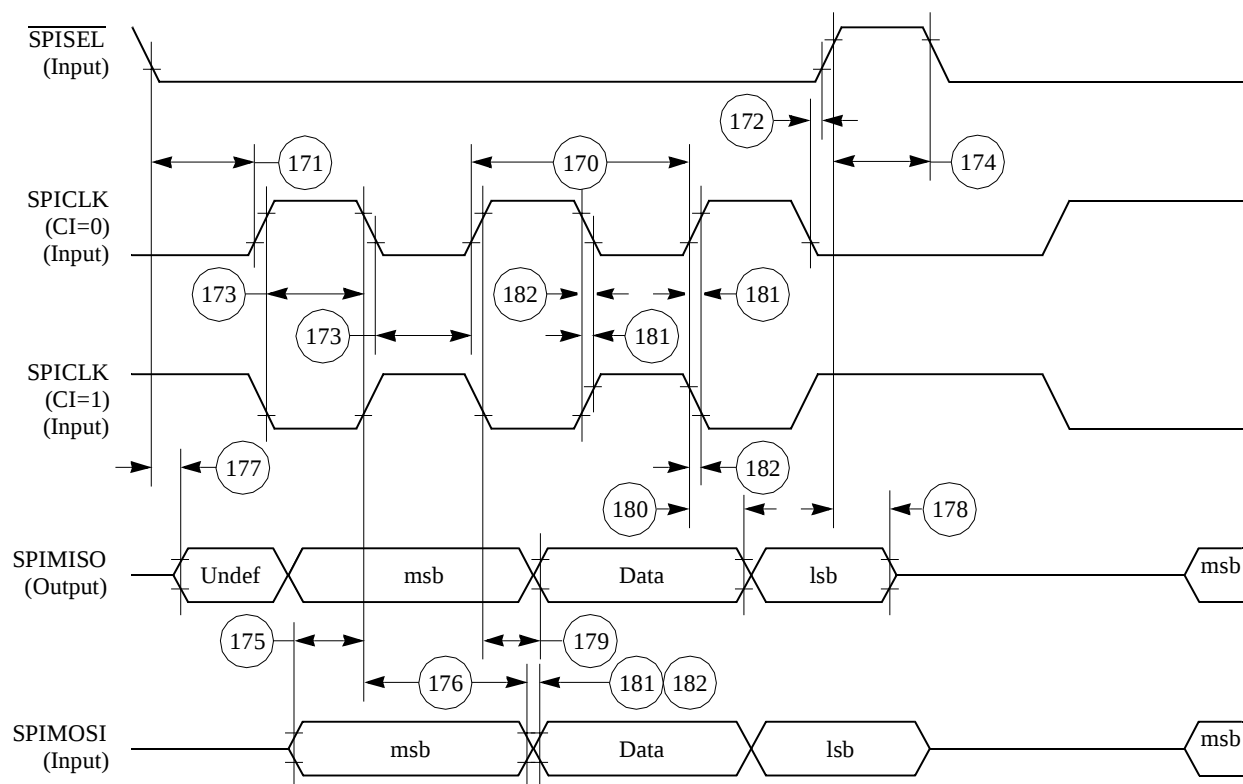


Figure 60. SPI Slave (CP = 1) Timing Diagram

8.11 I²C AC Electrical Specifications

Table 24 provides the I²C (SCL < 100 KHz) timings.

Table 24. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) ¹	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	—	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	—	ns
209	SDL/SCL rise time	—	1.00	μs

9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivatives

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

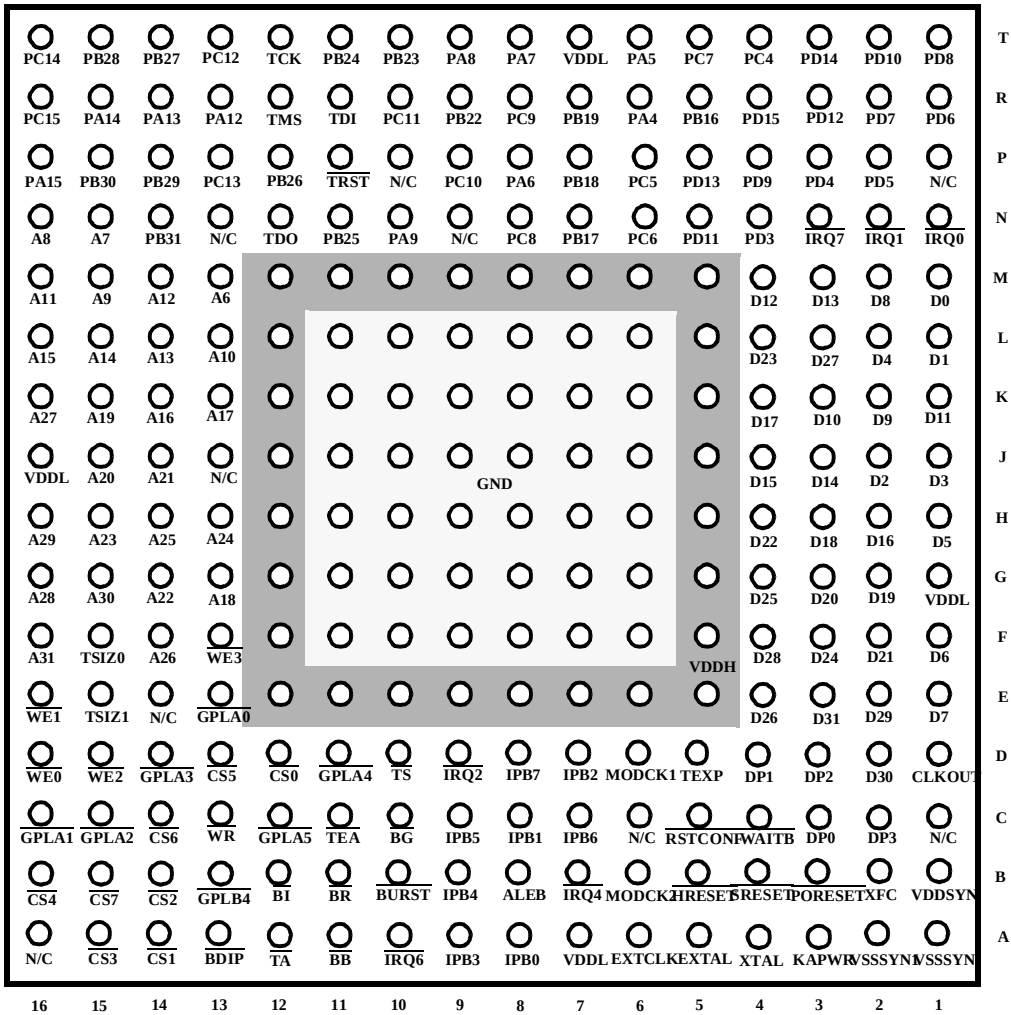
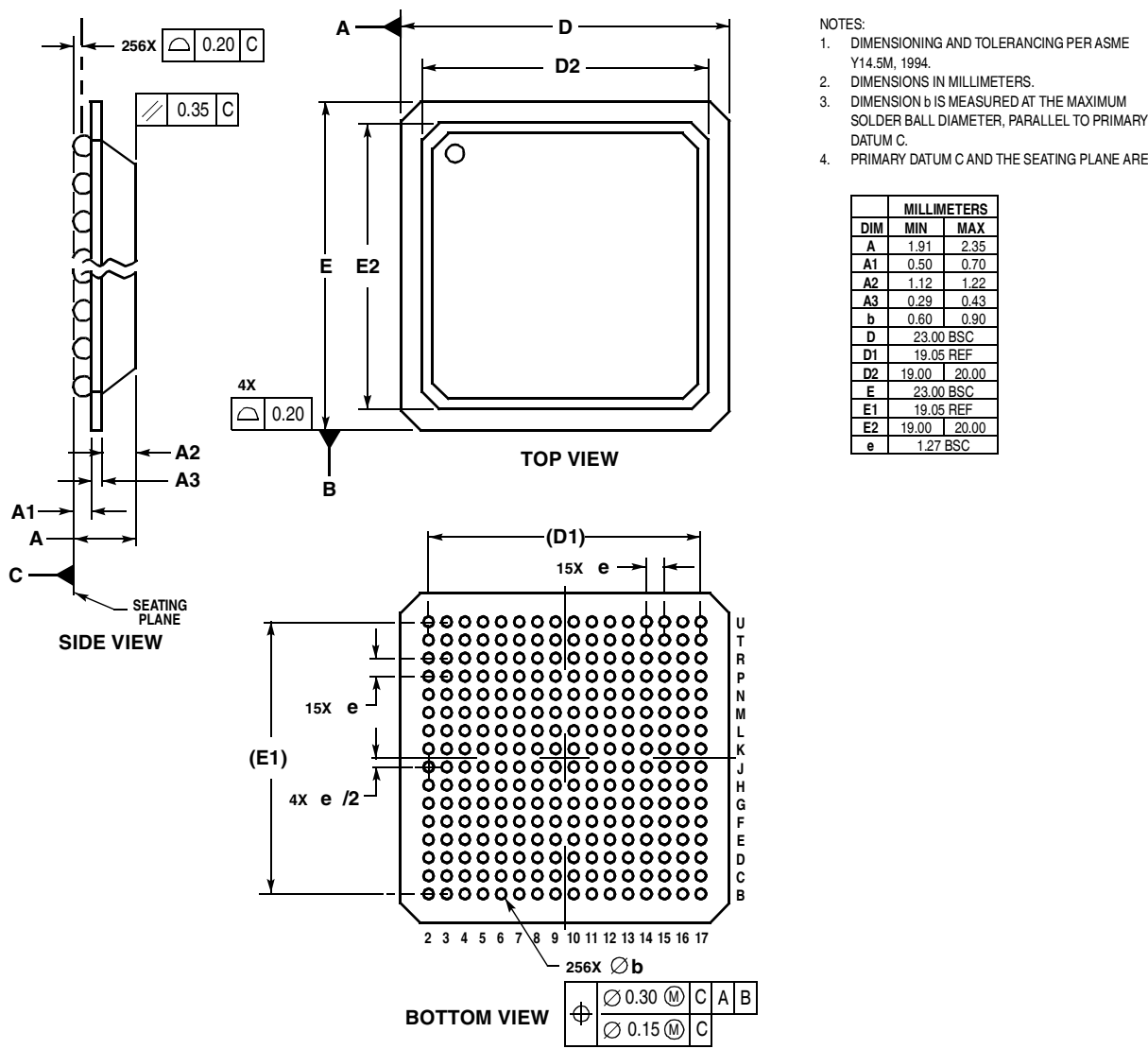


Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

Figure 65 shows the JEDEC package dimensions of the PBGA.



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Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard

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