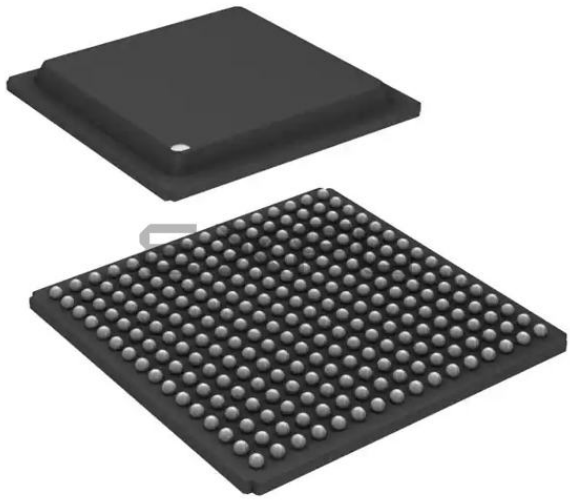

**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 50MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 256-BBGA |
| Supplier Device Package | 256-PBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc850dslzq50bu |

$\theta_{JA}$ = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between $P_D$ and $T_J$ is:

$P_D = K \div (T_J + 273°C)$(2)

Solving equations (1) and (2) for K gives:

$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$(3)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 5.1 Layout Practices

Each $V_{CC}$ pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{CC}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$ and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

Figure 4 provides the timing for the synchronous output signals.

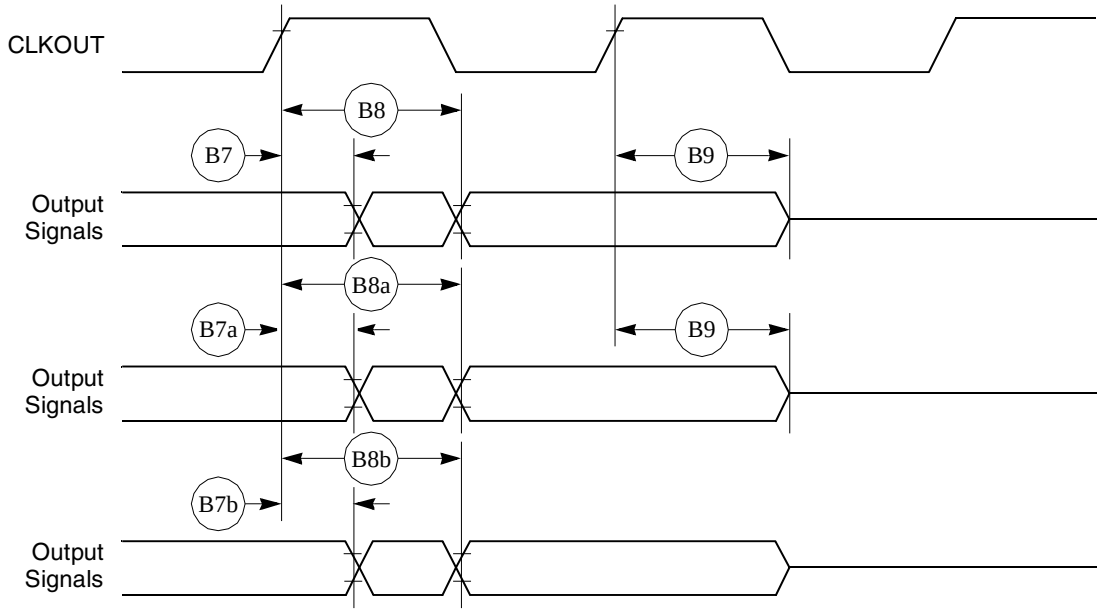


**Figure 4. Synchronous Output Signals Timing**

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.

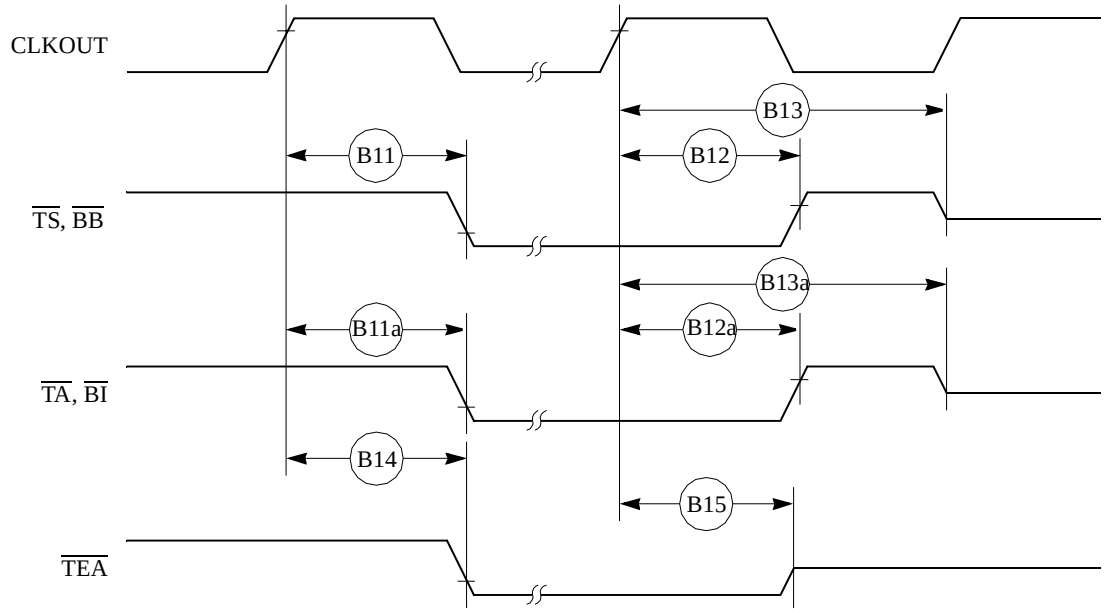


**Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing**

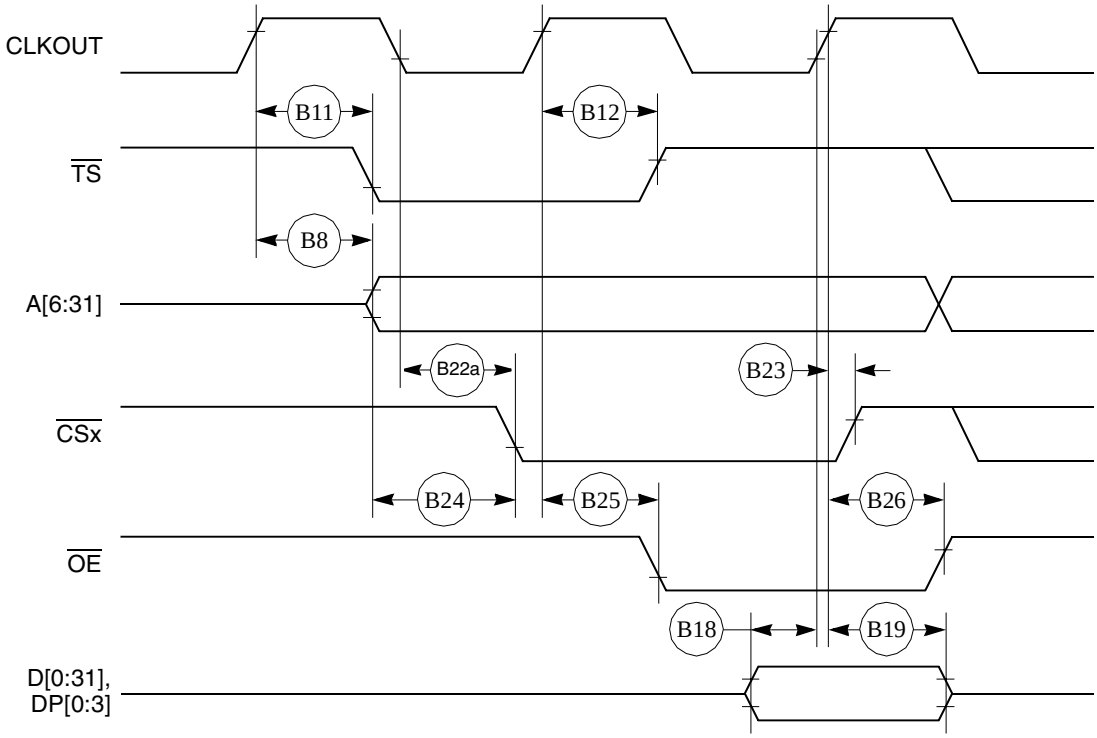


**Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)**

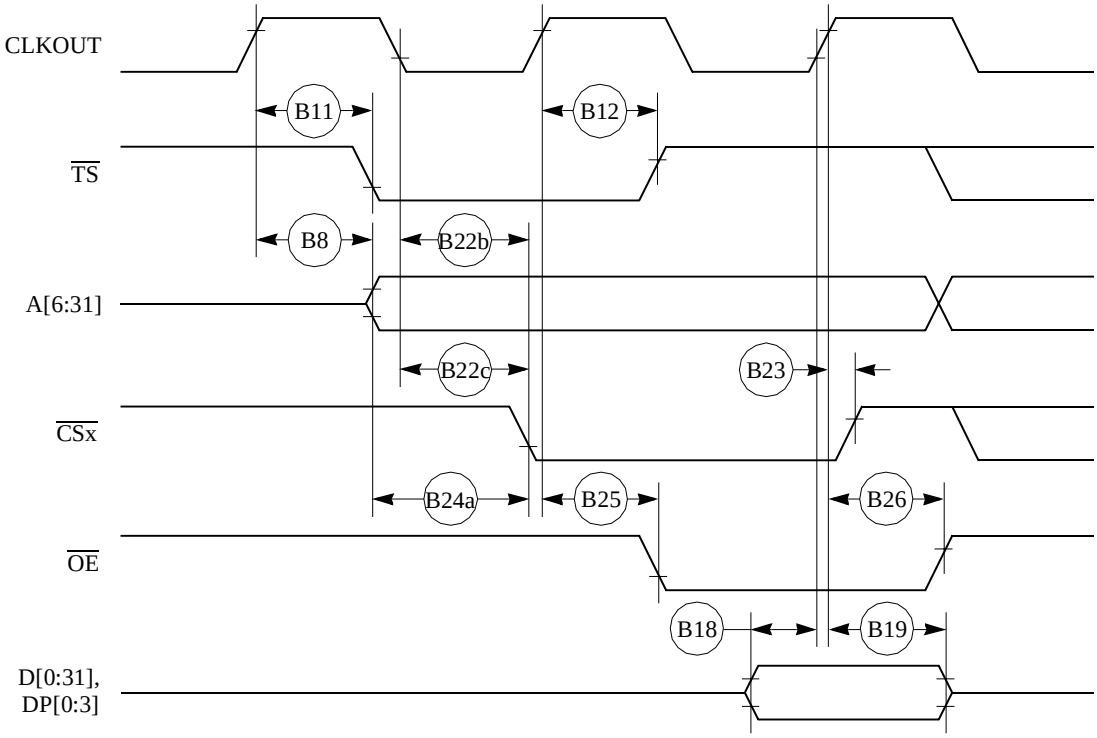


**Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)**

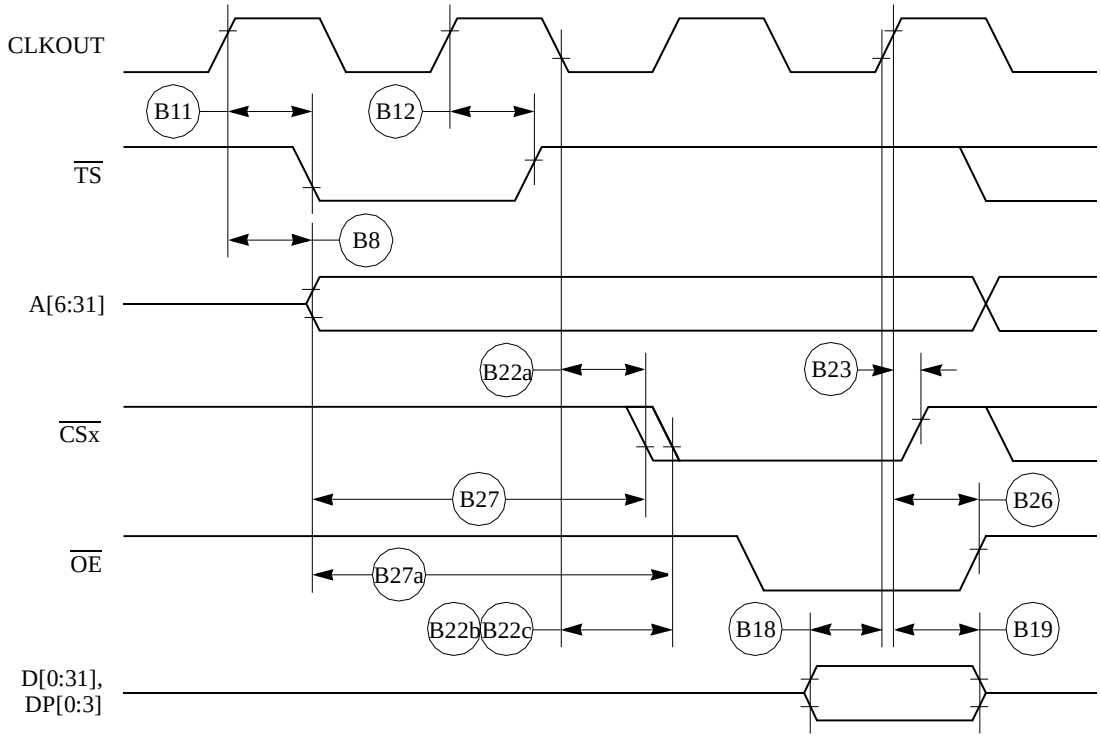


**Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)**

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

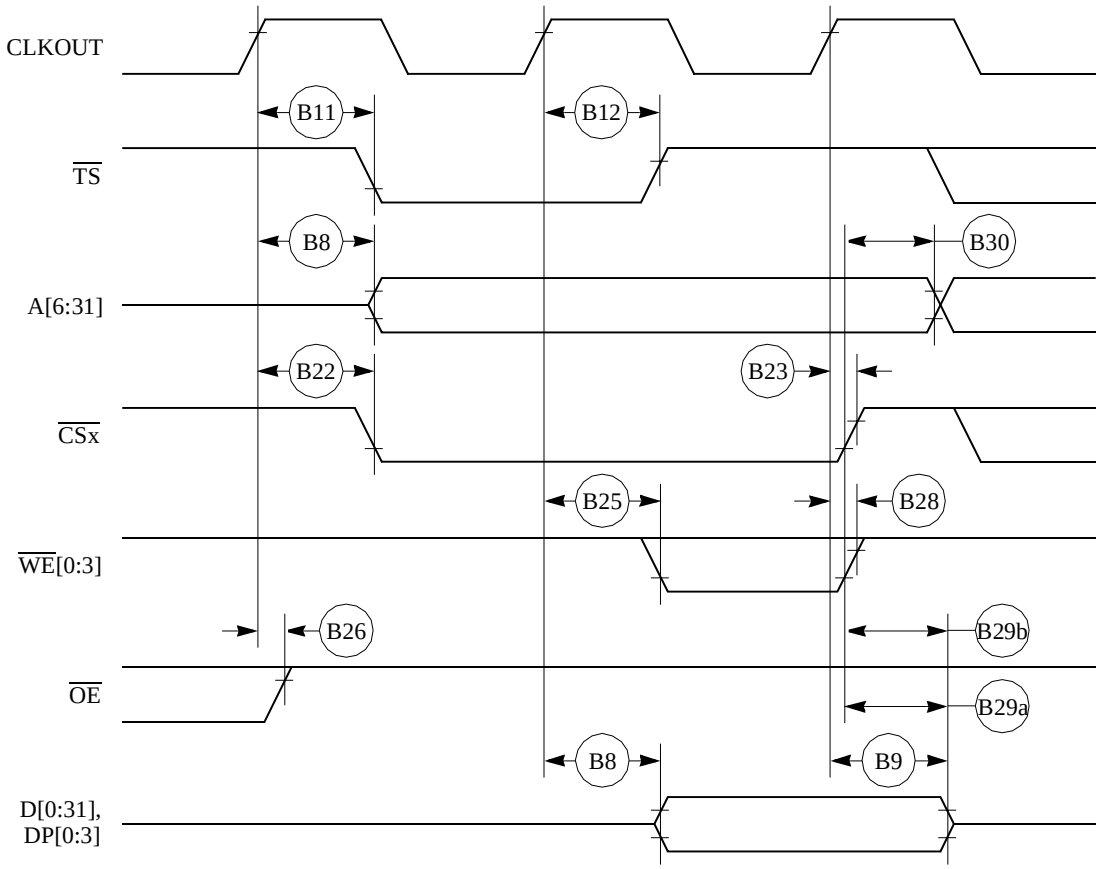


**Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)**

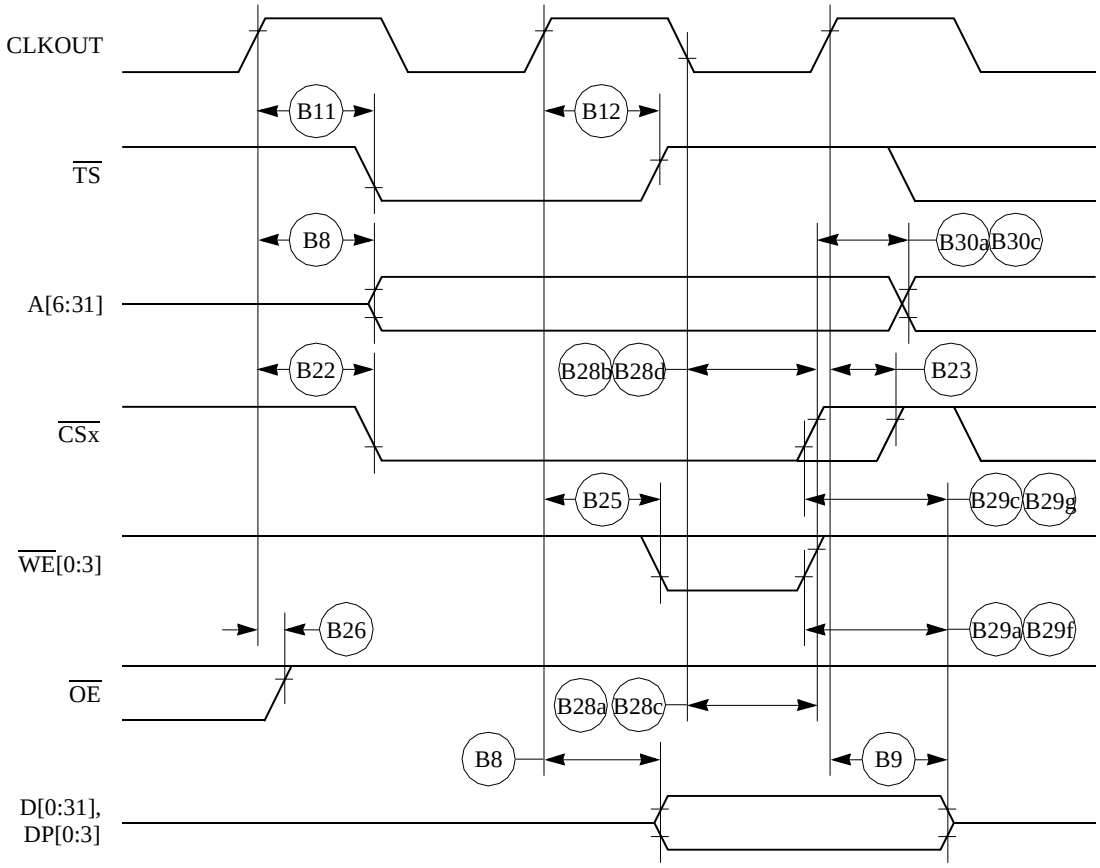


**Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)**

Figure 17 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

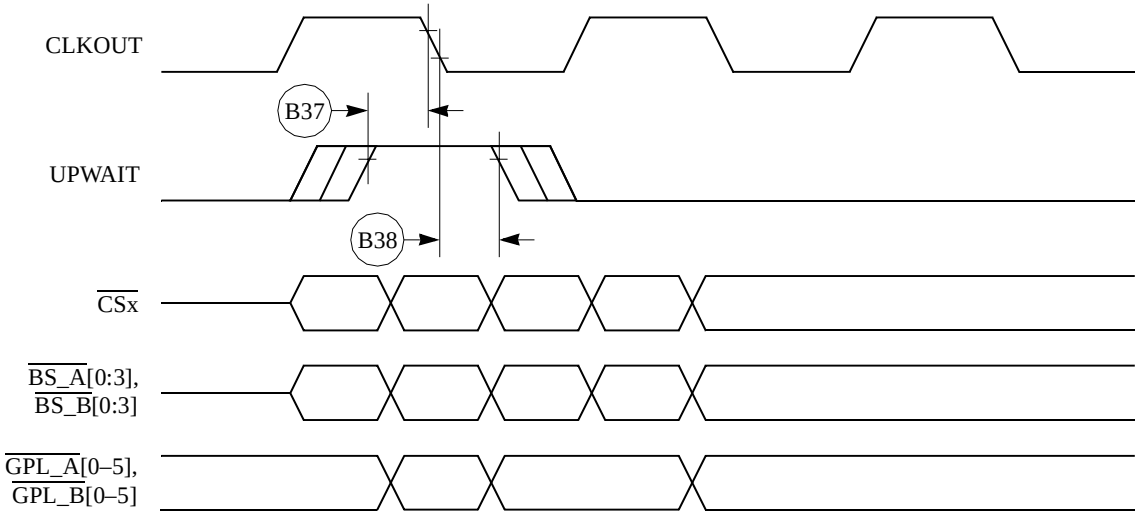


**Figure 17. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing**

Figure 18 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

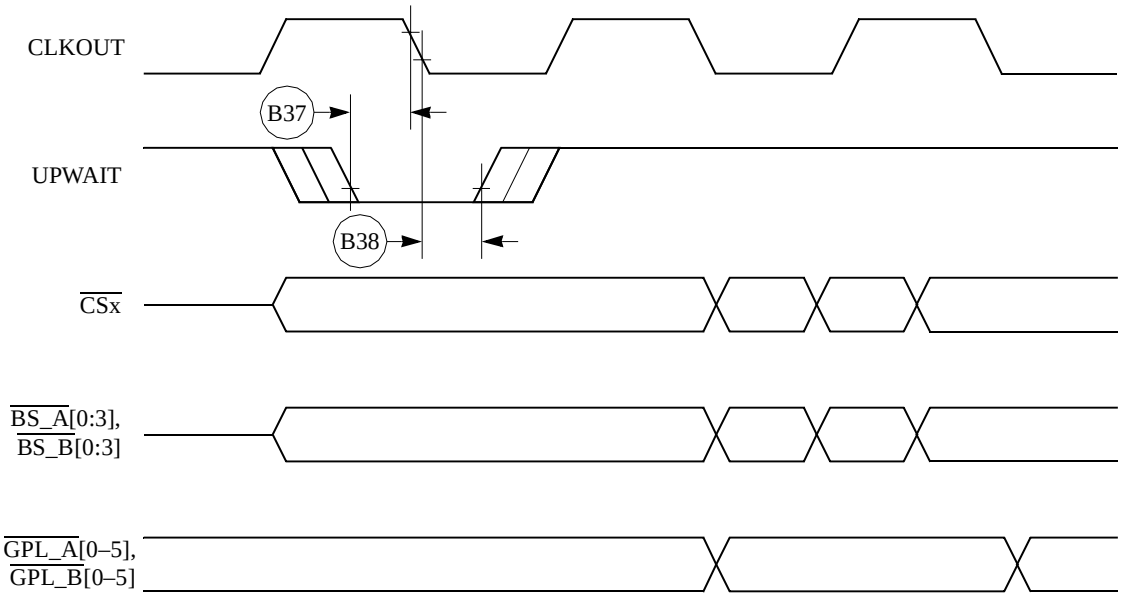


**Figure 18. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing**

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

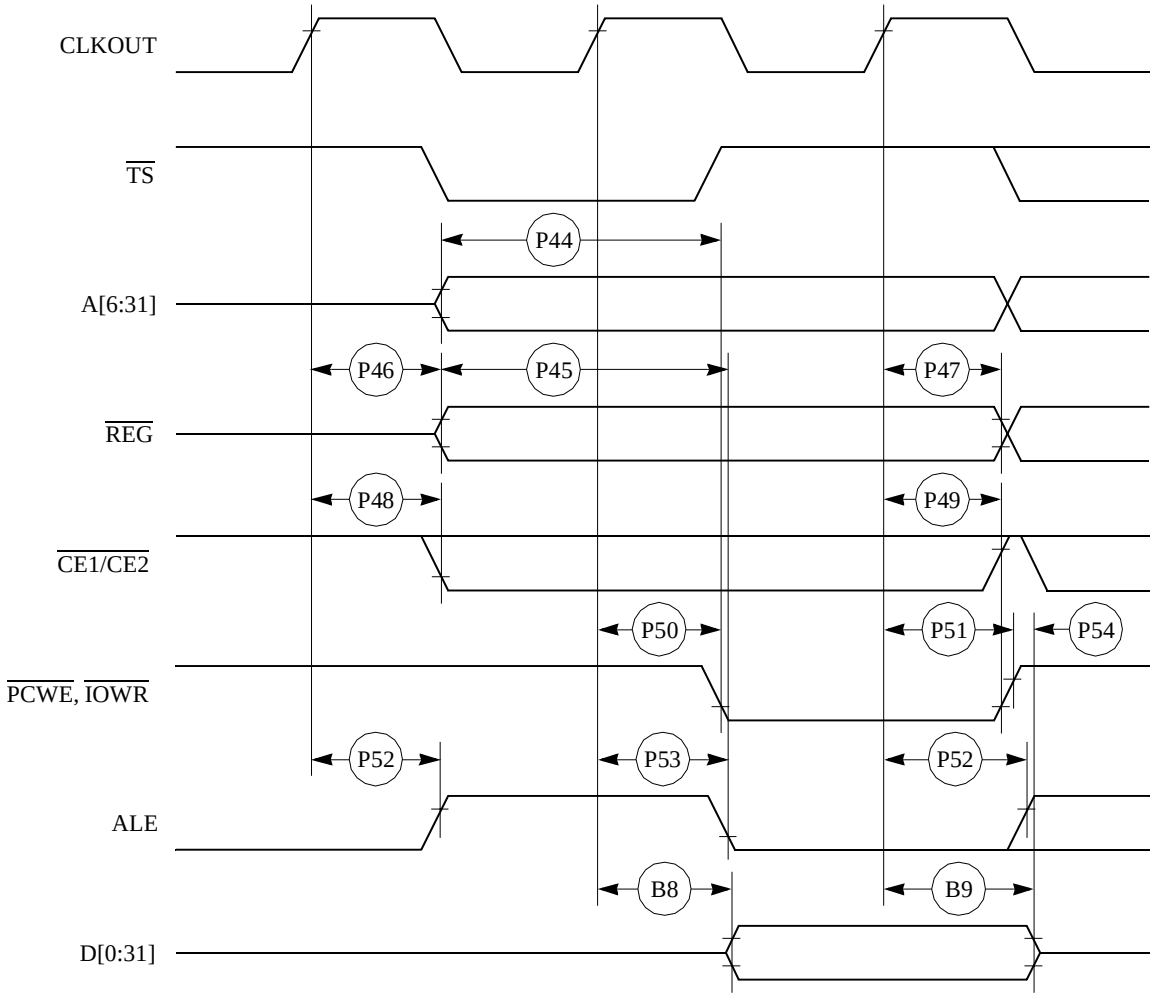


**Figure 25. PCMCIA Access Cycles Timing External Bus Write**

Figure 26 provides the PCMCIA WAIT signals detection timing.

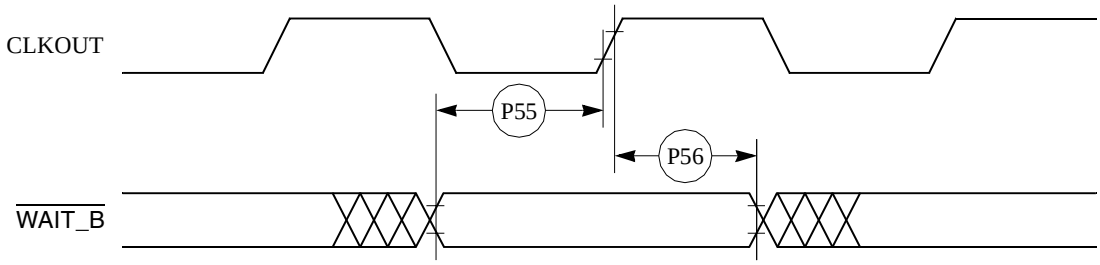


**Figure 26. PCMCIA WAIT Signal Detection Timing**

Table 10 shows the debug port timing for the MPC850.

**Table 10. Debug Port Timing**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| D61 | DSCK cycle time | 60.00 | — | 91.00 | — | 75.00 | — | ns |
| D62 | DSCK clock pulse width | 25.00 | — | 38.00 | — | 31.00 | — | ns |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | 0.00 | 3.00 | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| D65 | DSDI data hold time | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | 0.00 | 15.00 | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | 0.00 | 2.00 | 0.00 | 2.00 | ns |

Figure 29 provides the input timing for the debug port clock.

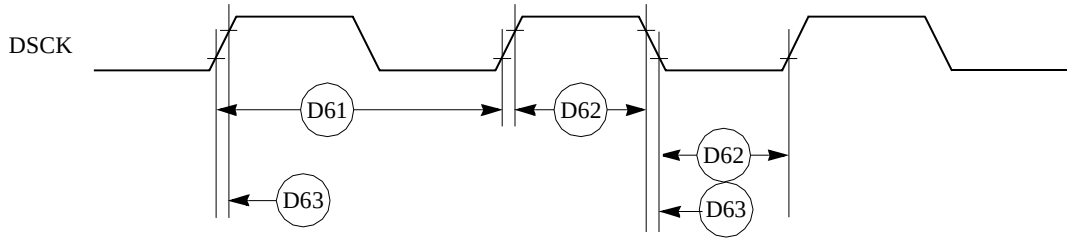


**Figure 29. Debug Port Clock Input Timing**

Figure 30 provides the timing for the debug port.

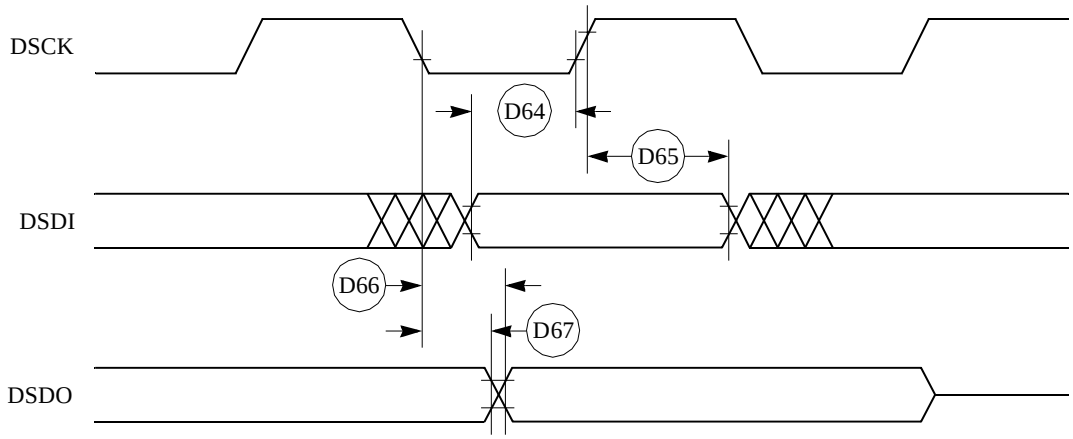


**Figure 30. Debug Port Timings**

Figure 31 shows the reset timing for the data bus configuration.

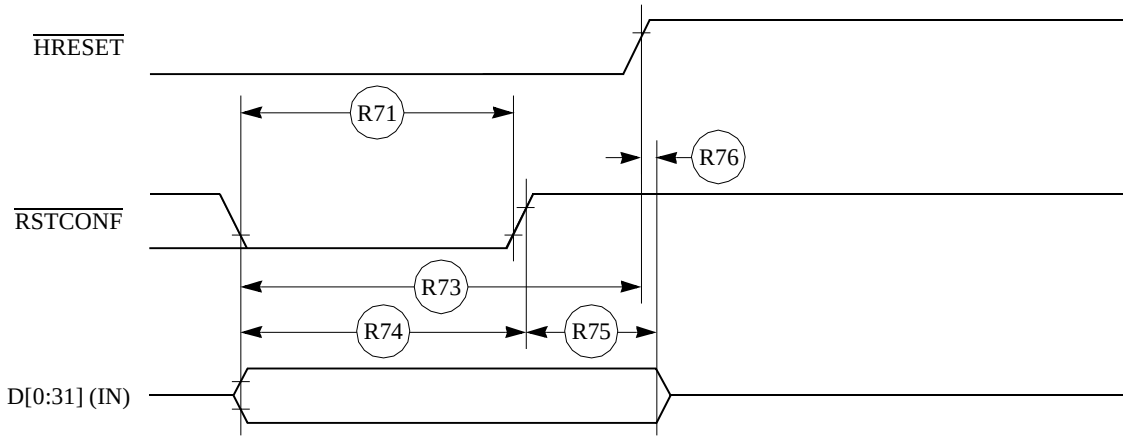


**Figure 31. Reset Timing—Configuration from Data Bus**

Figure 32 provides the reset timing for the data bus weak drive during configuration.

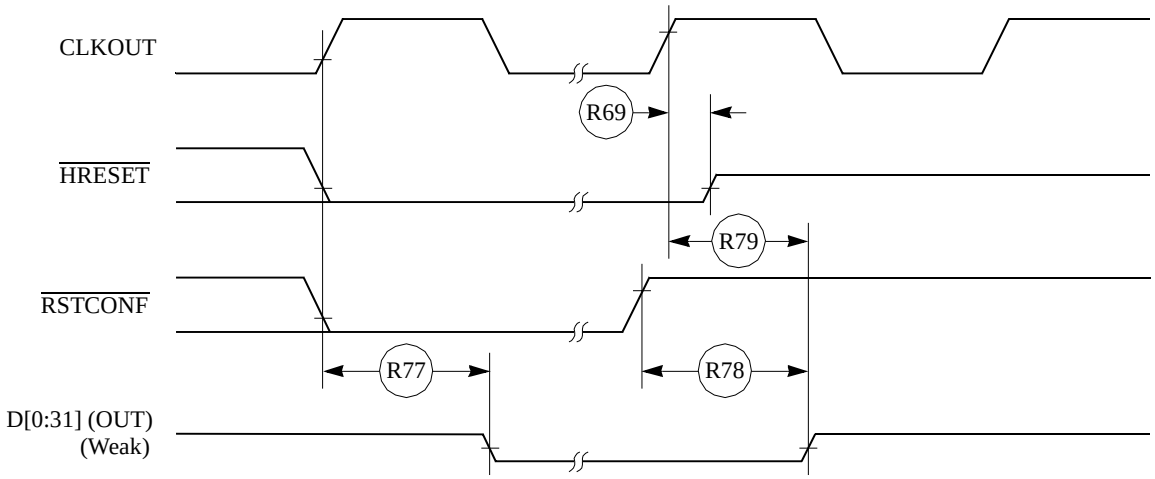


**Figure 32. Reset Timing—Data Bus Weak Drive during Configuration**

Figure 33 provides the reset timing for the debug port configuration.

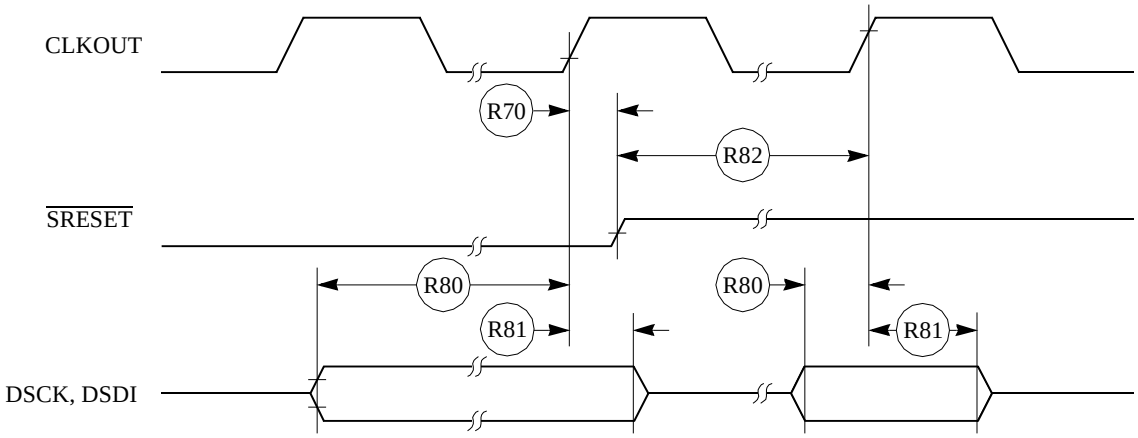


**Figure 33. Reset Timing—Debug Port Configuration**

# 7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

**Table 12. JTAG Timing**

| Num | Characteristic | 50 MHz | | 66MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | 100.00 | — | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | 40.00 | — | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | 0.00 | 10.00 | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | — | 27.00 | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | 100.00 | — | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | 40.00 | — | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | 50.00 | — | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | 50.00 | — | 50.00 | — | ns |

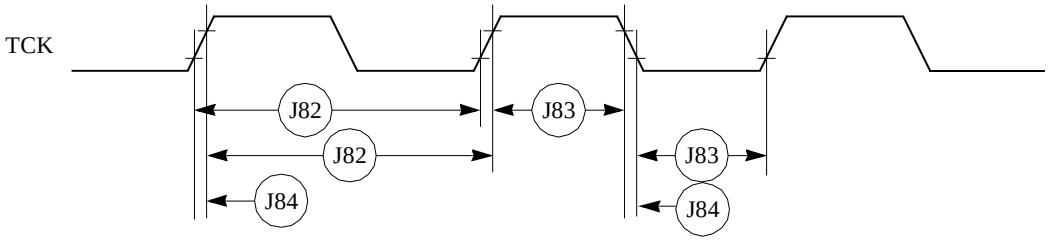


**Figure 34. JTAG Test Clock Input Timing**

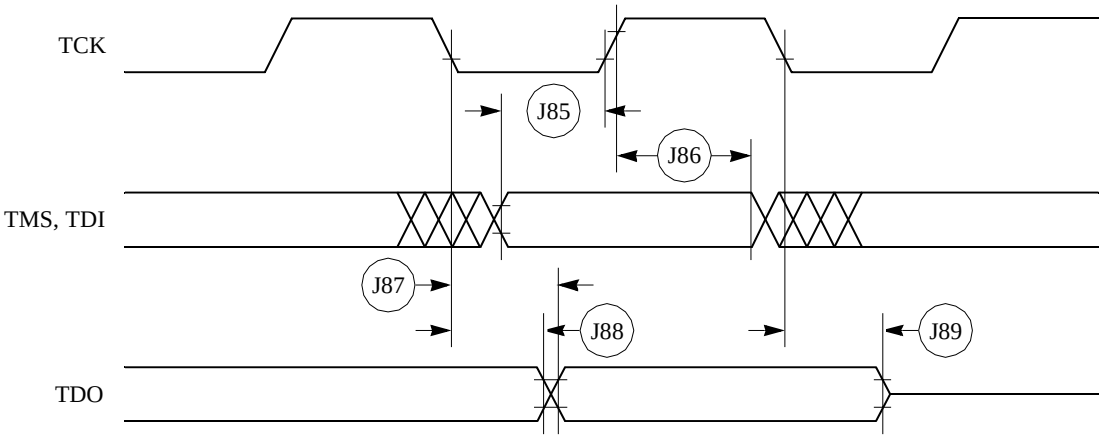


**Figure 35. JTAG Test Access Port Timing Diagram**

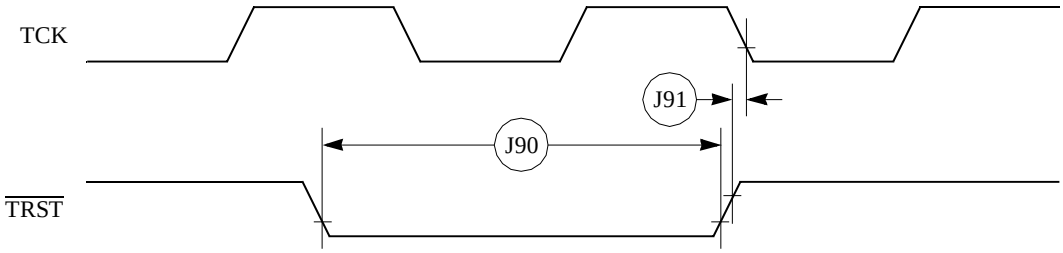


**Figure 36. JTAG $\overline{\text{TRST}}$ Timing Diagram**

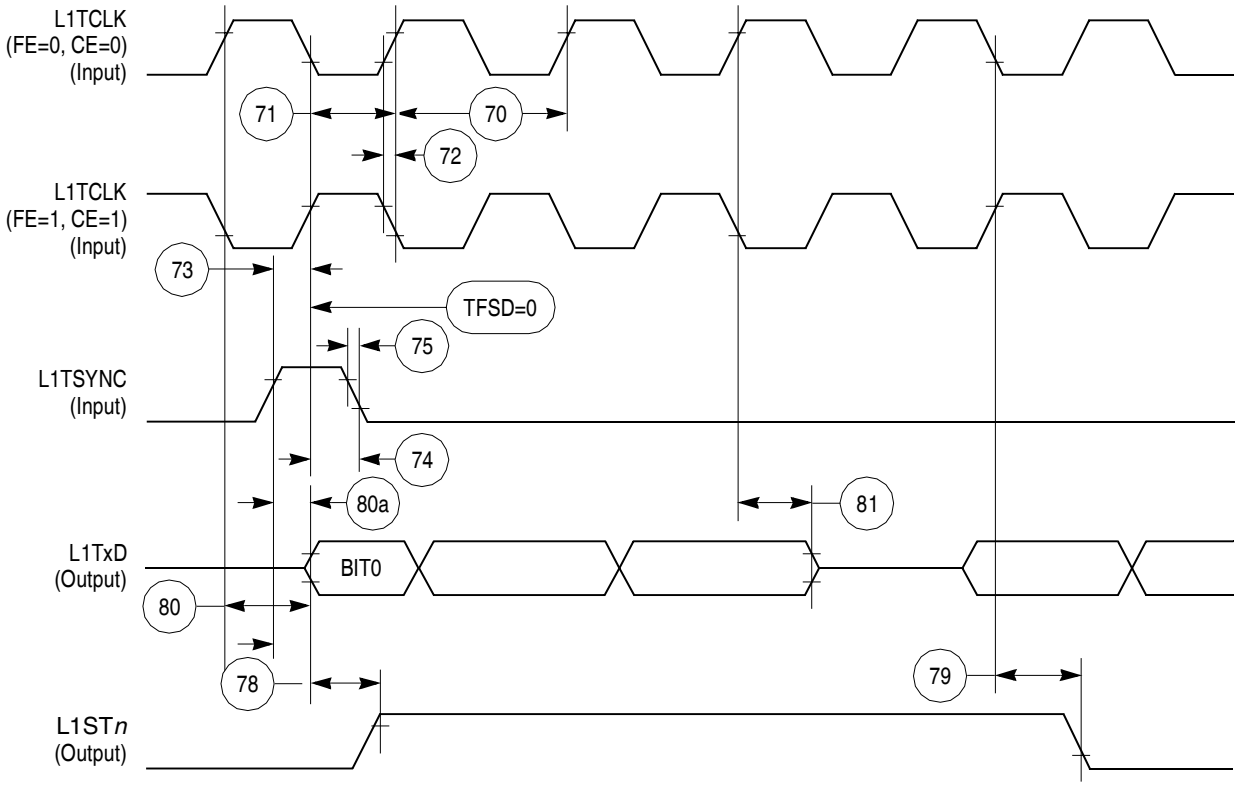


**Figure 47. SI Transmit Timing Diagram**

Figure 50 through Figure 52 show the NMSI timings.

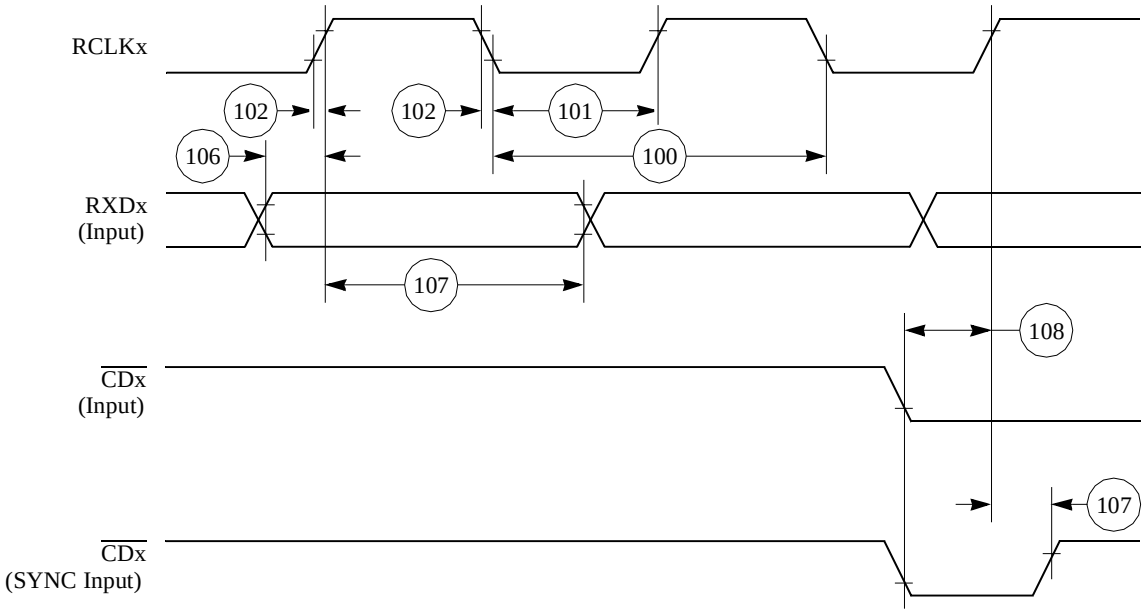


**Figure 50. SCC NMSI Receive Timing Diagram**

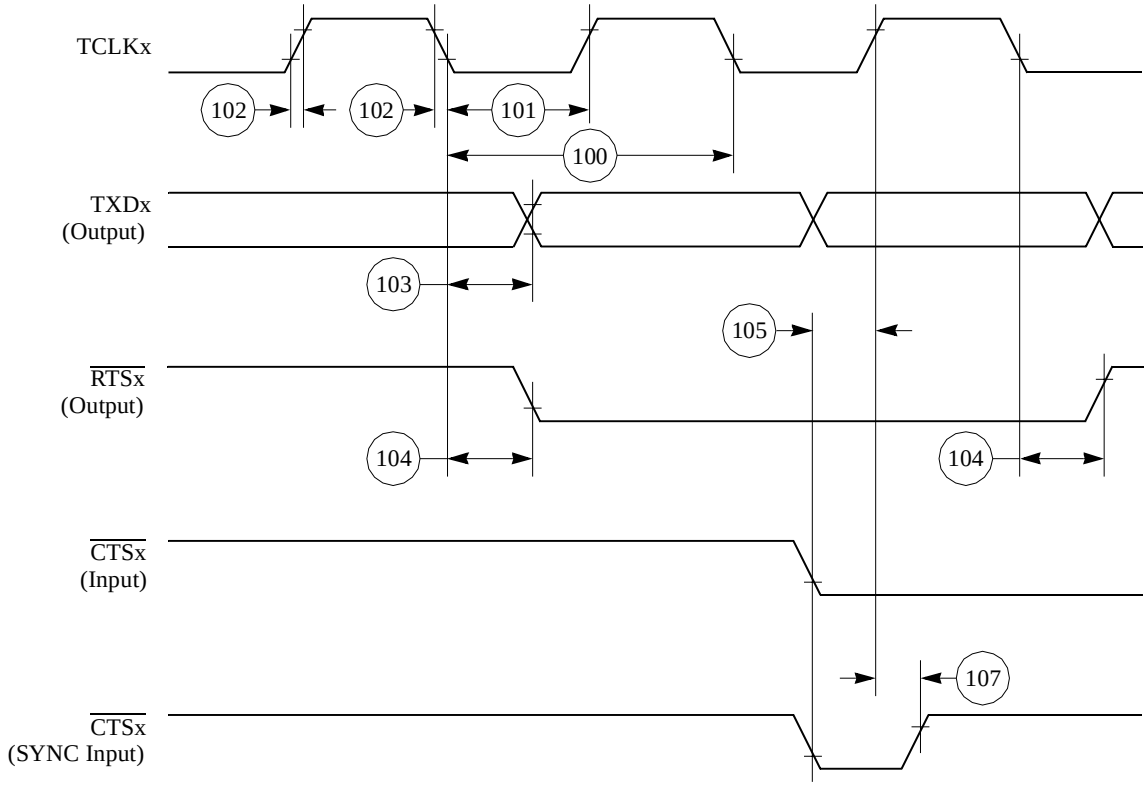


**Figure 51. SCC NMSI Transmit Timing Diagram**

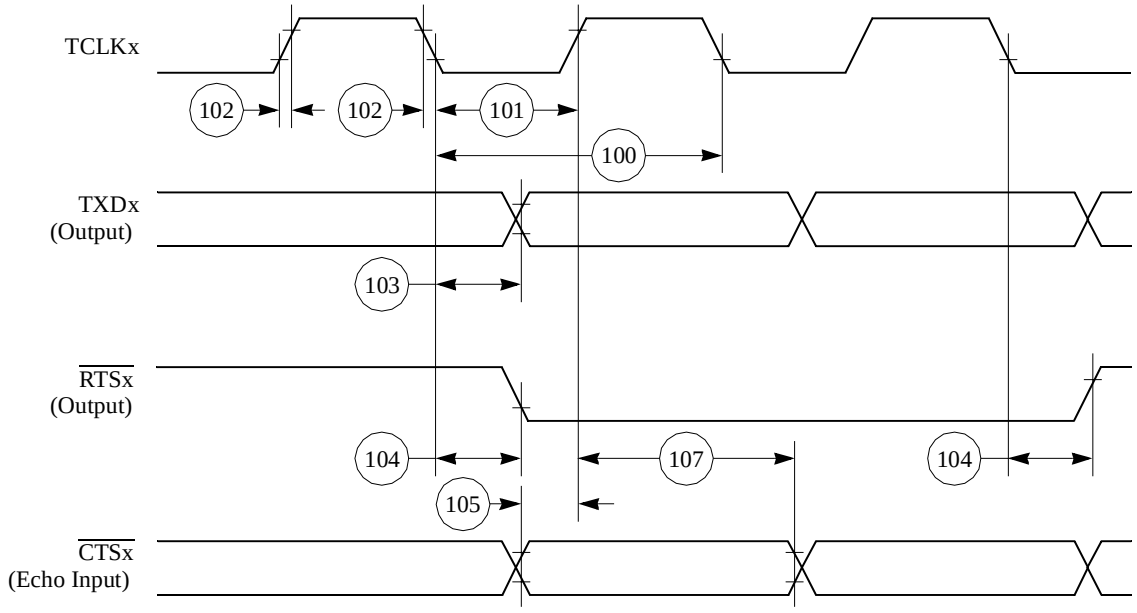


**Figure 52. HDLC Bus Timing Diagram**

## 8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

**Table 20. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40.00 | — | ns |
| 121 | RCLKx rise/fall time (x = 2, 3 for all specs in this table) | — | 15.00 | ns |
| 122 | RCLKx width low | 40.00 | — | ns |
| 123 | RCLKx clock period [1] | 80.00 | 120.00 | ns |
| 124 | RXDx setup time | 20.00 | — | ns |
| 125 | RXDx hold time | 5.00 | — | ns |
| 126 | RENA active delay (from RCLKx rising edge of the last data bit) | 10.00 | — | ns |
| 127 | RENA width low | 100.00 | — | ns |
| 128 | TCLKx rise/fall time | — | 15.00 | ns |
| 129 | TCLKx width low | 40.00 | — | ns |
| 130 | TCLKx clock period[1] | 99.00 | 101.00 | ns |
| 131 | TXDx active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 132 | TXDx inactive delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 133 | TENA active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |

**Table 20. Ethernet Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 134 | TENA inactive delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 138 | CLKOUT low to $\overline{\text{SDACK}}$ asserted [2] | — | 20.00 | ns |
| 139 | CLKOUT low to $\overline{\text{SDACK}}$ negated [2] | — | 20.00 | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame destination address into memory.

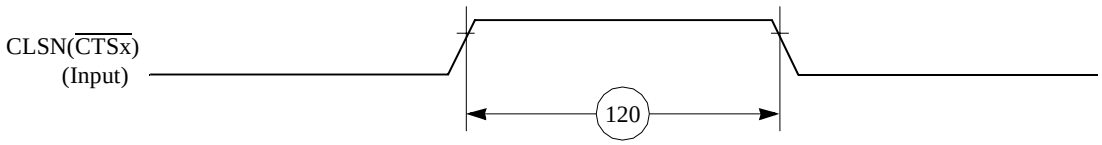


**Figure 53. Ethernet Collision Timing Diagram**

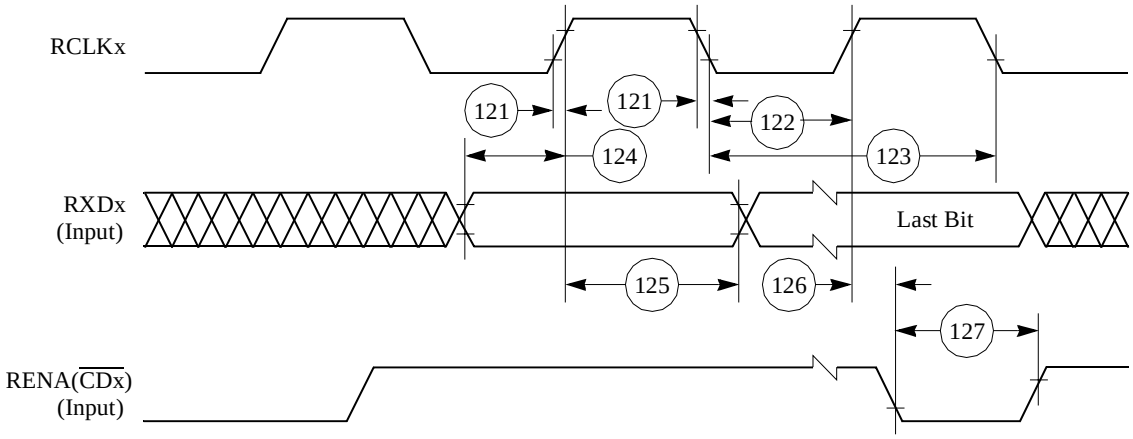


**Figure 54. Ethernet Receive Timing Diagram**

# 10 Document Revision History

Table 28 lists significant changes between revisions of this document.

**Table 28. Document Revision History**

| Revision | Date | Change |
|---|---|---|
| 2 | 7/2005 | Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit. |
| 1 | 10/2002 | Added MPC850DSL. Corrected Figure 25 on page 34. |
| 0.2 | 04/2002 | Updated power numbers and added Rev. C |
| 0.1 | 11/2001 | Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table. |

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK