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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc850srcvr66bu

- 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
 - Caches are two-way, set-associative
 - Physically addressed
 - Cache blocks can be updated with a 4-word line burst
 - Least-recently used (LRU) replacement algorithm
 - Lockable one-line granularity
- Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
- MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
 - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
 - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
 - Hardware bus monitor
 - Spurious interrupt monitor
 - Software watchdog
 - Periodic interrupt timer
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
 - Reset controller
 - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
 - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
 - Memory controller programmable to support most size and speed memory interfaces
 - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
 - Variable block sizes, 32 Kbytes to 256 Mbytes
 - Selectable write protection
 - On-chip bus arbiter supports one external bus master
 - Special features for burst mode support
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers

- Gate mode can enable/disable counting
- Interrupt can be masked on reference match and event capture
- Interrupts
 - Eight external interrupt request (IRQ) lines
 - Twelve port pins with interrupt capability
 - Fifteen internal interrupt sources
 - Programmable priority among SCCs and USB
 - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
 - Master (socket) interface, release 2.1 compliant
 - Single PCMCIA socket
 - Supports eight memory or I/O windows
- Communications processor module (CPM)
 - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
 - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 8 Kbytes of dual-port RAM
 - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
 - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
 - Can be connected to any SCC, SMC, or USB
 - Allow changes during operation
 - Autobaud support option
- Two SCCs (serial communications controllers)
 - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
 - HDLC/SDLC™ (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support PPP (point-to-point protocol)
 - AppleTalk®
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))

θ_{JA} = Package thermal resistance, junction to ambient, °C/W

$$P_D = P_{INT} + P_{I/O}$$

$$P_{INT} = I_{DD} \times V_{DD}, \text{ watts—chip internal power}$$

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \div (T_J + 273^\circ\text{C})(2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273^\circ\text{C}) + \theta_{JA} \bullet P_D^2(3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

5.1 Layout Practices

Each V_{CC} pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at <http://www.mot.com/netcomm>.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B9	CLKOUT to A[6–31] RD/WR, BURST, D[0–31], DP[0–3], TSIZ[0–1], REG, RSV, AT[0–3], PTR high-Z	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B11	CLKOUT to \overline{TS} , \overline{BB} assertion	5.00	11.00	7.58	13.58	6.25	12.25	0.250	50.00	ns
B11a	CLKOUT to \overline{TA} , \overline{BI} assertion, (When driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	—	50.00	ns
B12	CLKOUT to \overline{TS} , \overline{BB} negation	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B12a	CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	—	50.00	ns
B13	CLKOUT to \overline{TS} , \overline{BB} high-Z	5.00	19.00	7.58	21.58	6.25	20.25	0.250	50.00	ns
B13a	CLKOUT to \overline{TA} , \overline{BI} high-Z, (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B14	CLKOUT to \overline{TEA} assertion	2.50	10.00	2.50	10.00	2.50	10.00	—	50.00	ns
B15	CLKOUT to \overline{TEA} high-Z	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B16	\overline{TA} , \overline{BI} valid to CLKOUT (setup time) ⁵	9.75	—	9.75	—	9.75	—	—	50.00	ns
B16a	\overline{TEA} , \overline{KR} , \overline{RETRY} , valid to CLKOUT (setup time) ⁵	10.00	—	10.00	—	10.00	—	—	50.00	ns
B16b	\overline{BB} , \overline{BG} , \overline{BR} valid to CLKOUT (setup time) ⁶	8.50	—	8.50	—	8.50	—	—	50.00	ns
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (Hold time). ⁵	1.00	—	1.00	—	1.00	—	—	50.00	ns
B17a	CLKOUT to \overline{KR} , \overline{RETRY} , except \overline{TEA} valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B18	D[0–31], DP[0–3] valid to CLKOUT rising edge (setup time) ⁷	6.00	—	6.00	—	6.00	—	—	50.00	ns
B19	CLKOUT rising edge to D[0–31], DP[0–3] valid (hold time) ⁷	1.00	—	1.00	—	1.00	—	—	50.00	ns
B20	D[0–31], DP[0–3] valid to CLKOUT falling edge (setup time) ⁸	4.00	—	4.00	—	4.00	—	—	50.00	ns
B21	CLKOUT falling edge to D[0–31], DP[0–3] valid (hold time) ⁸	2.00	—	2.00	—	2.00	—	—	—	—

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B29h	$\overline{WE}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B29i	\overline{CS} negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B30	\overline{CS} , $\overline{WE}[0-3]$ negated to A[6-31] invalid GPCM write access ⁹	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B30a	$\overline{WE}[0-3]$ negated to A[6-31] invalid GPCM write access, TRLX = 0, CSNT = 1, \overline{CS} negated to A[6-31] invalid GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B30b	$\overline{WE}[0-3]$ negated to A[6-31] invalid GPCM write access, TRLX = 1, CSNT = 1, \overline{CS} negated to A[6-31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B30c	$\overline{WE}[0-3]$ negated to A[6-31] invalid GPCM write access, TRLX = 0, CSNT = 1, \overline{CS} negated to A[6-31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	8.00	—	6.00	—	0.375	50.00	ns
B30d	$\overline{WE}[0-3]$ negated to A[6-31] invalid GPCM write access TRLX = 1, CSNT = 1, \overline{CS} negated to A[6-31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

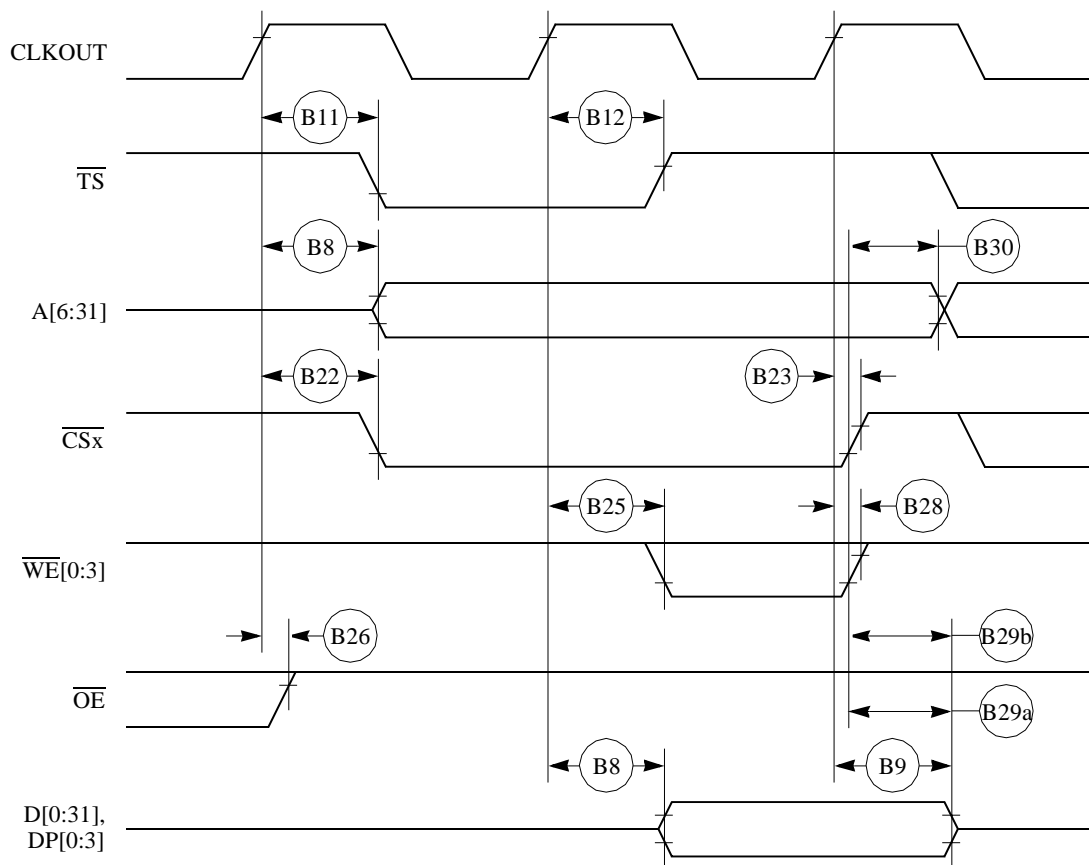


Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

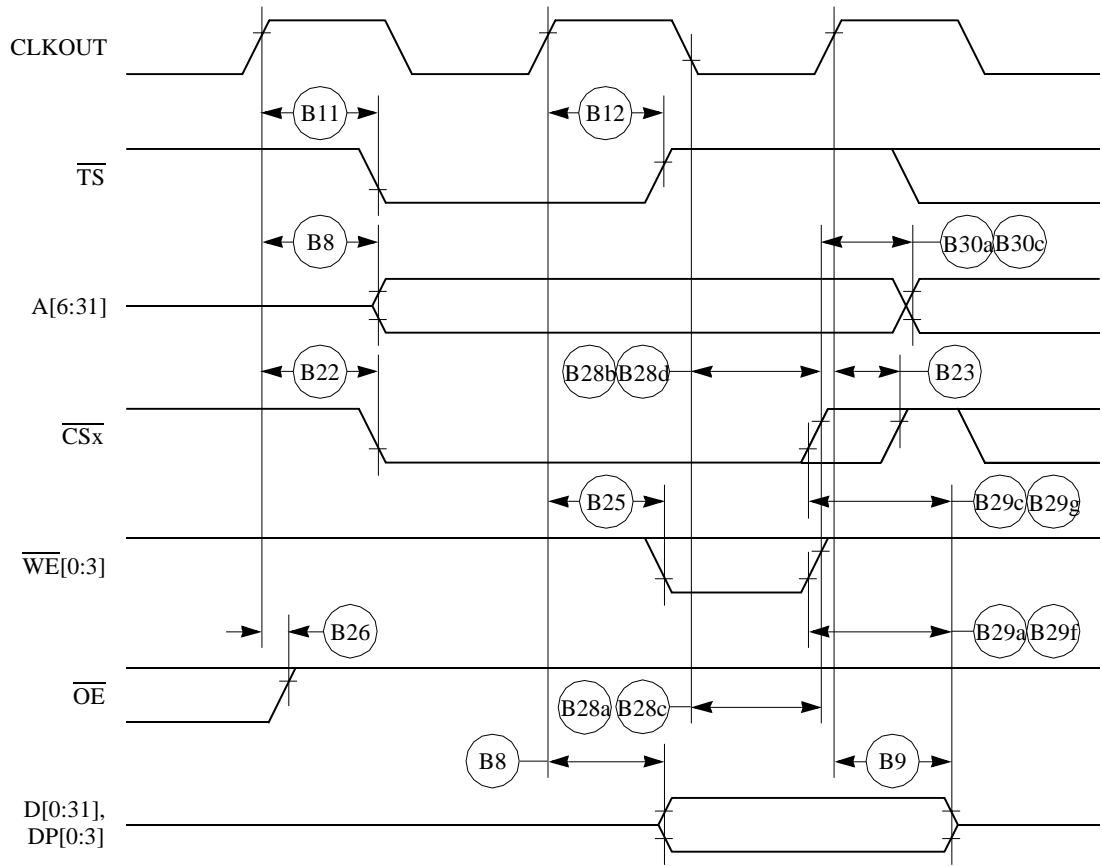


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Figure 17 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

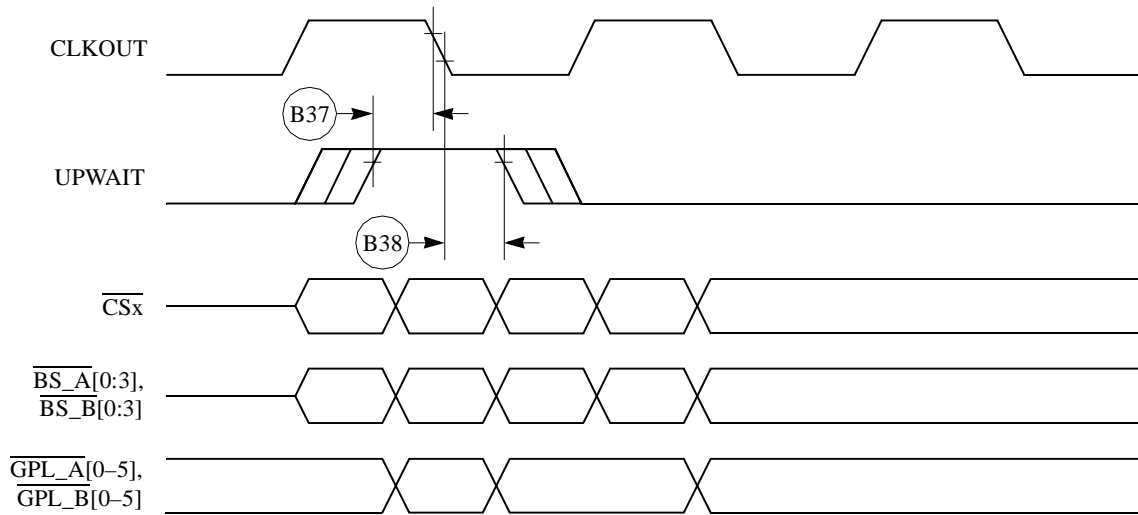


Figure 17. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 18 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

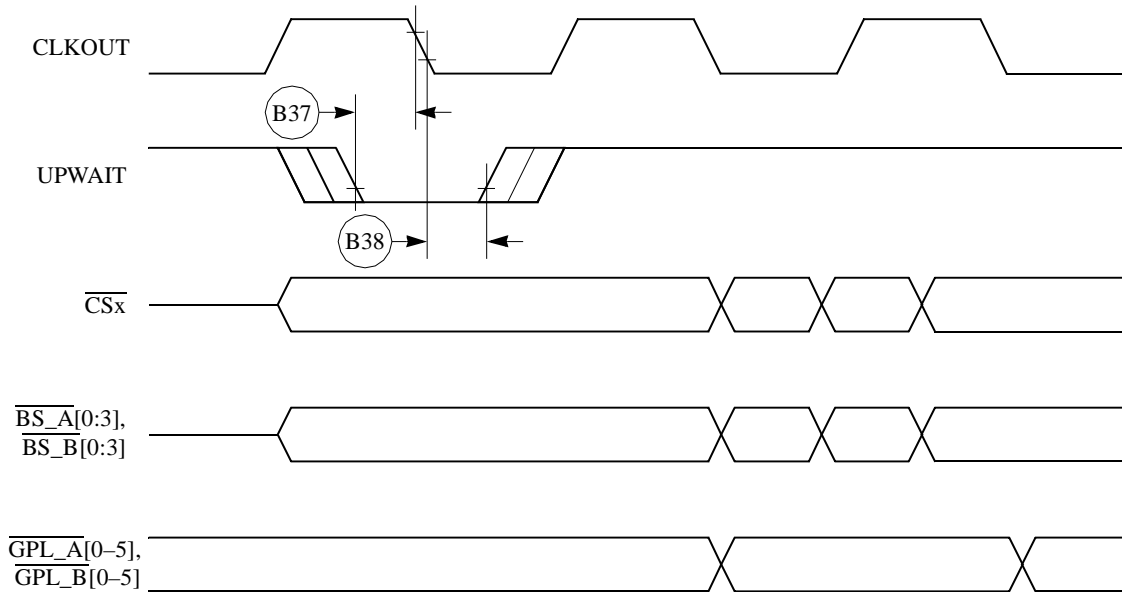


Figure 18. Asynchronous $\overline{\text{UPWAIT}}$ Negated Detection in UPM Handled Cycles Timing

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

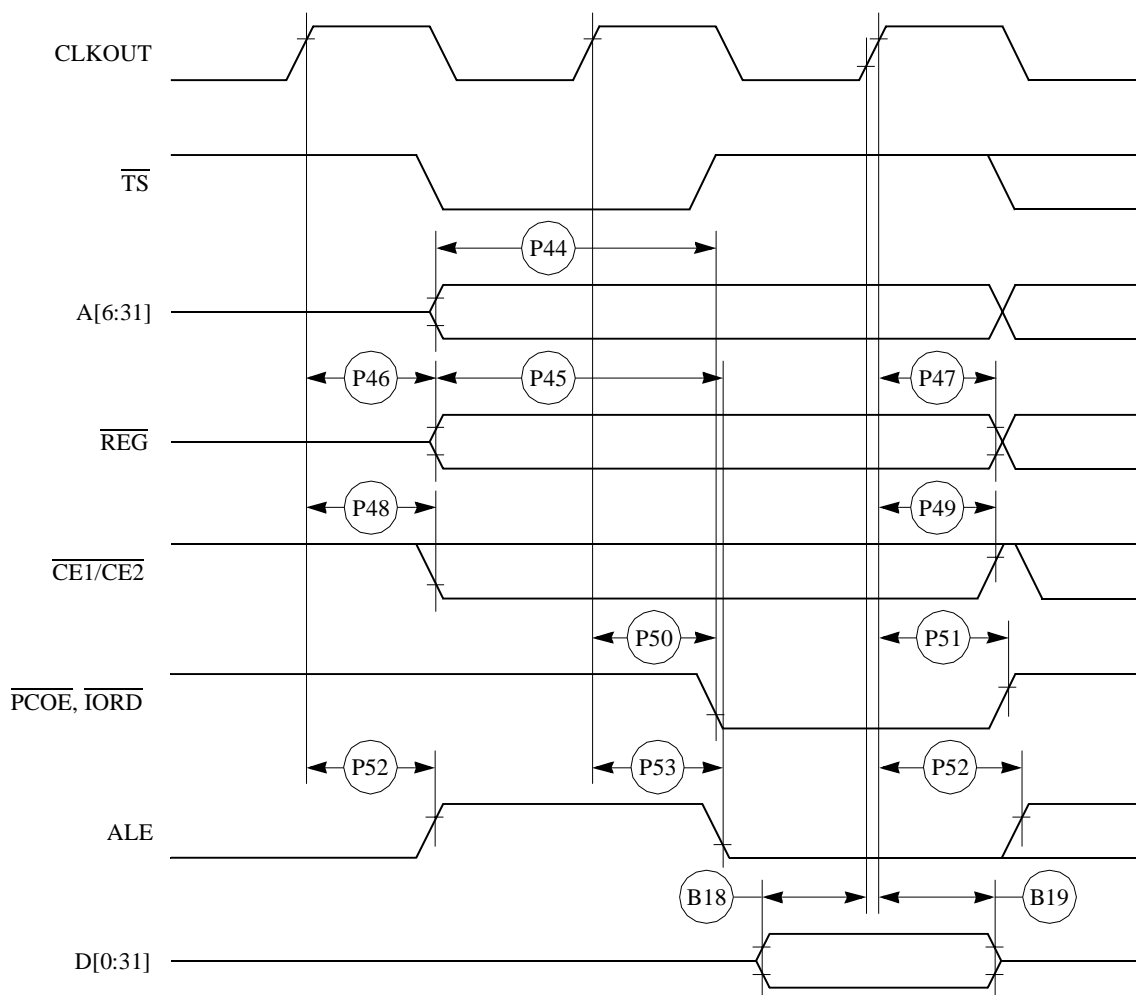


Figure 24. PCMCIA Access Cycles Timing External Bus Read

Table 9 shows the PCMCIA port timing for the MPC850.

Table 9. PCMCIA Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive ¹	18.00	—	26.00	—	22.00	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

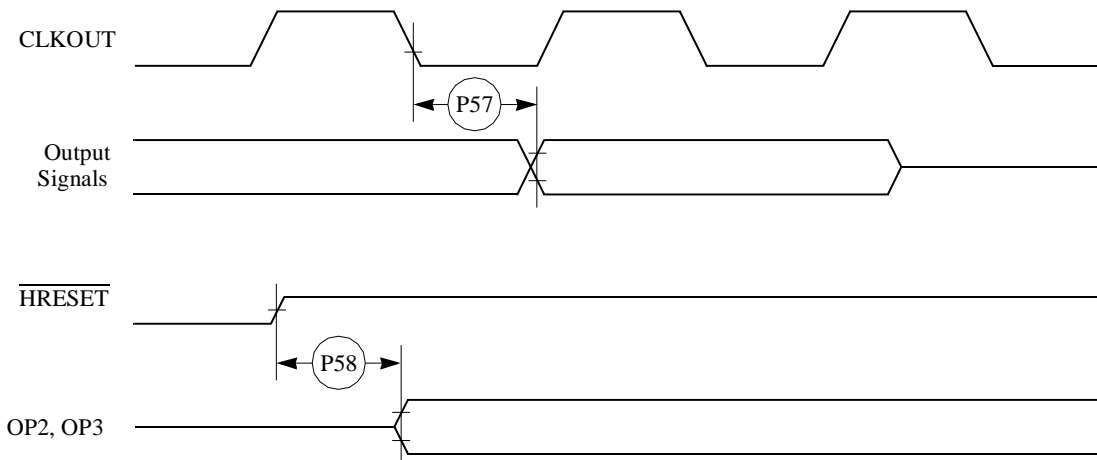


Figure 27. PCMCIA Output Port Timing

Figure 28 provides the PCMCIA output port timing for the MPC850.

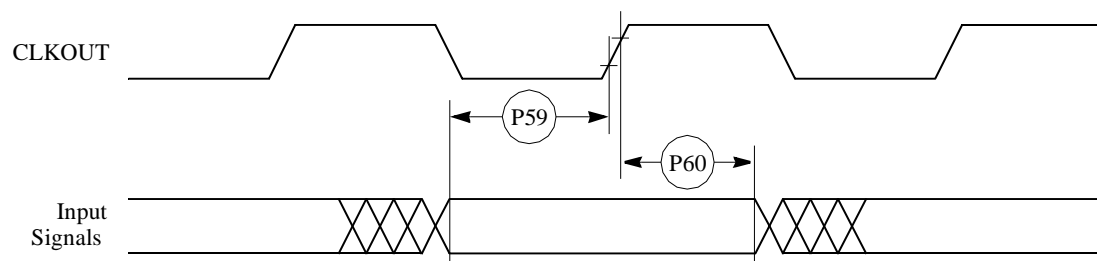


Figure 28. PCMCIA Input Port Timing

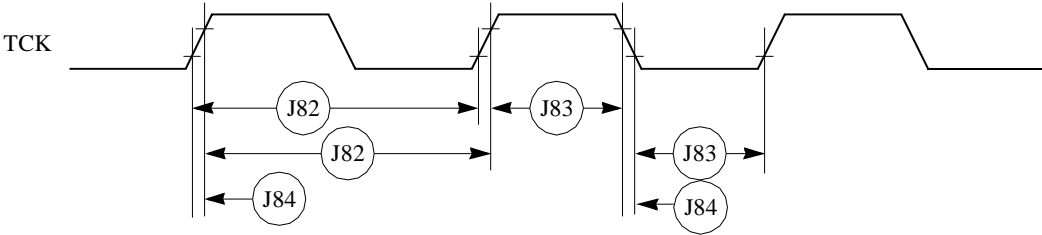


Figure 34. JTAG Test Clock Input Timing

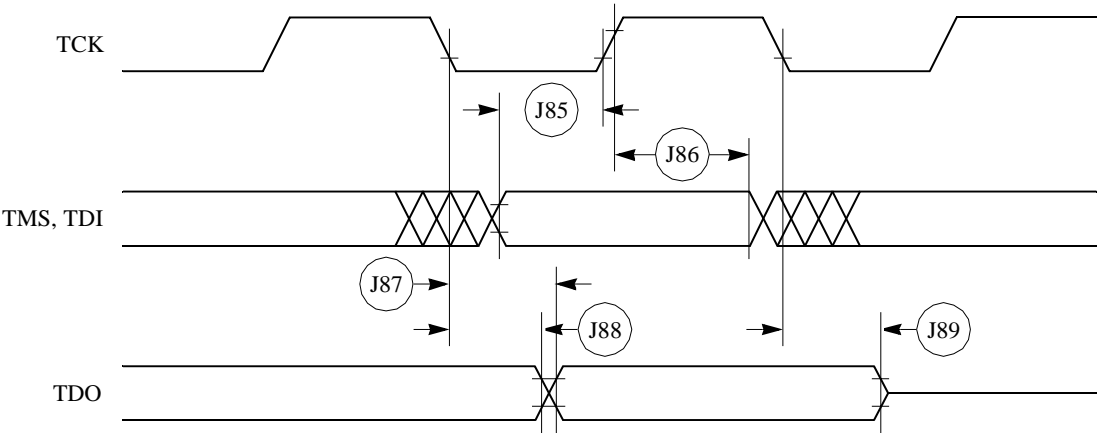


Figure 35. JTAG Test Access Port Timing Diagram

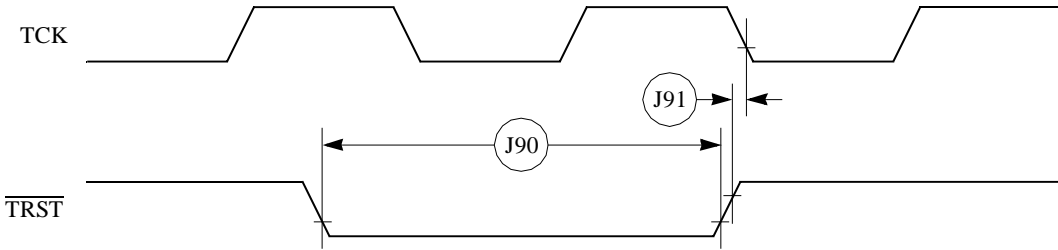


Figure 36. JTAG $\overline{\text{TRST}}$ Timing Diagram

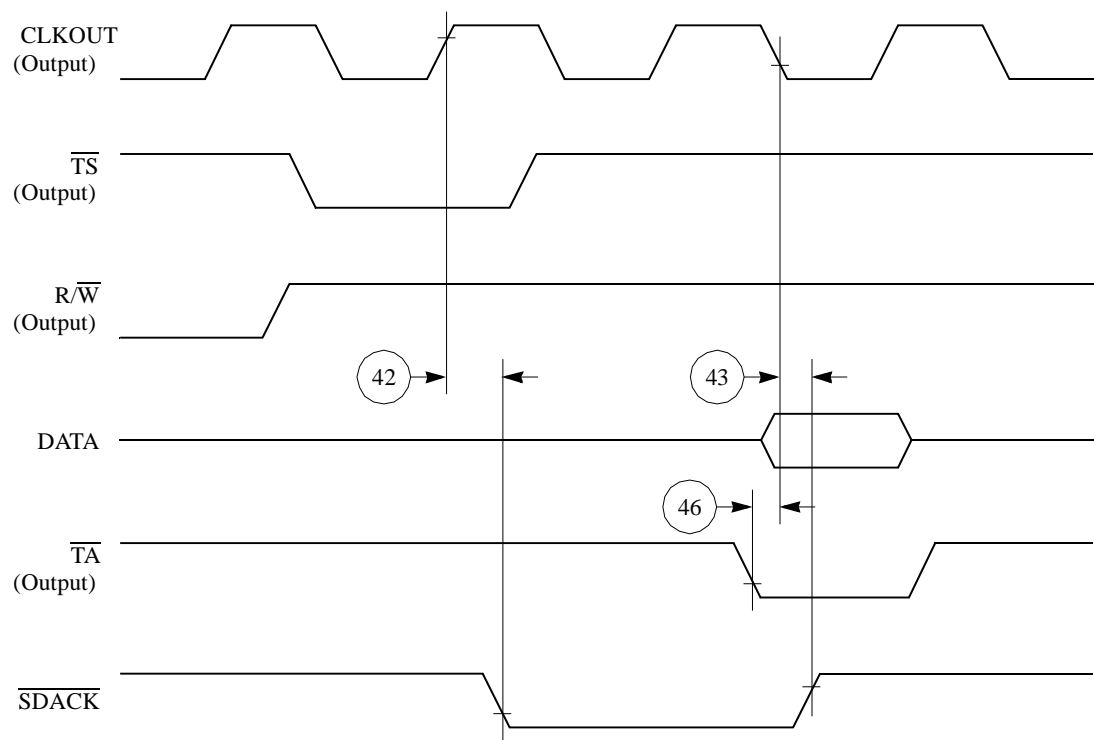


Figure 40. \overline{SDACK} Timing Diagram—Peripheral Write, \overline{TA} Sampled Low at the Falling Edge of the Clock

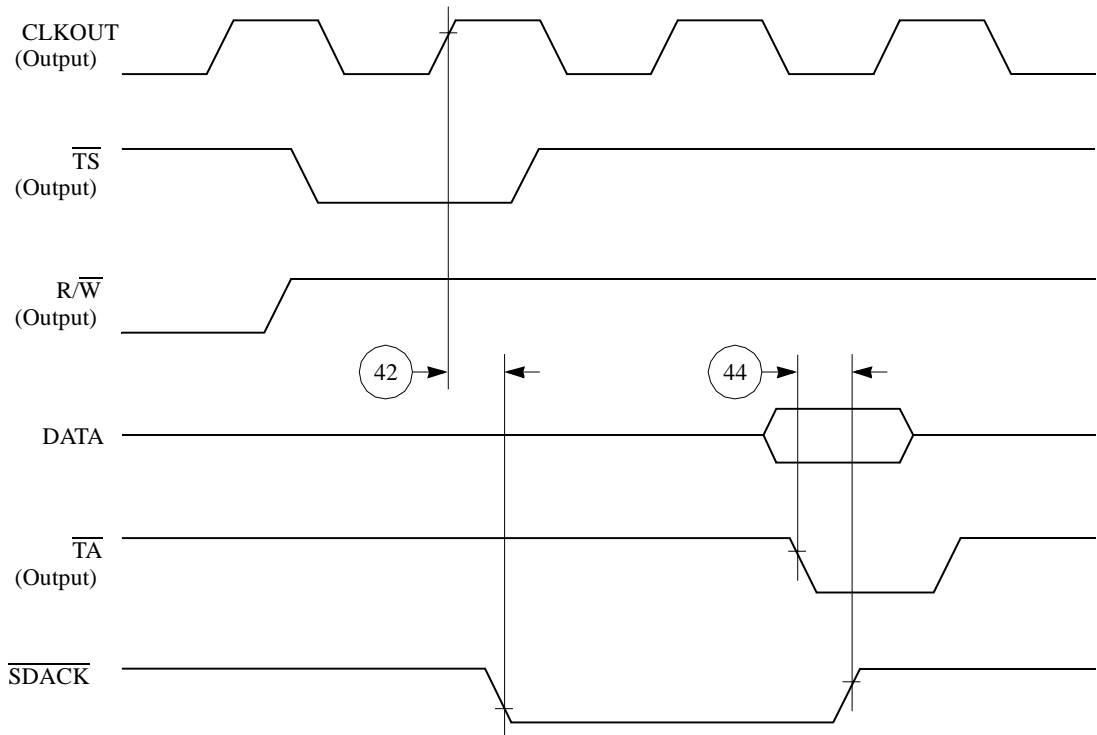


Figure 41. \overline{SDACK} Timing Diagram—Peripheral Write, \overline{TA} Sampled High at the Falling Edge of the Clock

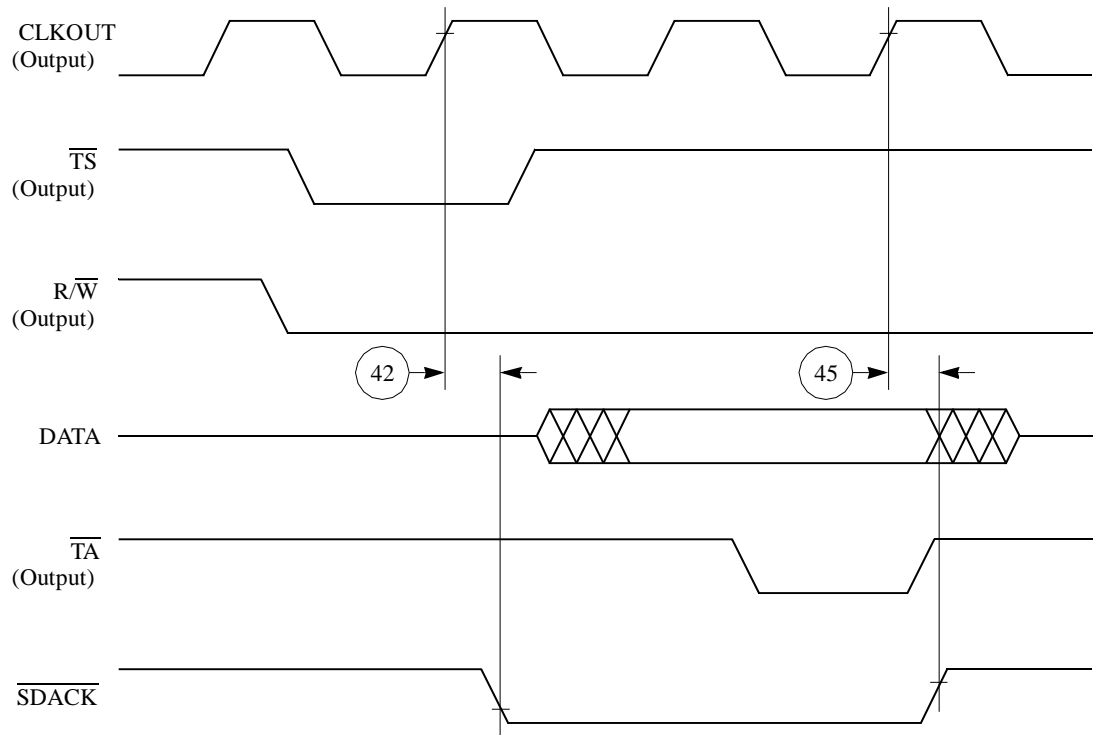


Figure 42. \overline{SDACK} Timing Diagram—Peripheral Read

8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns

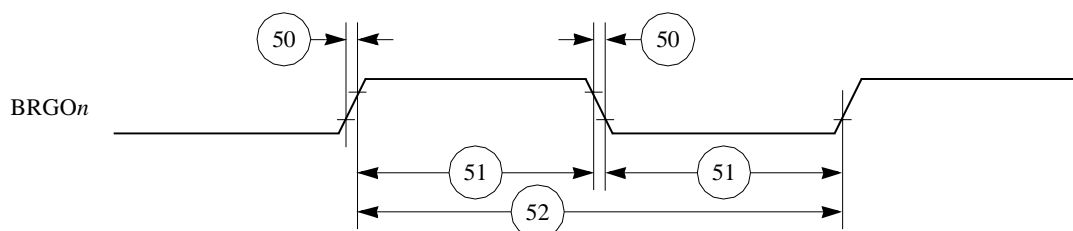


Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Table 16. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/TGATE rise and fall time	10.00	—	ns
62	TIN/TGATE low time	1.00	—	clk
63	TIN/TGATE high time	2.00	—	clk
64	TIN/TGATE cycle time	3.00	—	clk
65	CLKO high to TOUT valid	3.00	25.00	ns

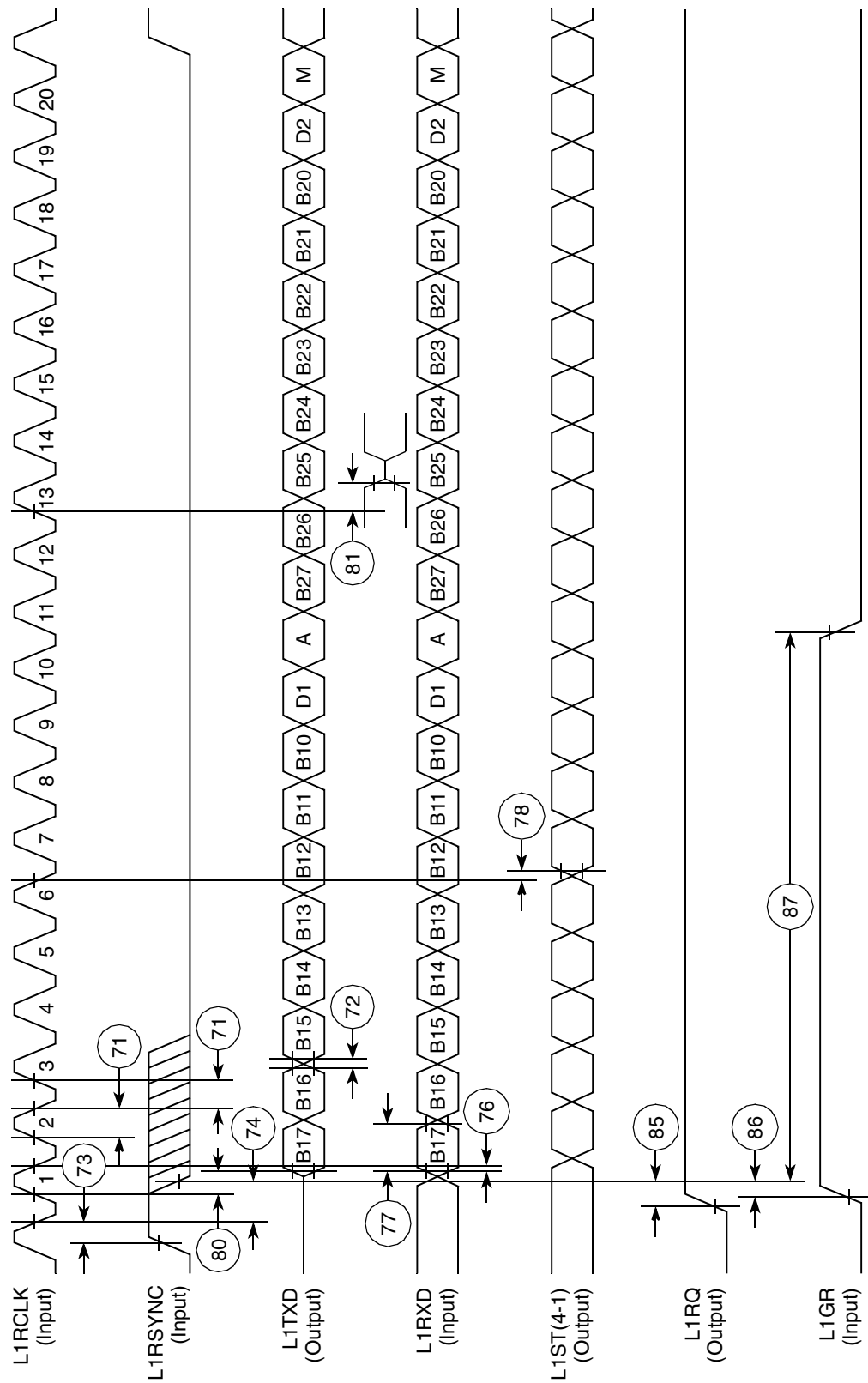


Figure 49. IDL Timing

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

Table 18. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency ¹ (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	—	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge ²	5.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	5.00	—	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency ¹ (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time	—	—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	40.00	—	ns
106	RXDx setup time to RCLKx rising edge	40.00	—	ns
107	RXDx hold time from RCLKx rising edge ²	0.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	40.00	—	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

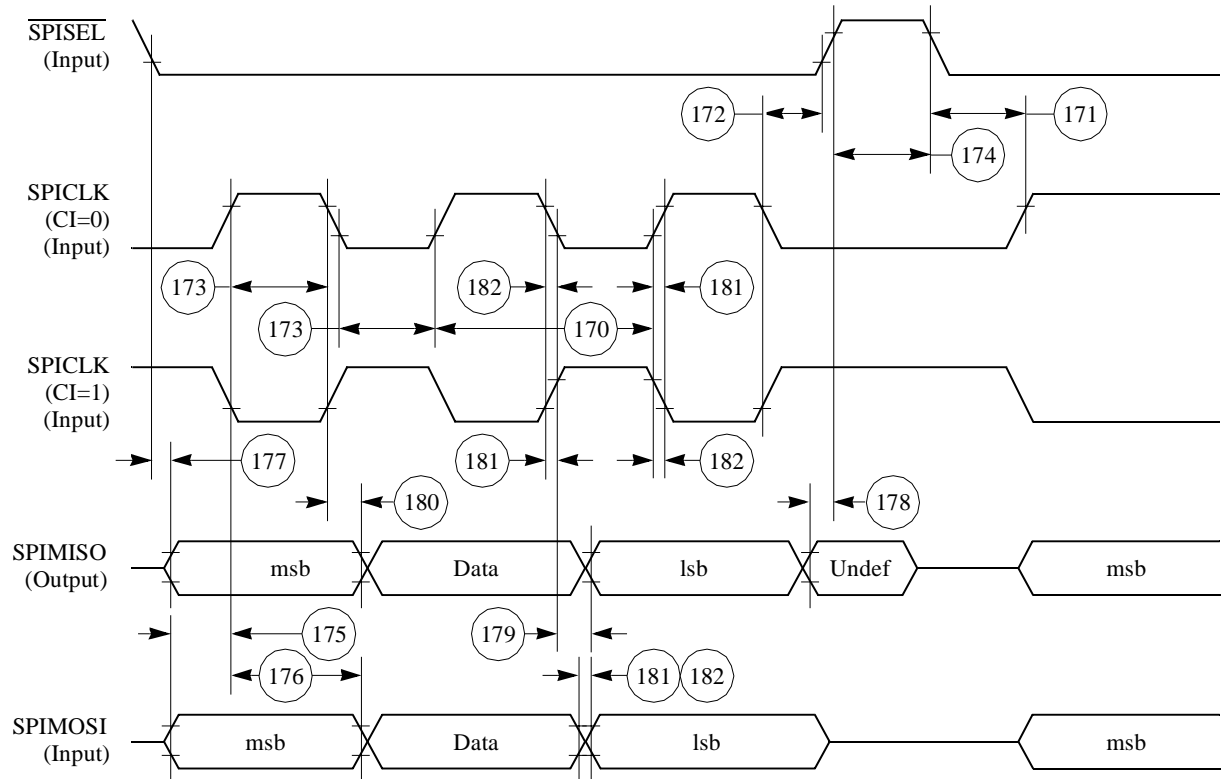


Figure 59. SPI Slave (CP = 0) Timing Diagram

9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivatives

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

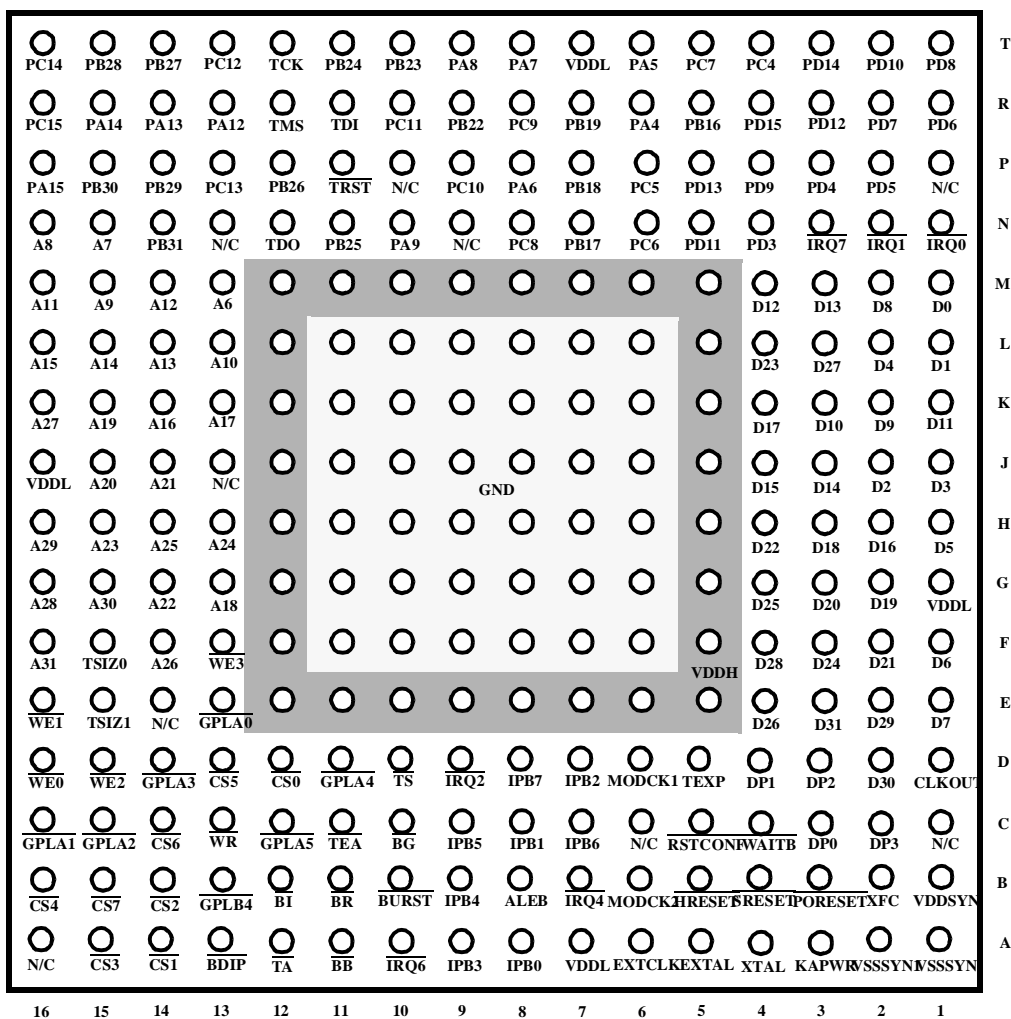


Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard



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