Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850cvr66bu

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I^{2}C port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

Table 1. MPC850 Functionality Matrix

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Additional documentation may be provided for parts listed in Table 1.

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA [1]	θ_{JA}	40 [2]	°C/W
	θ_{JA}	31 [3]	°C/W
	θ_{JA}	24 [4]	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

[1] For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

[2] Assumes natural convection and a single layer board (no thermal vias).

[3] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

[4] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$\quad P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

$\qquad$ where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

[1] Typical power dissipation is measured at 3.3V

[2] Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input low voltage	VIL	GND	0.8	V
EXTAL, EXTCLK input high voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input leakage current, Vin = 5.5 V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{in}	—	100	µA
Input leakage current, Vin = 3.6V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{In}	—	10	µA
Input leakage current, Vin = 0V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I_{In}	—	10	µA
Input capacitance	C_{in}	—	20	pF
Output high voltage, IOH = -2.0 mA, VDDH = 3.0V except XTAL, XFC, and open-drain pins	VOH	2.4	—	V
Output low voltage CLKOUT [3] IOL = 3.2 mA [1] IOL = 5.3 mA [2] IOL = 7.0 mA PA[14]/$\overline{\text{USBOE}}$, PA[12]/TXD2 IOL = 8.9 mA $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$	VOL	—	0.5	V

[1] A[6:31], TSIZ0/$\overline{\text{REG}}$, TSIZ1, D[0:31], DP[0:3]/$\overline{\text{IRQ[3:6]}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, RSV/$\overline{\text{IRQ2}}$, IP_B[0:1]/IWP[0:1]/$\overline{\text{VFLS[0:1]}}$, IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/$\overline{\text{PTR}}$/AT3, PA[15]/USBRXD, PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/$\overline{\text{TOUT1}}$/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/$\overline{\text{TOUT2}}$/TIN4, PB[31]/$\overline{\text{SPISEL}}$, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/$\overline{\text{BRGO1}}$, PB[26]/I2CSCL/$\overline{\text{BRGO2}}$, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/$\overline{\text{SDACK1}}$, PB[22]/SMSYN2/$\overline{\text{SDACK2}}$, PB[19]/L1ST1, PB[18]/$\overline{\text{RTS2}}$/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/$\overline{\text{DREQ0}}$/L1ST5, PC[14]/$\overline{\text{DREQ1}}$/$\overline{\text{RTS2}}$/L1ST6, PC[13]/L1ST7/$\overline{\text{RTS3}}$, PC[12]/L1RQa/L1ST8, PC[11]/USBRXP, PC[10]/$\overline{\text{TGATE1}}$/$\overline{\text{USBRXN}}$, PC[9]/$\overline{\text{CTS2}}$, PC[8]/$\overline{\text{CD2}}$/TGATE1, PC[7]/USBTXP, PC[6]/USBTXN, PC[5]/$\overline{\text{CTS3}}$/L1TSYNCA/$\overline{\text{SDACK1}}$, PC[4]/$\overline{\text{CD3}}$/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

[2] $\overline{\text{BDIP}}$/GPL_B5, $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{FRZ}}$/IRQ6, $\overline{\text{CS[0:5]}}$, $\overline{\text{CS6}}$/$\overline{\text{CE1\_B}}$, $\overline{\text{CS7}}$/$\overline{\text{CE2\_B}}$, $\overline{\text{WE0}}$/$\overline{\text{BS\_AB0}}$/$\overline{\text{IORD}}$, $\overline{\text{WE1}}$/$\overline{\text{BS\_AB1}}$/$\overline{\text{IOWR}}$, $\overline{\text{WE2}}$/$\overline{\text{BS\_AB2}}$/$\overline{\text{PCOE}}$, $\overline{\text{WE3}}$/$\overline{\text{BS\_AB3}}$/$\overline{\text{PCWE}}$, $\overline{\text{GPL\_A0}}$/$\overline{\text{GPL\_B0}}$, $\overline{\text{OE}}$/$\overline{\text{GPL\_A1}}$/$\overline{\text{GPL\_B1}}$, $\overline{\text{GPL\_A[2:3]}}$/$\overline{\text{GPL\_B[2:3]}}$/$\overline{\text{CS[2:3]}}$, UPWAITA/GPL_A4/$\overline{\text{AS}}$, UPWAITB/GPL_B4, GPL_A5, ALE_B/DSCK/AT1, OP2/MODCK1/$\overline{\text{STS}}$, OP3/MODCK2/DSDO

3 The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, IOH and IOL for Clkout should be extracted from the IBIS model at any output voltage level.

5 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (P_D \bullet \theta_{JA})(1)$$

where

T_A = Ambient temperature, °C

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz Min	50 MHz Max	66 MHz Min	66 MHz Max	80 MHz Min	80 MHz Max	FFACT	Cap Load (default 50 pF)	Unit
B9	CLKOUT to A[6–31] RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3], TSIZ[0–1], REG, RSV, AT[0–3], PTR high-Z	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion	5.00	11.00	7.58	13.58	6.25	12.25	0.250	50.00	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion, (When driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	—	50.00	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	—	50.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ high-Z	5.00	19.00	7.58	21.58	6.25	20.25	0.250	50.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ high-Z, (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion	2.50	10.00	2.50	10.00	2.50	10.00	—	50.00	ns
B15	CLKOUT to $\overline{TEA}$ high-Z	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT(setup time) [5]	9.75	—	9.75	—	9.75	—	—	50.00	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, valid to CLKOUT (setup time) [5]	10.00	—	10.00	—	10.00	—	—	50.00	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid to CLKOUT (setup time) [6]	8.50	—	8.50	—	8.50	—	—	50.00	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (Hold time).[5]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, except $\overline{TEA}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B18	D[0–31], DP[0–3] valid to CLKOUT rising edge (setup time) [7]	6.00	—	6.00	—	6.00	—	—	50.00	ns
B19	CLKOUT rising edge to D[0–31], DP[0–3] valid (hold time) [7]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B20	D[0–31], DP[0–3] valid to CLKOUT falling edge (setup time) [8]	4.00	—	4.00	—	4.00	—	—	50.00	ns
B21	CLKOUT falling edge to D[0–31], DP[0–3] valid (hold time) [8]	2.00	—	2.00	—	2.00	—	—	—	—

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Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B33	CLKOUT falling edge to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns

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Table 6. Bus Operation Timing [1] **(continued)**

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B42	CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B43	$\overline{\text{AS}}$ negation to memory controller signals negation	—	TBD	—	TBD	TBD	—	—	50.00	ns

[1] The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{\text{FFACTOR x 1000}}{F} + (D_{50} - 20 \text{ x FFACTOR})$$

For maxima:

$$D = \frac{\text{FFACTOR x 1000}}{F} + (D_{50} - 20 \text{ x FFACTOR}) + 1\text{ns}(\text{CAP LOAD} - 50) / 10$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

D_{50} is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

[2] Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.

[3] If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

[4] The timing for $\overline{\text{BR}}$ output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for $\overline{\text{BG}}$ output is relevant when the MPC850 is selected to work with internal bus arbiter.

[5] The setup times required for $\overline{\text{TA}}$, $\overline{\text{TEA}}$, and $\overline{\text{BI}}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).

[6] The timing required for $\overline{\text{BR}}$ input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC850 is selected to work with the external bus arbiter.

[7] The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.

[8] The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

[9] The timing B30 refers to $\overline{\text{CS}}$ when ACS = '00' and to $\overline{\text{WE[0:3]}}$ when CSNT = '0'.

[10] The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.

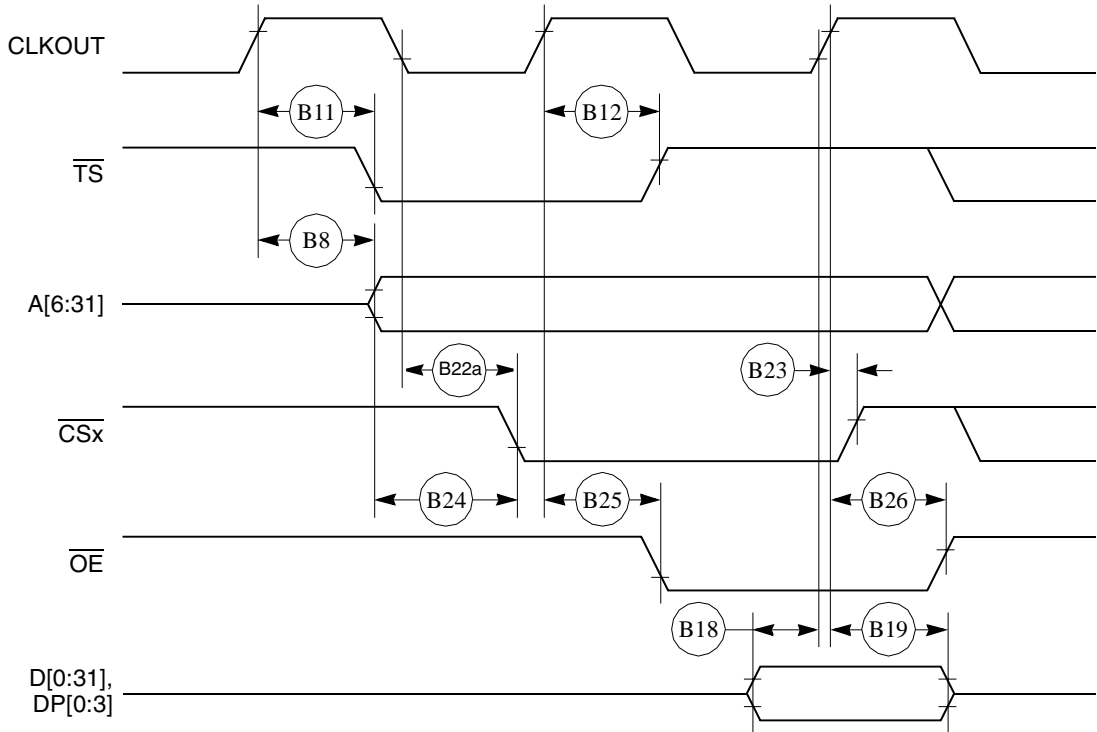[11] The $\overline{\text{AS}}$ signal is considered asynchronous to CLKOUT.

Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)
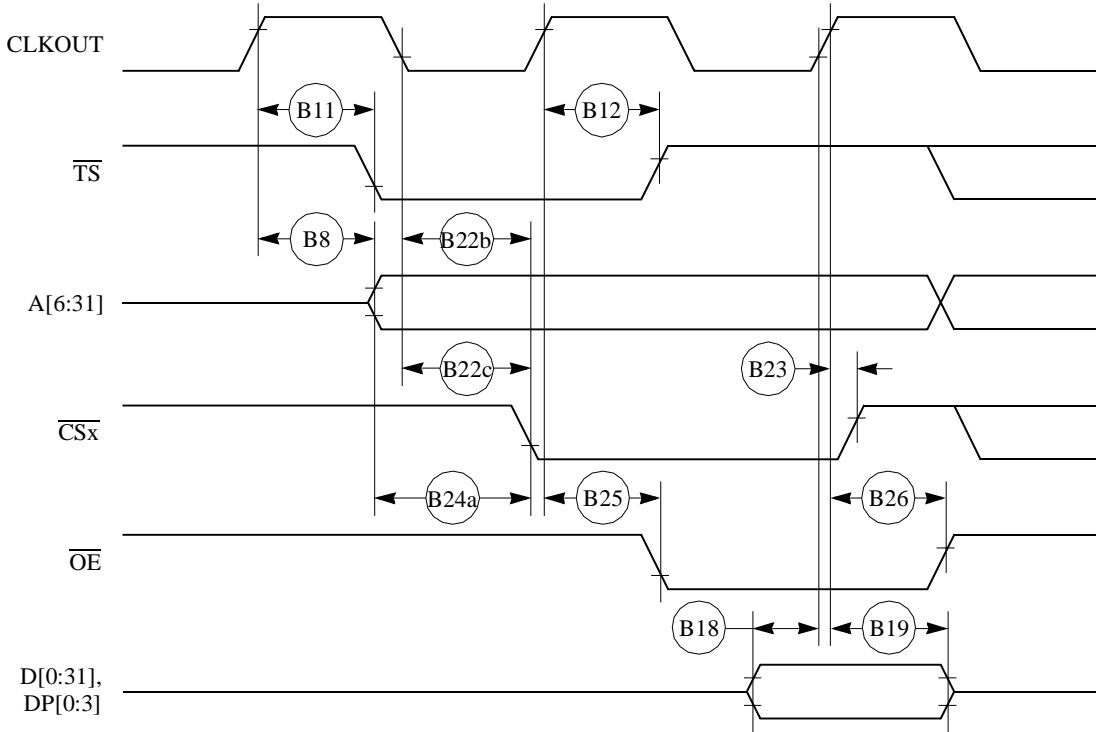

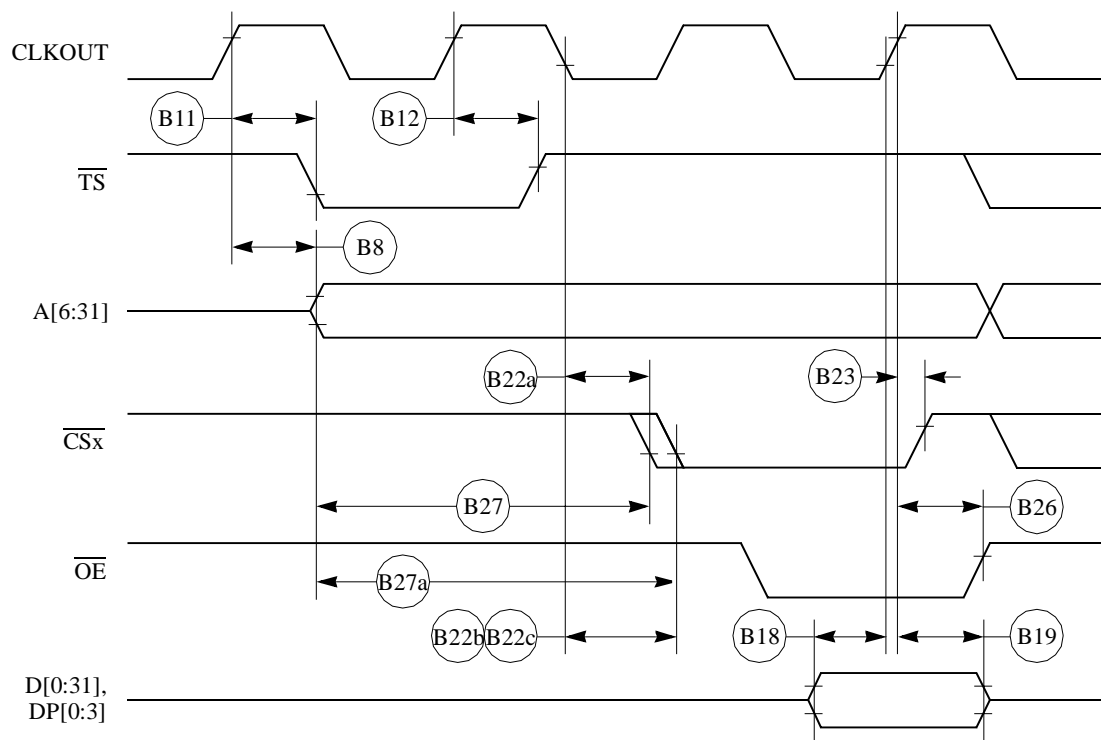**Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)**

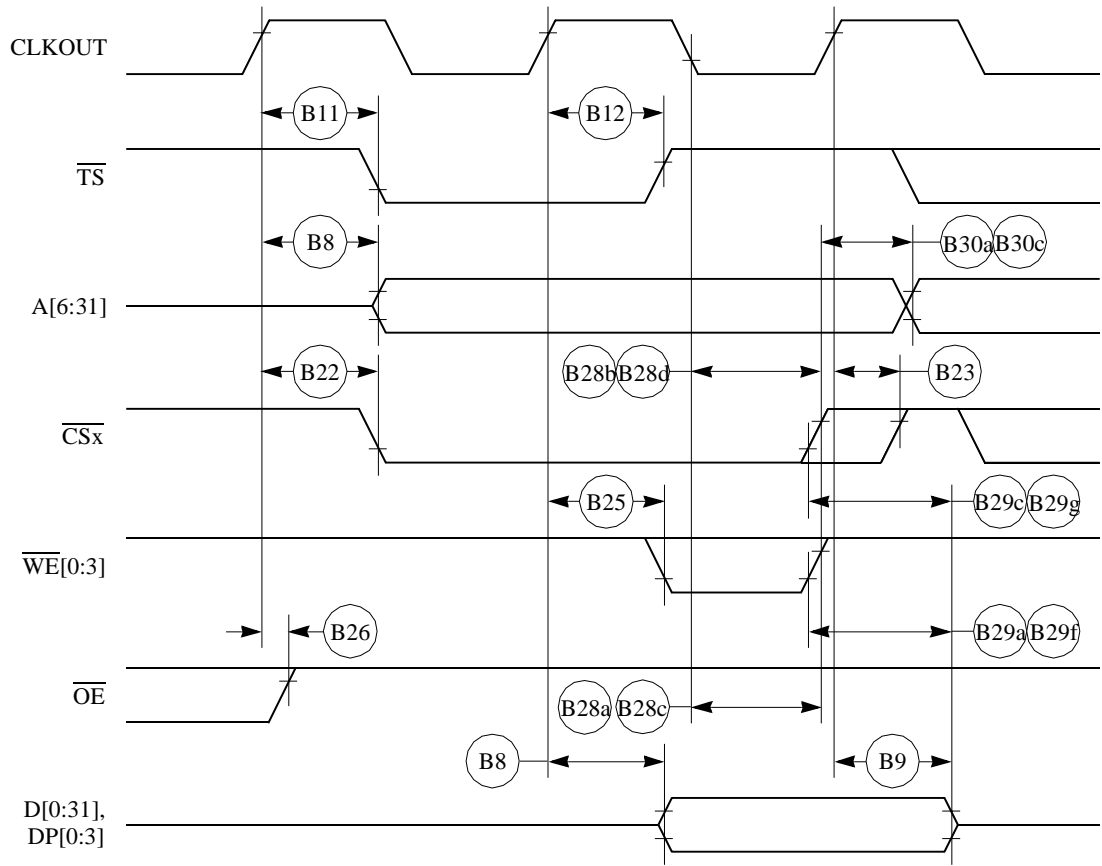**Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)**

Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)
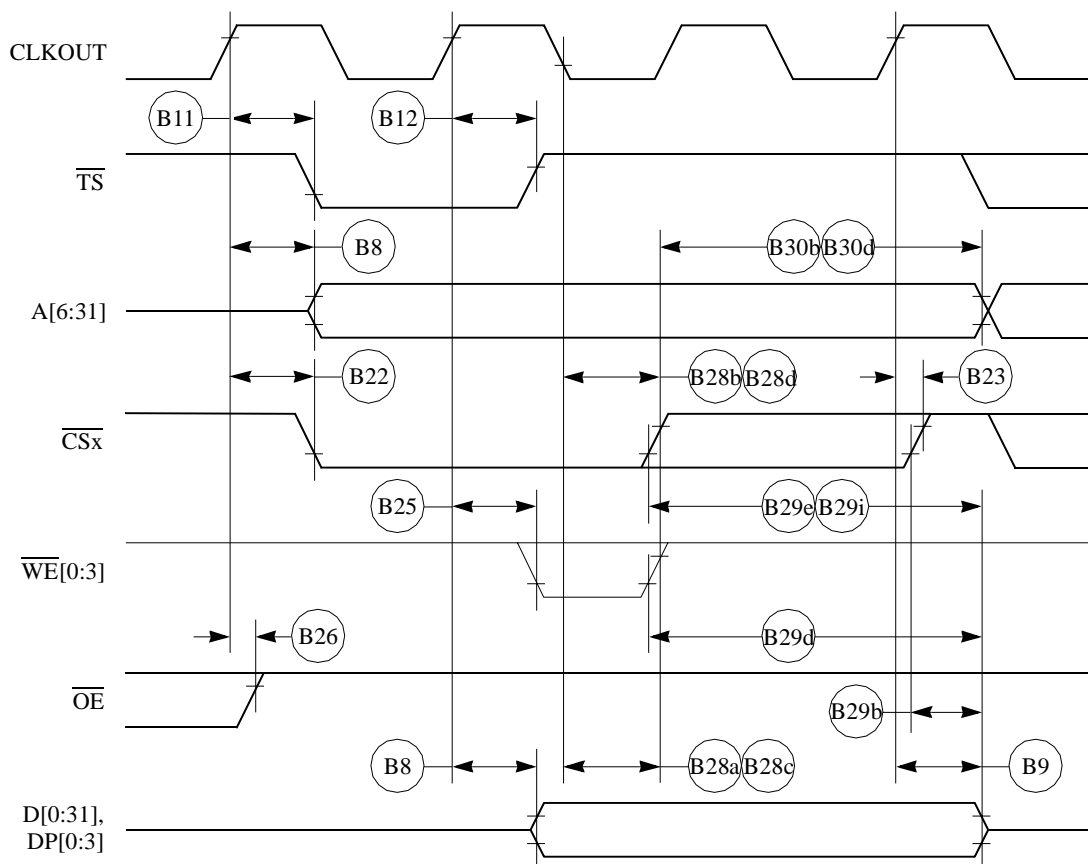
Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 17 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.
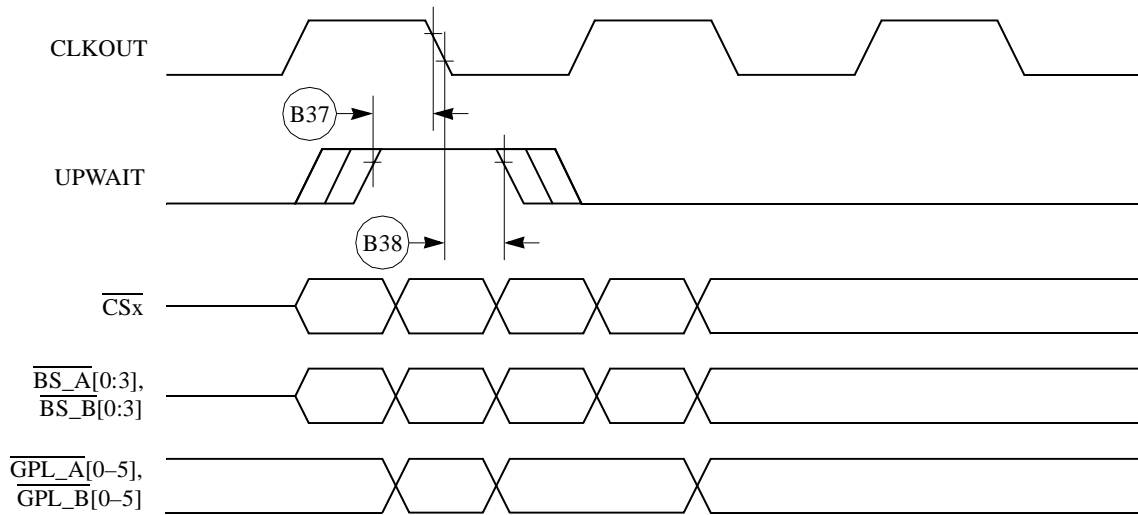

Figure 17. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

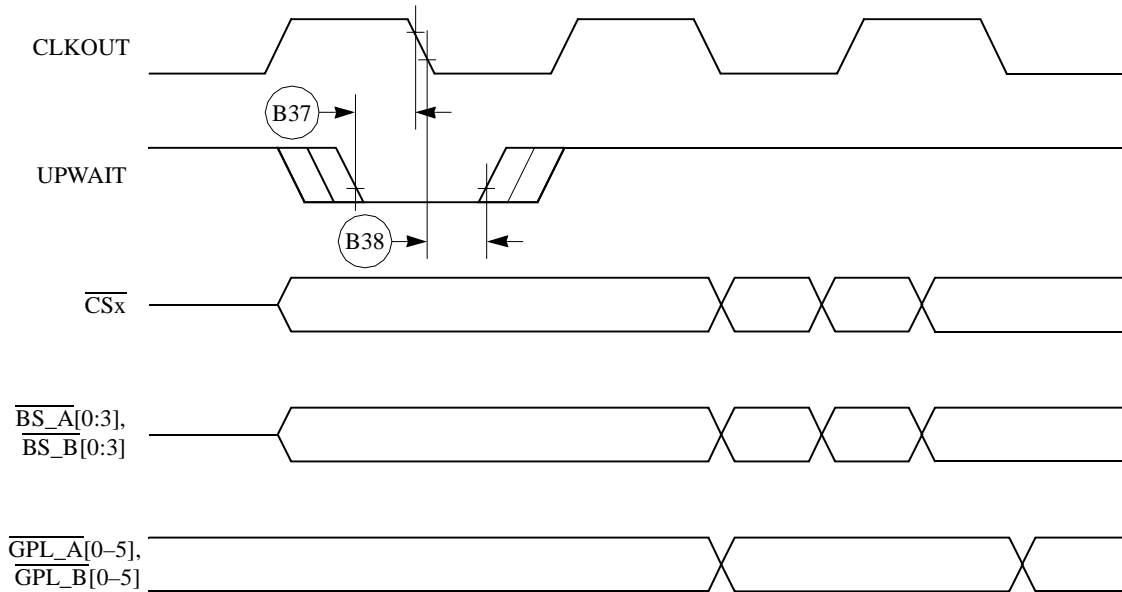Figure 18 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

Figure 18. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Table 7 provides interrupt timing for the MPC850.

Table 7. Interrupt Timing

Num	Characteristic [1]	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
I39	IRQx valid to CLKOUT rising edge (set up time)	6.00	—	6.00	—	6.00	—	ns
I40	IRQx hold time after CLKOUT.	2.00	—	2.00	—	2.00	—	ns
I41	IRQx pulse width low	3.00	—	3.00	—	3.00	—	ns
I42	IRQx pulse width high	3.00	—	3.00	—	3.00	—	ns
I43	IRQx edge-to-edge time	80.00	—	121.0	—	100.0	—	ns

[1] The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.
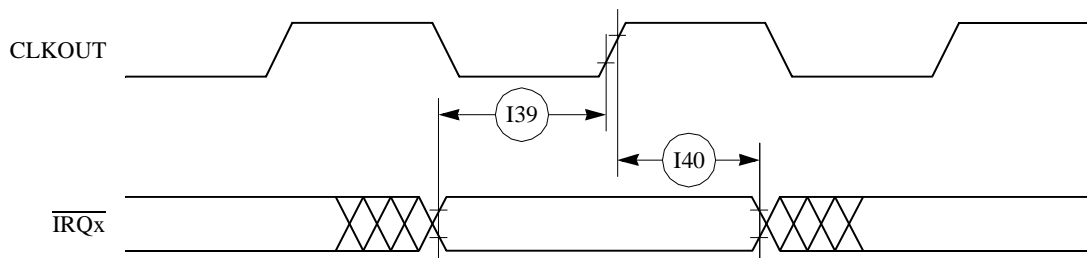

Figure 22. Interrupt Detection Timing for External Level Sensitive Lines

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.
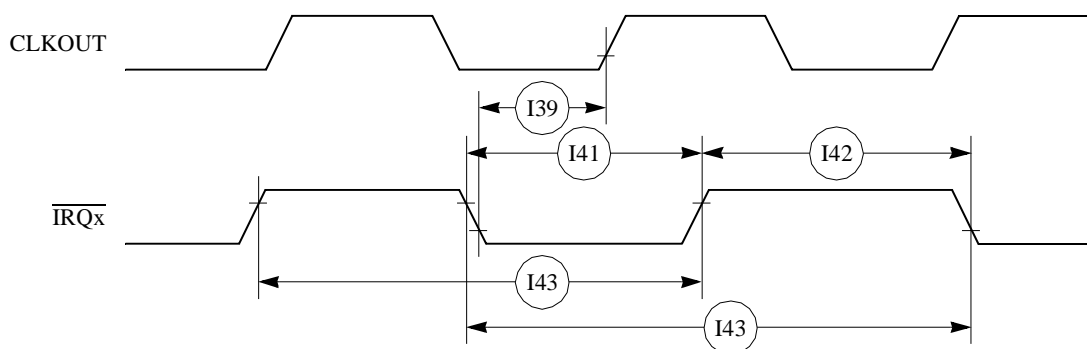
Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines

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Figure 31 shows the reset timing for the data bus configuration.

Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

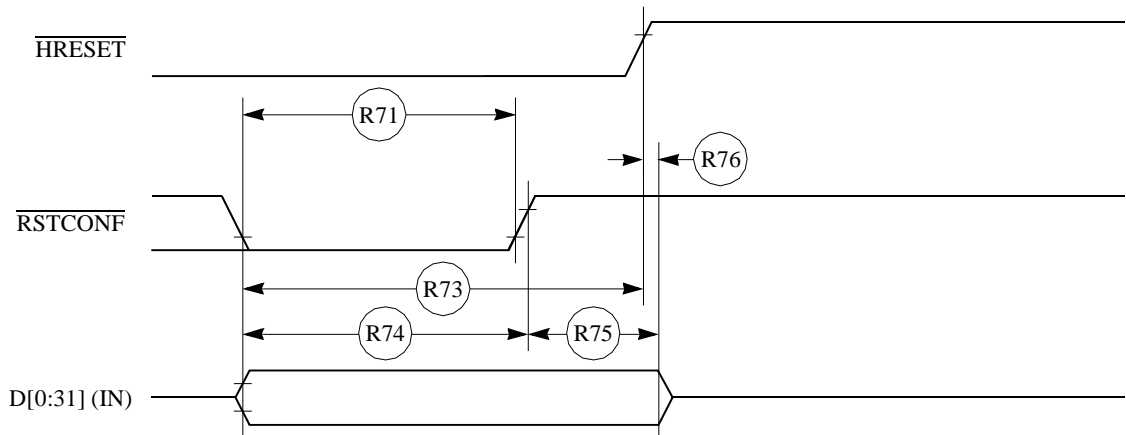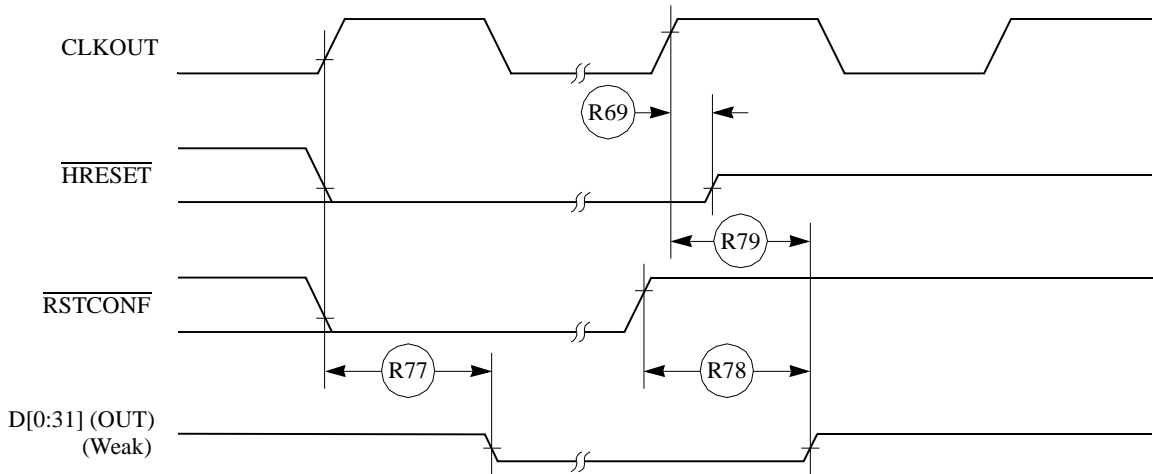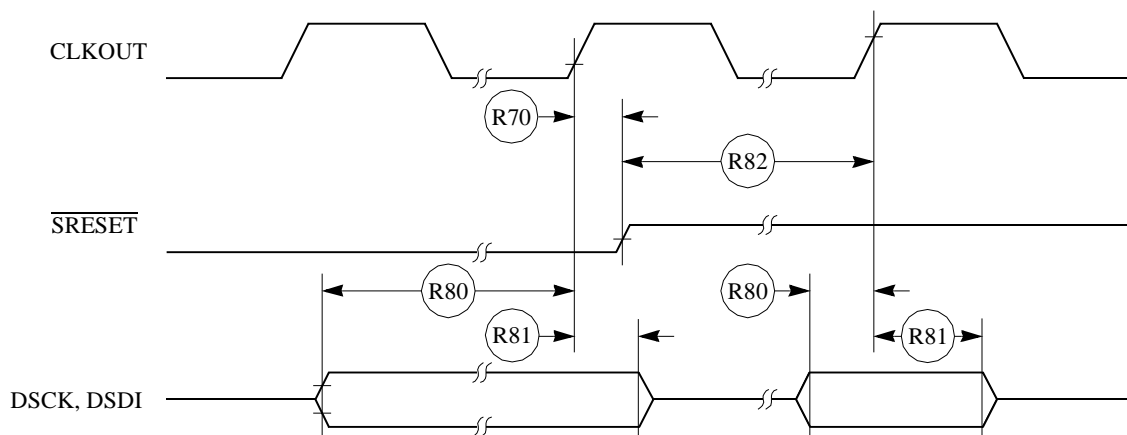Figure 33 provides the reset timing for the debug port configuration.

Figure 33. Reset Timing—Debug Port Configuration

7   IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

Table 12. JTAG Timing

| Num	Characteristic	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
J82	TCK cycle time	100.00	—	100.00	—	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	40.00	—	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	5.00	—	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	25.00	—	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	—	27.00	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	0.00	—	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	—	20.00	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	100.00	—	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	40.00	—	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	—	50.00	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	—	50.00	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	—	50.00	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	50.00	—	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	50.00	—	50.00	—	ns
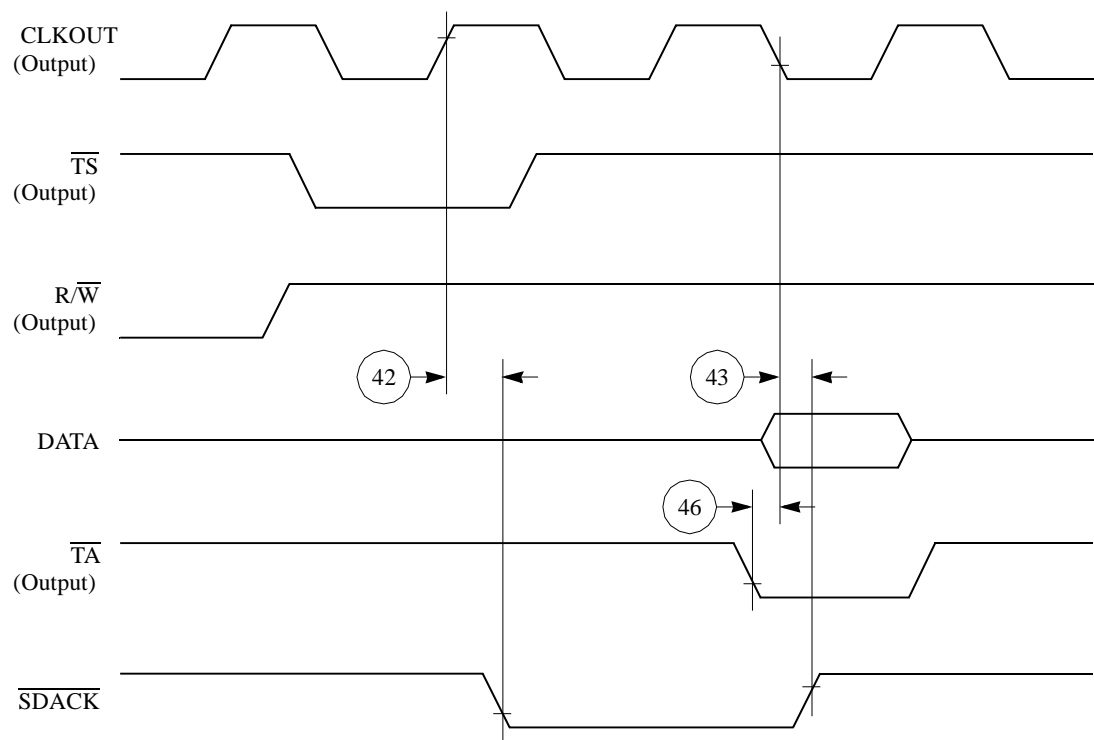
Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock

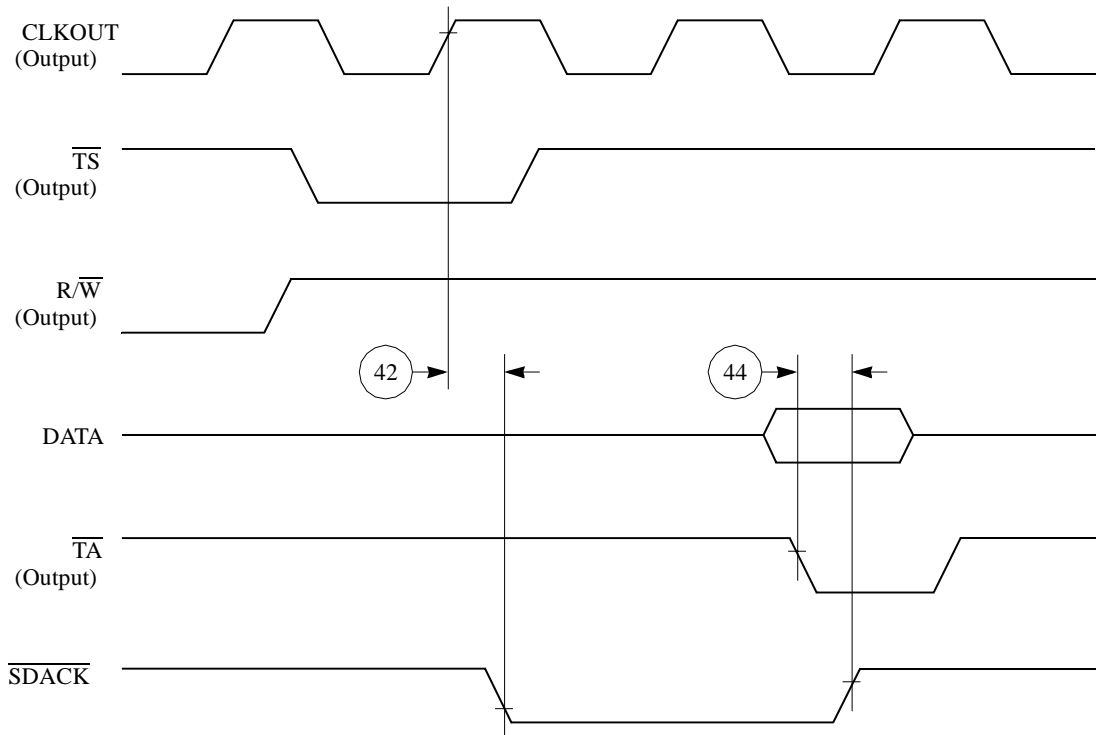**Figure 41. SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock**
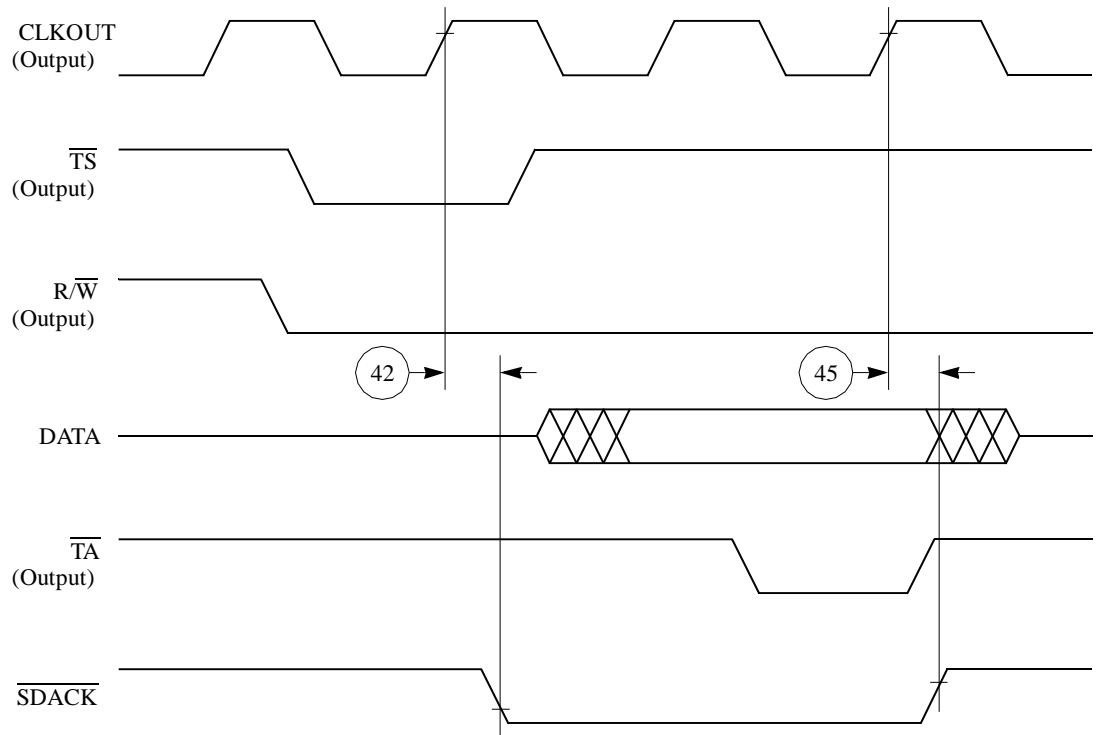
Figure 42. SDACK Timing Diagram—Peripheral Read
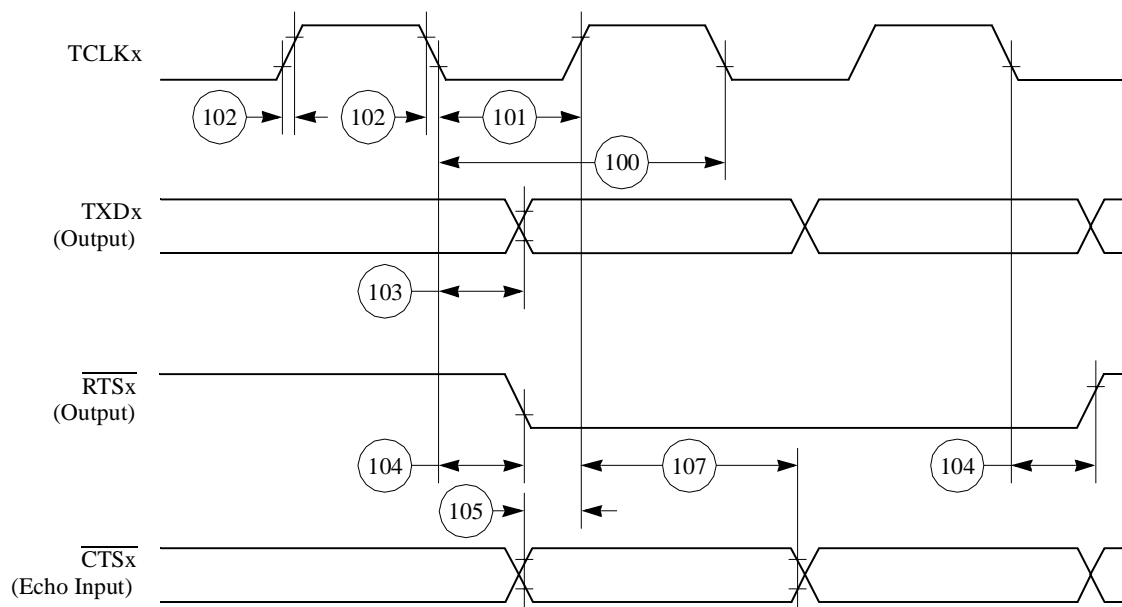
Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period [1]	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period[1]	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns

Table 24. I²C Timing (SCL < 100 KHz) (CONTINUED)

Num	Characteristic	All Frequencies		Unit
		Min	**Max**	
210	SDL/SCL fall time	—	300.00	ns
211	Stop condition setup time	4.70	—	µs

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I²C (SCL > 100 KHz) timings.

Table 25. I²C Timing (SCL > 100 KHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	**Max**	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) [1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	s
203	Low period of SCL		1/(2.2 * fSCL)	—	s
204	High period of SCL		1/(2.2 * fSCL)	—	s
205	Start condition setup time		1/(2.2 * fSCL)	—	s
206	Start condition hold time		1/(2.2 * fSCL)	—	s
207	Data hold time		0	—	s
208	Data setup time		1/(40 * fSCL)	—	s
209	SDL/SCL rise time		—	1/(10 * fSCL)	s
210	SDL/SCL fall time		—	1/(33 * fSCL)	s
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

[1] SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.
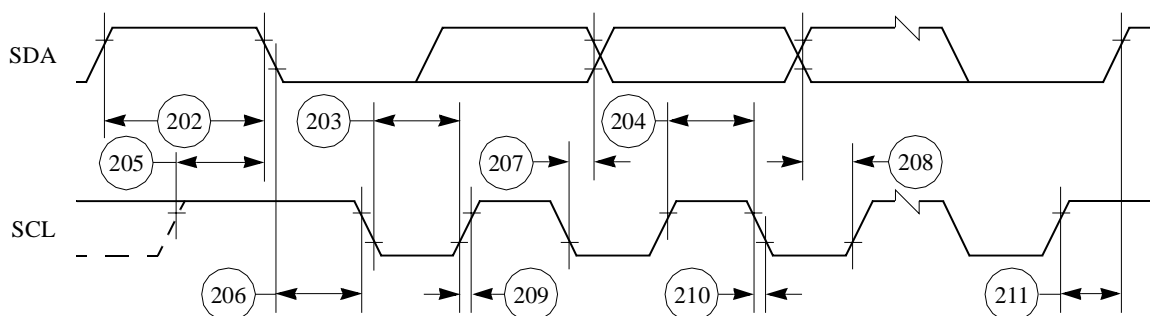
Figure 61 shows the I²C bus timing.

Figure 61. I²C Bus Timing Diagram

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customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.
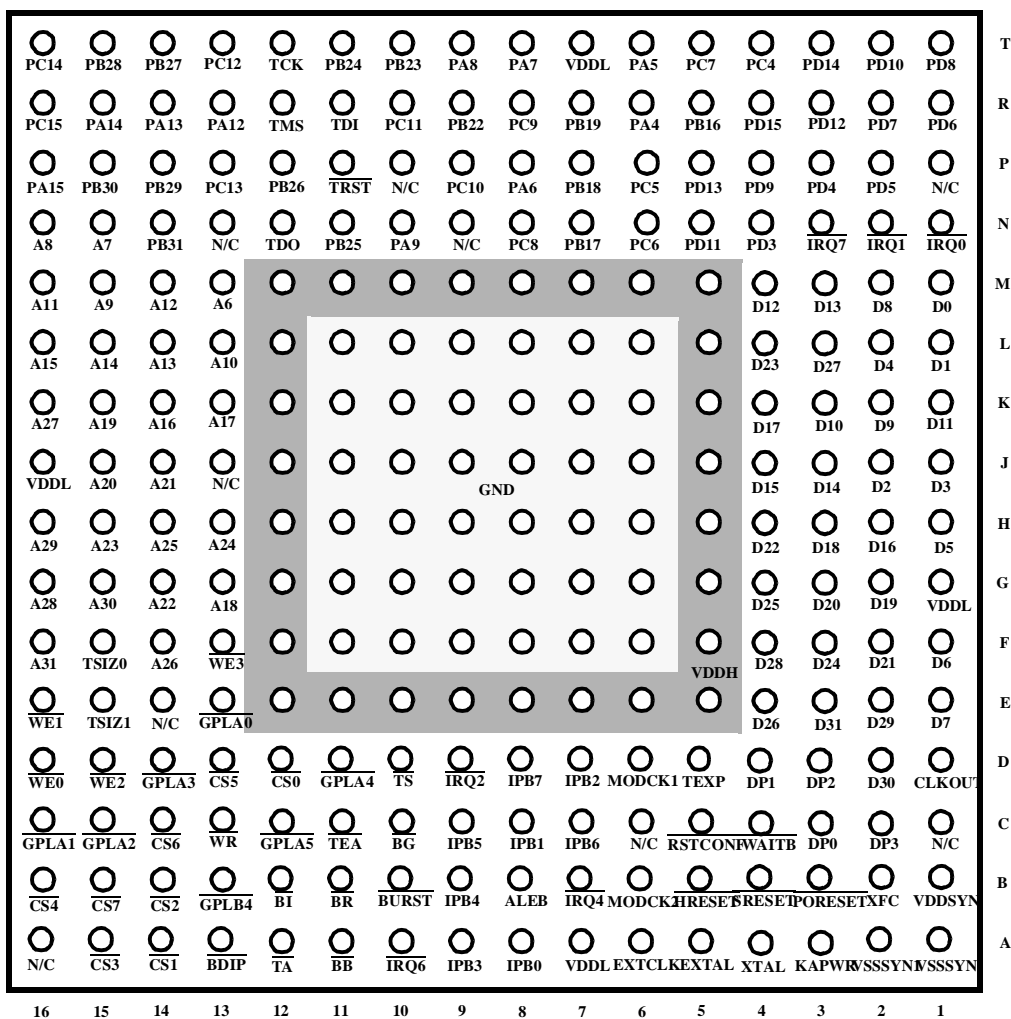
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
T	PC14	PB28	PB27	PC12	TCK	PB24	PB23	PA8	PA7	VDDL	PA5	PC7	PC4	PD14	PD10	PD8
R	PC15	PA14	PA13	PA12	TMS	TDI	PC11	PB22	PC9	PB19	PA4	PB16	PD15	PD12	PD7	PD6
P	PA15	PB30	PB29	PC13	PB26	TRST	N/C	PC10	PA6	PB18	PC5	PD13	PD9	PD4	PD5	N/C
N	A8	A7	PB31	N/C	TDO	PB25	PA9	N/C	PC8	PB17	PC6	PD11	PD3	IRQ7	IRQ1	IRQ0
M	A11	A9	A12	A6									D12	D13	D8	D0
L	A15	A14	A13	A10									D23	D27	D4	D1
K	A27	A19	A16	A17									D17	D10	D9	D11
J	VDDL	A20	A21	N/C				GND					D15	D14	D2	D3
H	A29	A23	A25	A24									D22	D18	D16	D5
G	A28	A30	A22	A18									D25	D20	D19	VDDL
F	A31	TSIZ0	A26	WE3							VDDH		D28	D24	D21	D6
E	WE1	TSIZ1	N/C	GPLA0									D26	D31	D29	D7
D	WE0	WE2	GPLA3	CS5	CS0	GPLA4	TS	IRQ2	IPB7	IPB2	MODCK1	TEXP	DP1	DP2	D30	CLKOUT
C	GPLA1	GPLA2	CS6	WR	GPLA5	TEA	BG	IPB5	IPB1	IPB6	N/C	RSTCONF	WAITB	DP0	DP3	N/C
B	CS4	CS7	CS2	GPLB4	BI	BR	BURST	IPB4	ALEB	IRQ4	MODCK2	HRESET	SRESET	PORESET	XFC	VDDSYN
A	N/C	CS3	CS1	BDIP	TA	BB	IRQ6	IPB3	IPB0	VDDL	EXTCLK	EXTAL	XTAL	KAPWR	VSSSYN1	VSSSYN

Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

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