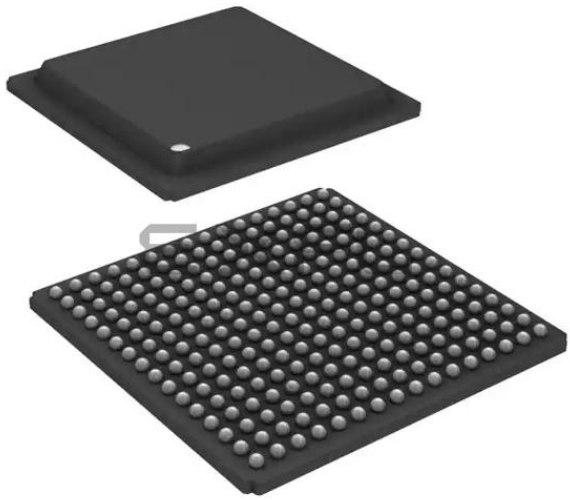

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850czq50bu

2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:

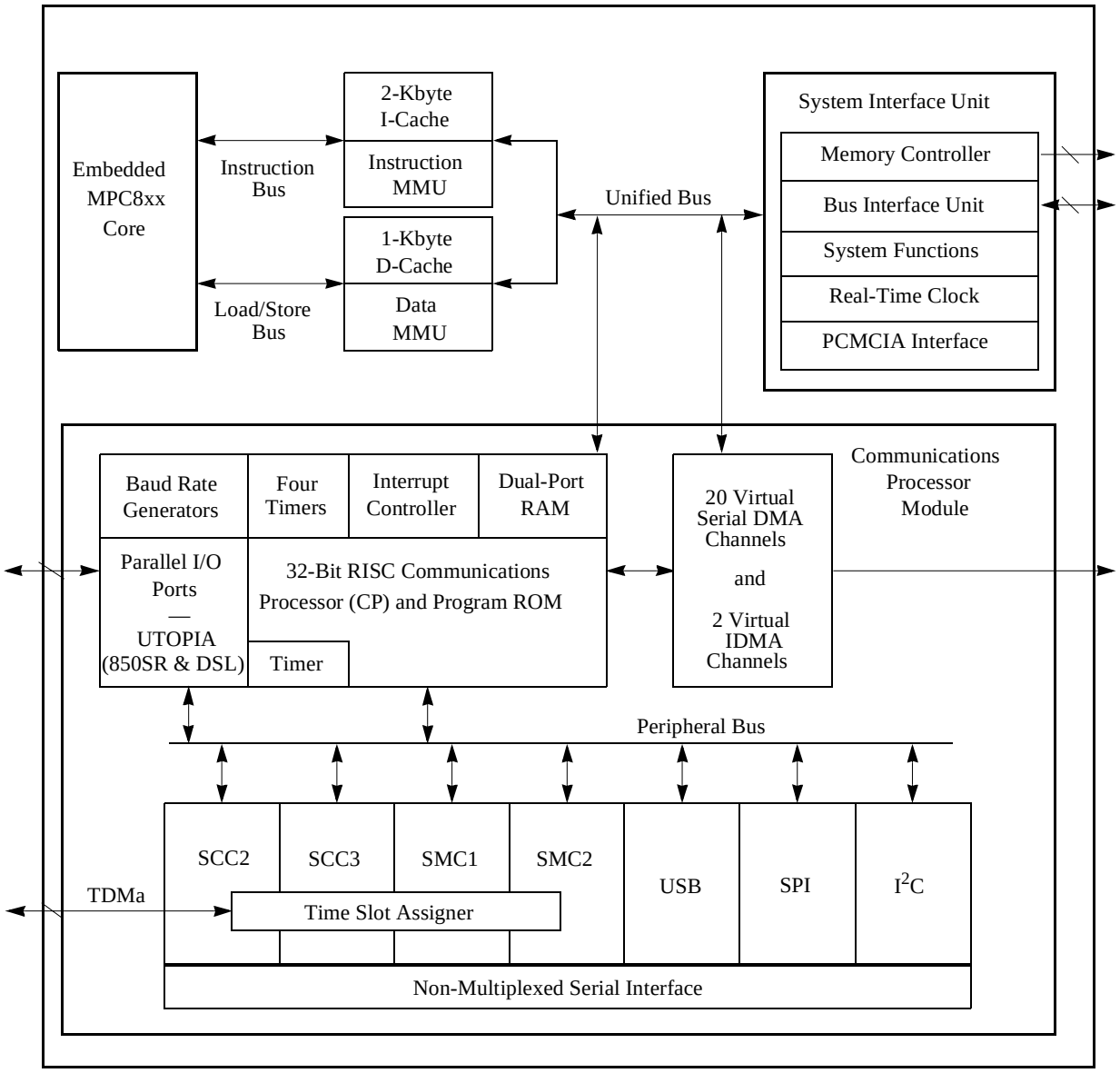


Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

  - 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
    - Caches are two-way, set-associative
    - Physically addressed
    - Cache blocks can be updated with a 4-word line burst
    - Least-recently used (LRU) replacement algorithm
    - Lockable one-line granularity
  - Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
  - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
  - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
  - Hardware bus monitor
  - Spurious interrupt monitor
  - Software watchdog
  - Periodic interrupt timer
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
  - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
  - Memory controller programmable to support most size and speed memory interfaces
  - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
  - Variable block sizes, 32 Kbytes to 256 Mbytes
  - Selectable write protection
  - On-chip bus arbiter supports one external bus master
  - Special features for burst mode support
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers

- QUICC multichannel controller (QMC) microcode features
  - Up to 64 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
  - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One $I^2C^{®}$ (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and CPM in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA [1]	θ_{JA}	40 [2]	°C/W
	θ_{JA}	31 [3]	°C/W
	θ_{JA}	24 [4]	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

[1] For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

[2] Assumes natural convection and a single layer board (no thermal vias).

[3] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

[4] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

[1] Typical power dissipation is measured at 3.3V

[2] Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B9	CLKOUT to A[6–31] RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3], $\overline{TSIZ}$[0–1], $\overline{REG}$, $\overline{RSV}$, AT[0–3], $\overline{PTR}$ high-Z	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion	5.00	11.00	7.58	13.58	6.25	12.25	0.250	50.00	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion, (When driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	—	50.00	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	—	50.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ high-Z	5.00	19.00	7.58	21.58	6.25	20.25	0.250	50.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ high-Z, (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion	2.50	10.00	2.50	10.00	2.50	10.00	—	50.00	ns
B15	CLKOUT to $\overline{TEA}$ high-Z	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT(setup time) [5]	9.75	—	9.75	—	9.75	—	—	50.00	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, valid to CLKOUT (setup time) [5]	10.00	—	10.00	—	10.00	—	—	50.00	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid to CLKOUT (setup time) [6]	8.50	—	8.50	—	8.50	—	—	50.00	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (Hold time).[5]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, except $\overline{TEA}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B18	D[0–31], DP[0–3] valid to CLKOUT rising edge (setup time) [7]	6.00	—	6.00	—	6.00	—	—	50.00	ns
B19	CLKOUT rising edge to D[0–31], DP[0–3] valid (hold time) [7]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B20	D[0–31], DP[0–3] valid to CLKOUT falling edge (setup time) [8]	4.00	—	4.00	—	4.00	—	—	50.00	ns
B21	CLKOUT falling edge to D[0–31], DP[0–3] valid (hold time) [8]	2.00	—	2.00	—	2.00	—	—	—	—

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B29h	$\overline{WE}$[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B29i	$\overline{CS}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B30	$\overline{CS}$, $\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access [9]	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B30a	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A[6–31] invalid GPCM write access TRLX = 0, CSNT =1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B30b	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A[6–31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B30c	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	8.00	—	6.00	—	0.375	50.00	ns
B30d	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B33a	CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B34	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B34a	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B34b	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B35	A[6–31] to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B35a	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by BST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B35b	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B36	A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B37	UPWAIT valid to CLKOUT falling edge [10]	6.00	—	6.00	—	6.00	—	—	50.00	ns
B38	CLKOUT falling edge to UPWAIT valid [10]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [11]	7.00	—	7.00	—	7.00	—	—	50.00	ns
B40	A[6–31], TSIZ[0–1], RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge.	7.00	—	7.00	—	7.00	—	—	50.00	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	—	50.00	ns

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

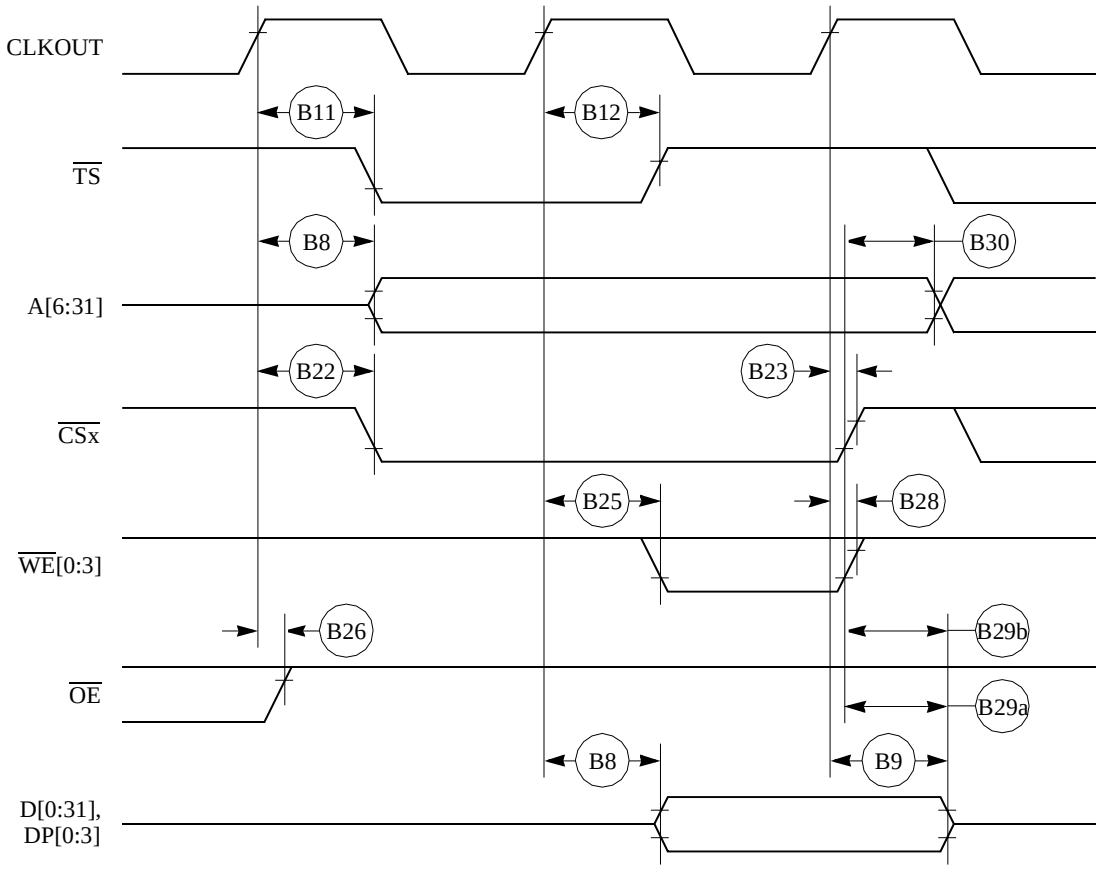


Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

Figure 17 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

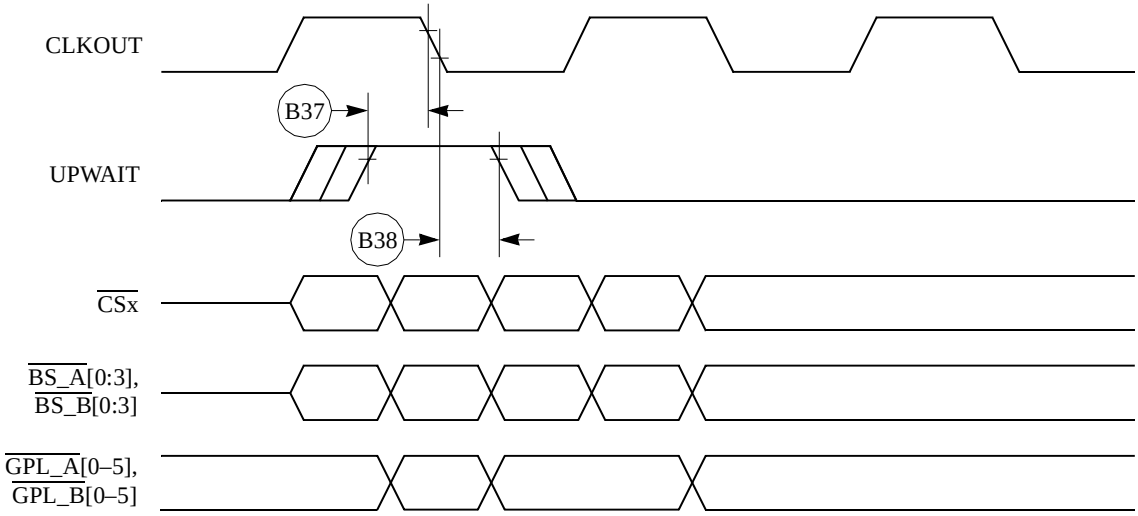


Figure 17. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 18 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

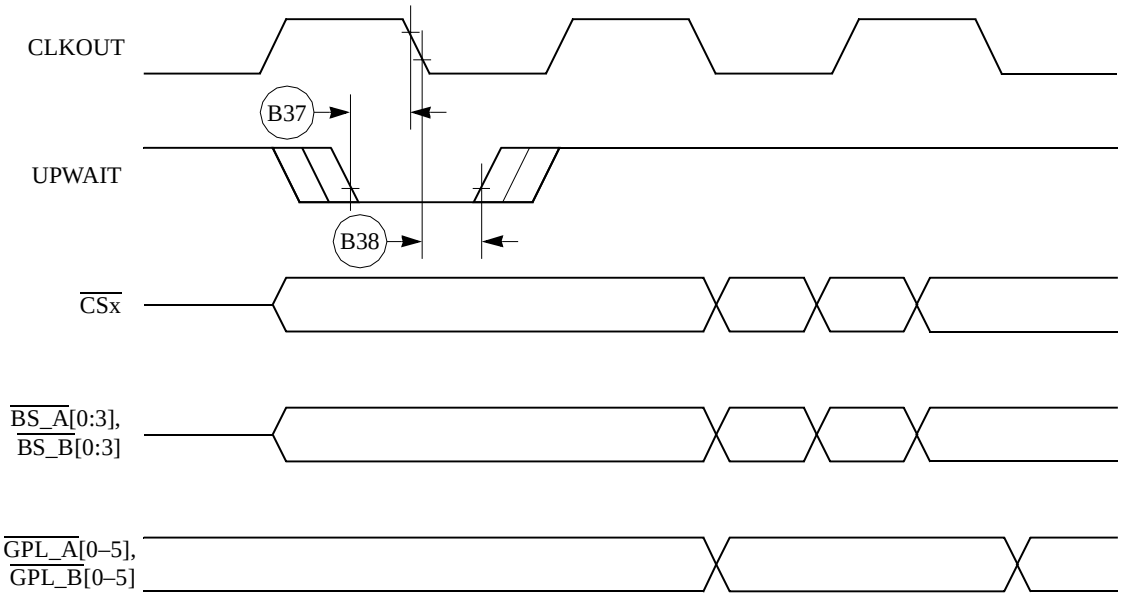


Figure 18. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

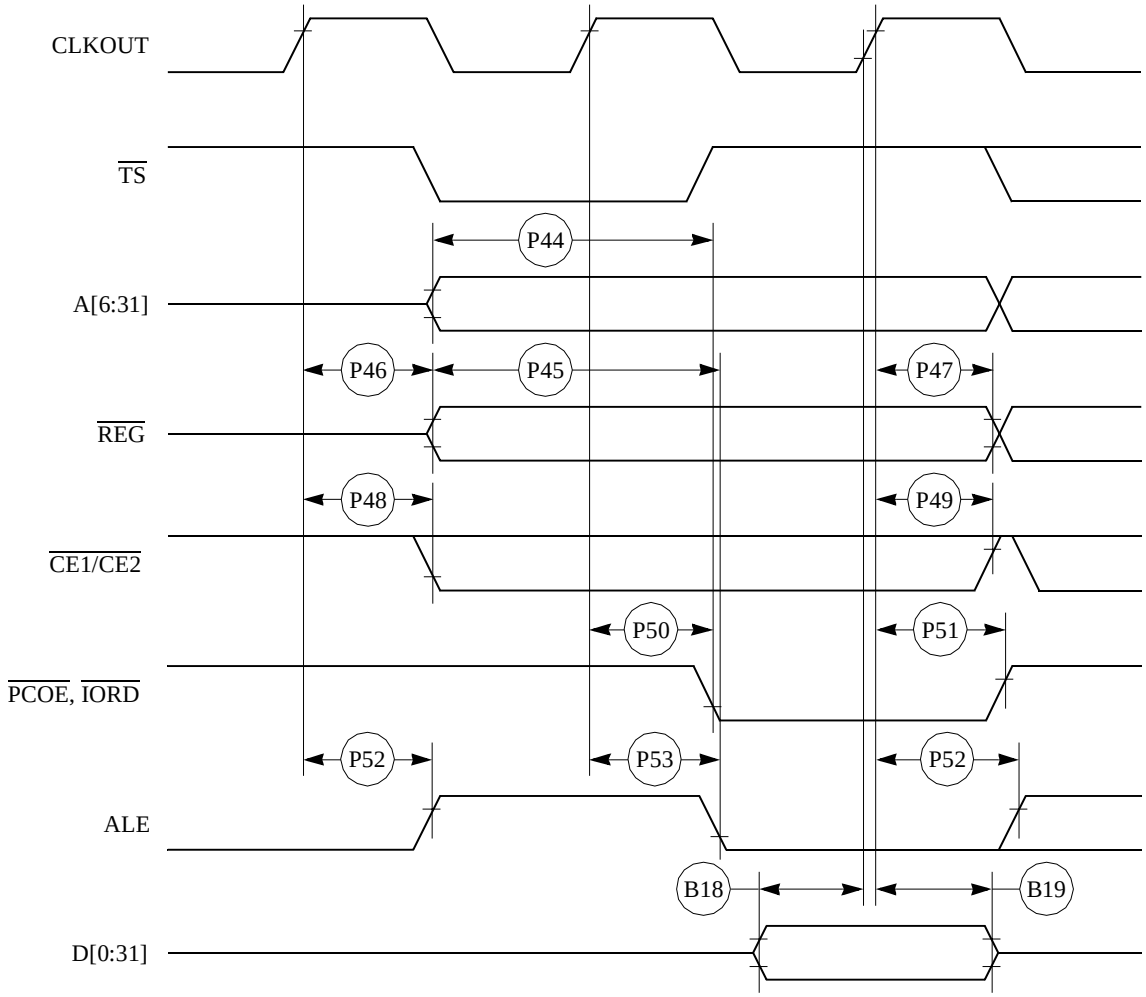


Figure 24. PCMCIA Access Cycles Timing External Bus Read

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

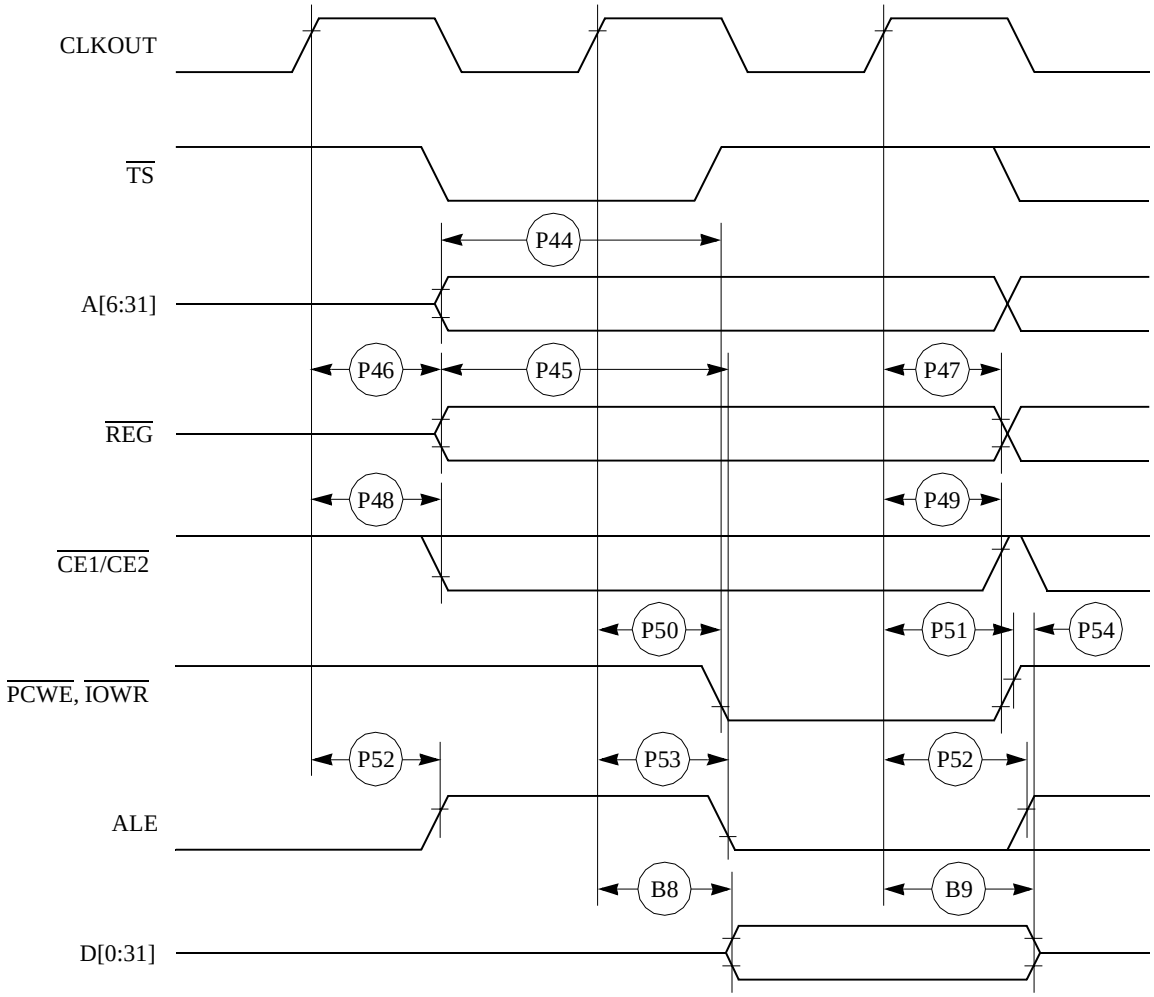


Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.

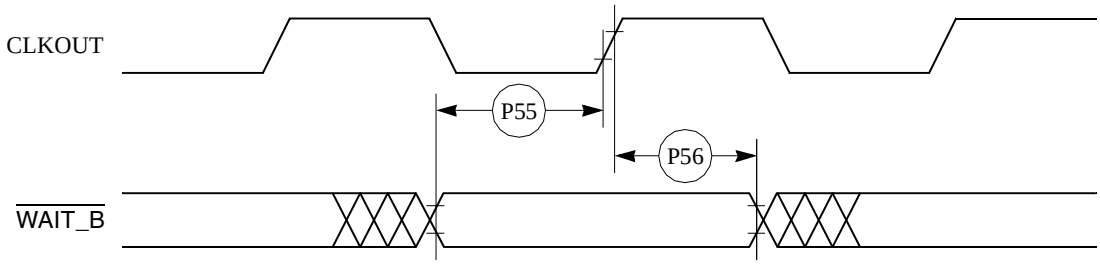


Figure 26. PCMCIA WAIT Signal Detection Timing

Figure 33 provides the reset timing for the debug port configuration.

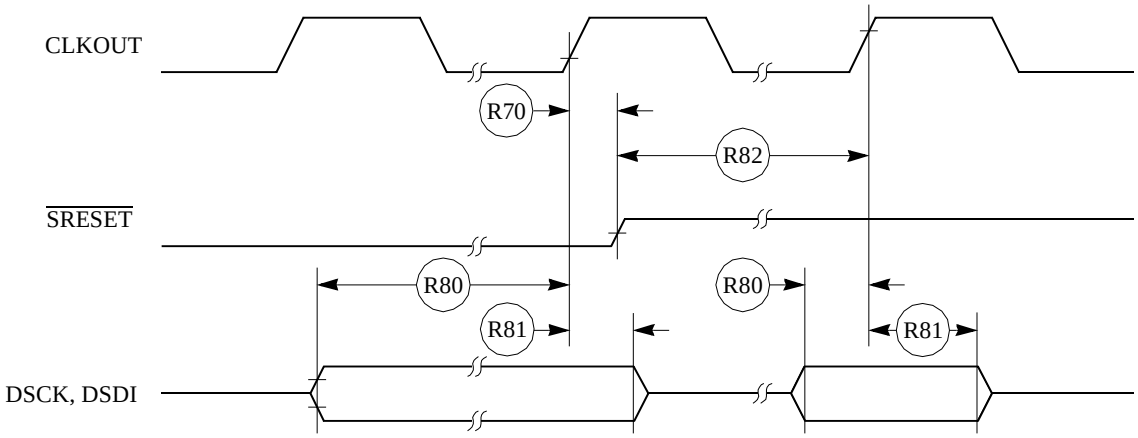


Figure 33. Reset Timing—Debug Port Configuration

7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

Table 12. JTAG Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
J82	TCK cycle time	100.00	—	100.00	—	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	40.00	—	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	5.00	—	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	25.00	—	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	—	27.00	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	0.00	—	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	—	20.00	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	100.00	—	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	40.00	—	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	—	50.00	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	—	50.00	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	—	50.00	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	50.00	—	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	50.00	—	50.00	—	ns

8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns

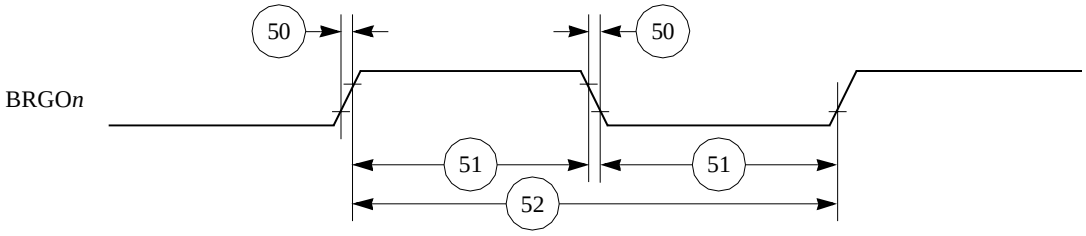


Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Table 16. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10.00	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1.00	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2.00	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3.00	—	clk
65	CLKO high to $\overline{\text{TOUT}}$ valid	3.00	25.00	ns

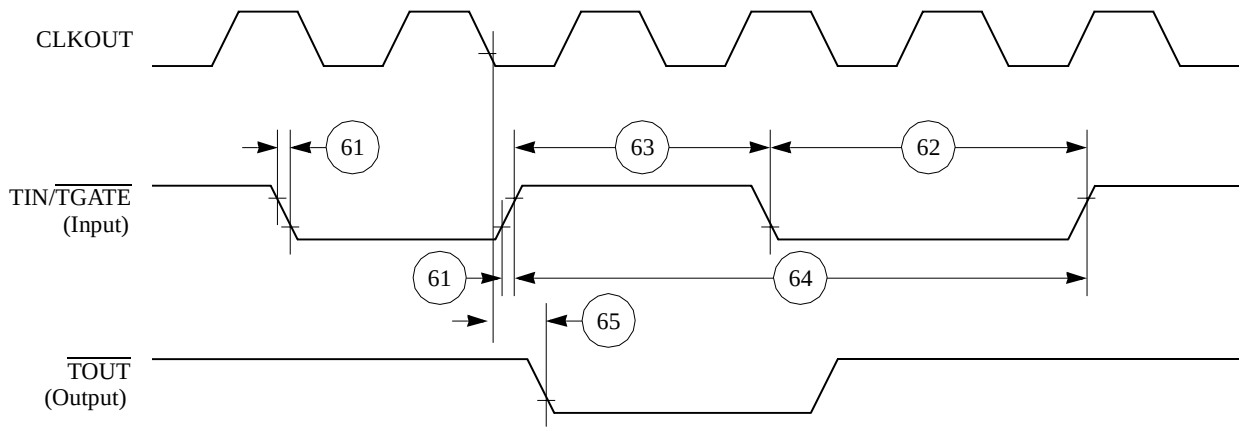


Figure 44. CPM General-Purpose Timers Timing Diagram

8.5 Serial Interface AC Electrical Specifications

Table 17 provides the serial interface timings as shown in Figure 45 to Figure 49.

Table 17. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) [1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXD, L1ST*n*, $\overline{\text{L1RQ}}$, L1xCLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1xCLK edge Edge (SYNC setup time)	20.00	—	ns
74	L1xCLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1xCLK edge (L1RXD setup time)	17.00	—	ns
77	L1xCLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1xCLK edge to L1ST*n* valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST*n* valid	10.00	45.00	ns
79	L1xCLK edge to L1ST*n* invalid	10.00	45.00	ns
80	L1xCLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1xCLK edge to L1TXD high impedance	0.00	42.00	ns

Table 17. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83A	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

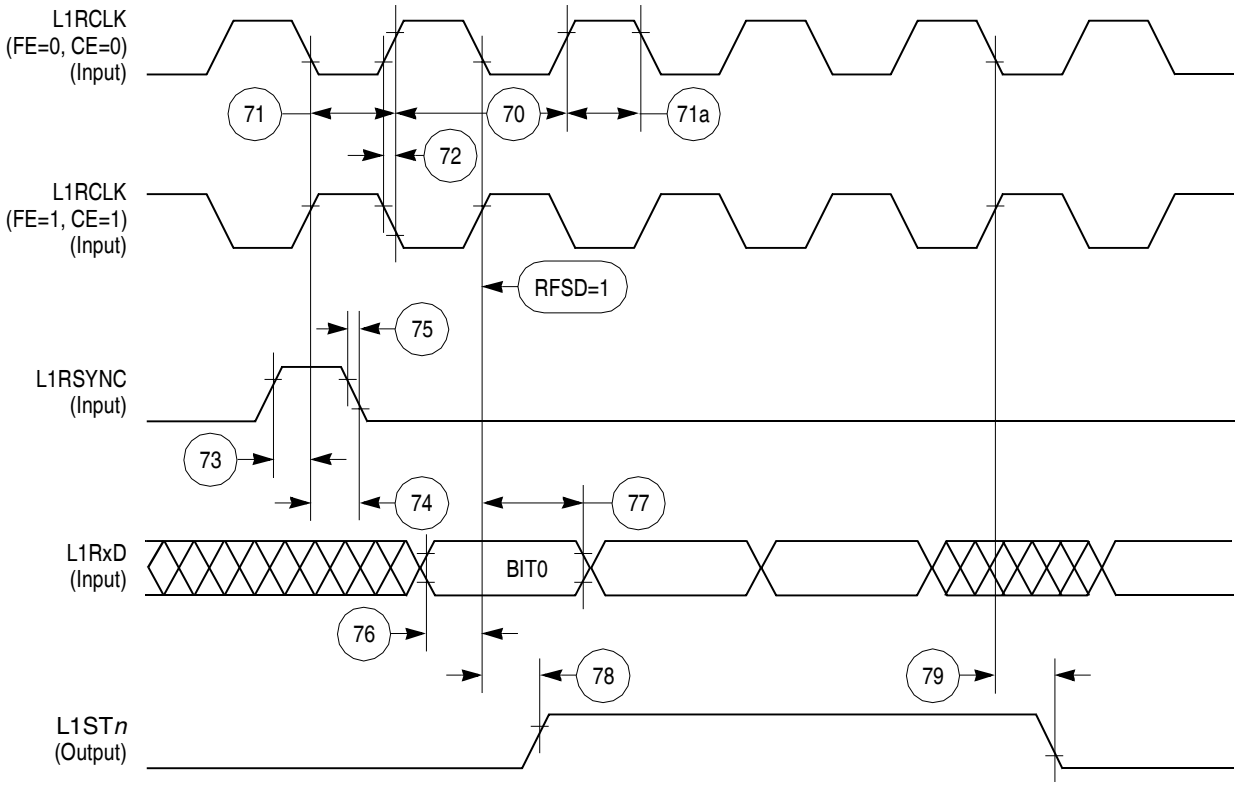


Figure 45. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

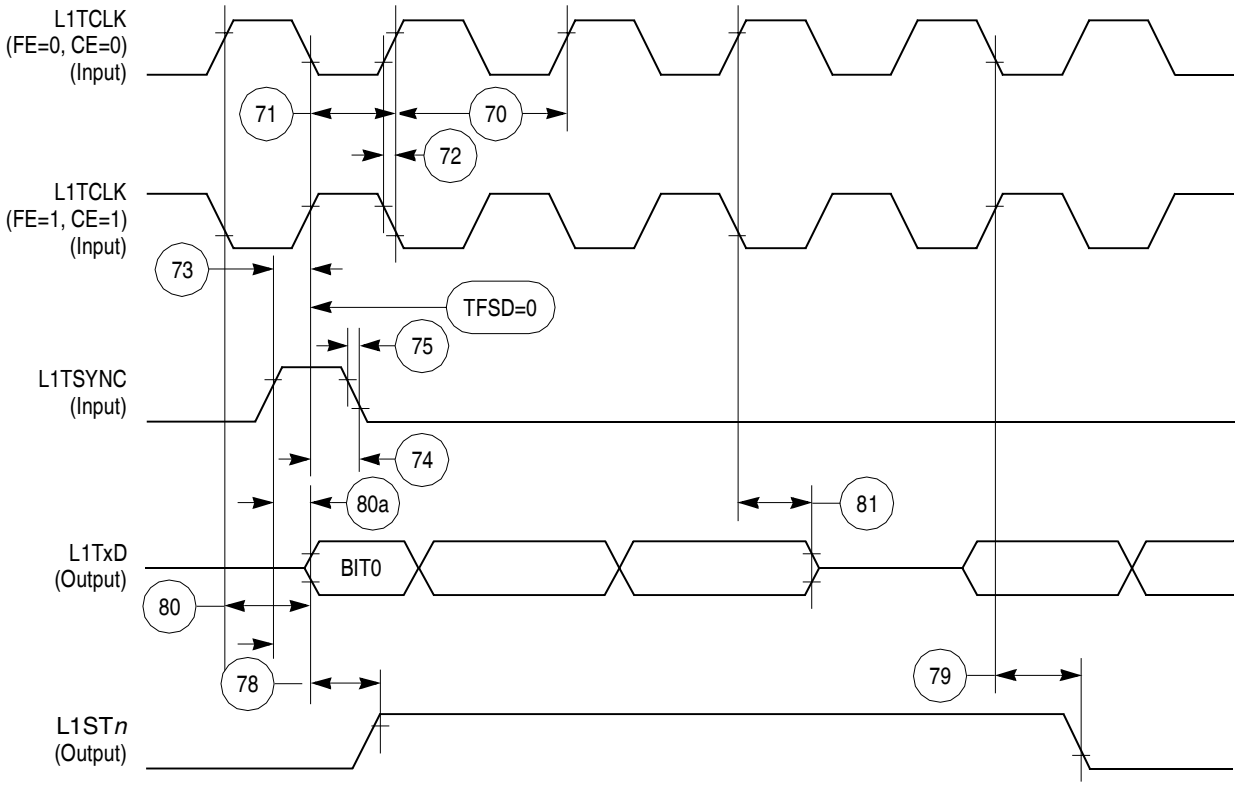


Figure 47. SI Transmit Timing Diagram

Figure 50 through Figure 52 show the NMSI timings.

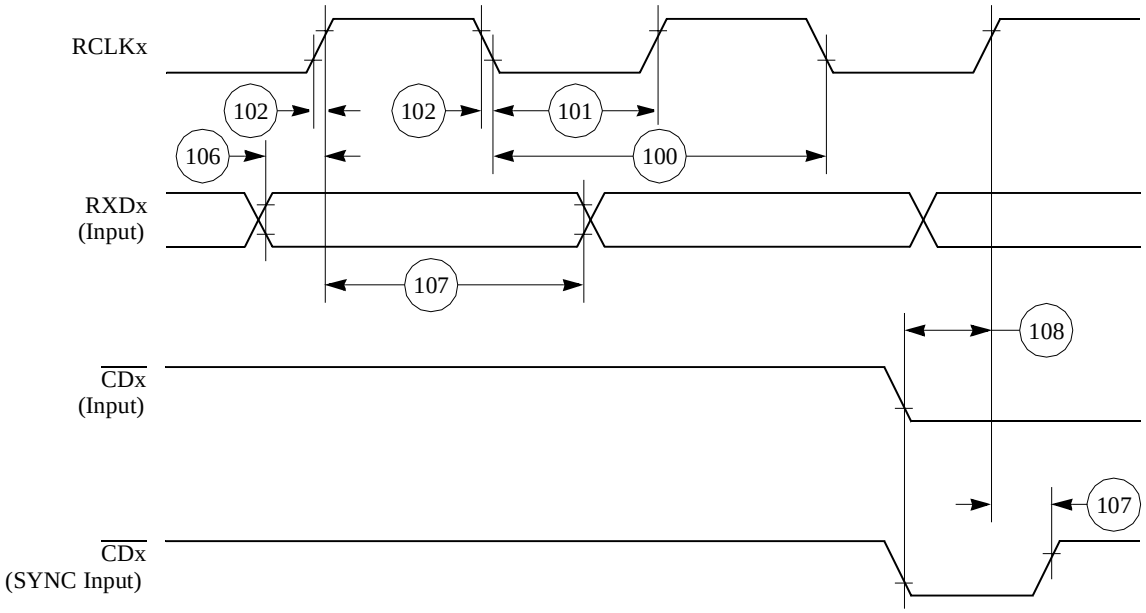


Figure 50. SCC NMSI Receive Timing Diagram

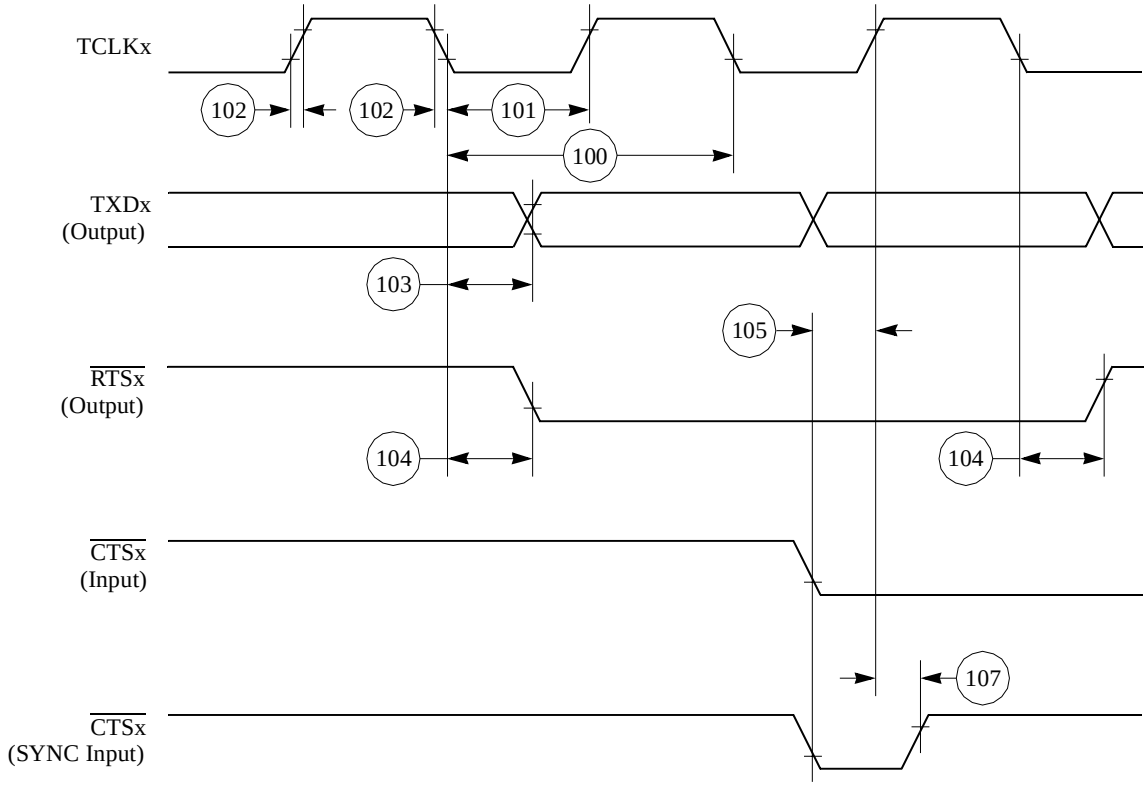


Figure 51. SCC NMSI Transmit Timing Diagram

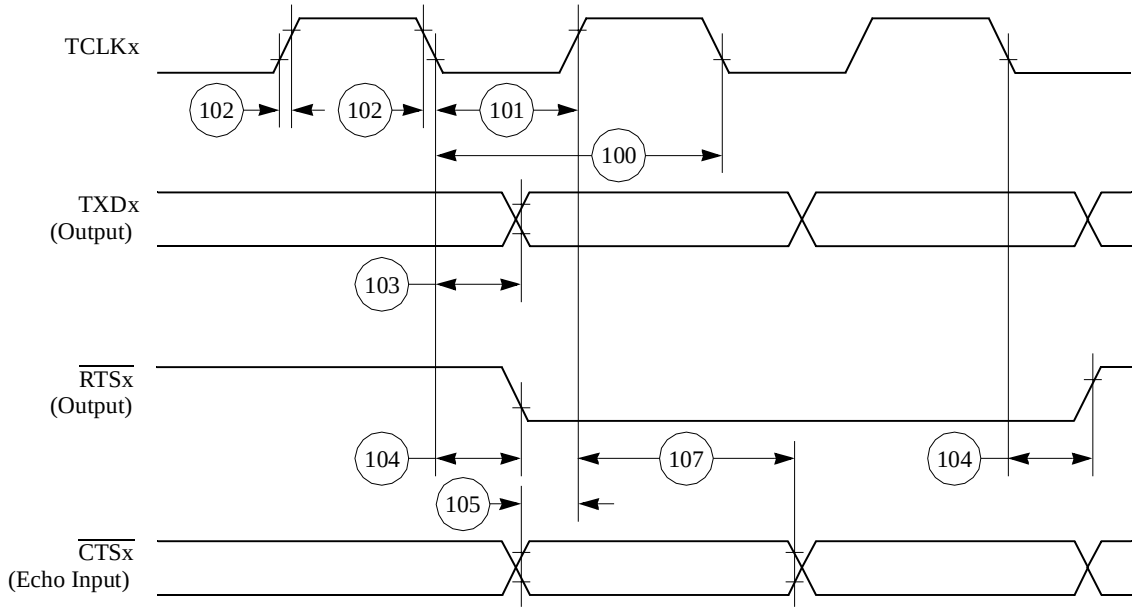


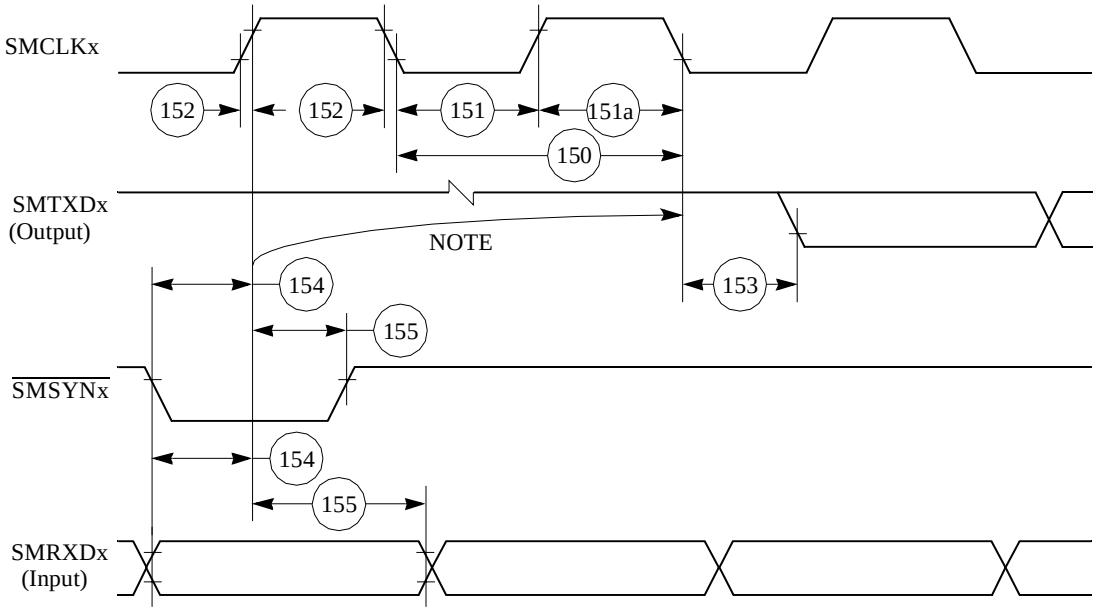
Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period [1]	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period[1]	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 56. SMC Transparent Timing Diagram

8.9 SPI Master AC Electrical Specifications

Table 22 provides the SPI master timings as shown in Figure 57 and Figure 58.

Table 22. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50.00	—	ns
163	Master data hold time (inputs)	0.00	—	ns
164	Master data valid (after SCK edge)	—	20.00	ns
165	Master data hold time (outputs)	0.00	—	ns
166	Rise time output	—	15.00	ns
167	Fall time output	—	15.00	ns

9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivatives

Device	Ethernet Support	Number of SCCs [1]	32-Channel HDLC Support	64-Channel HDLC Support [2]
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

1 Serial Communication Controller (SCC)

2 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support