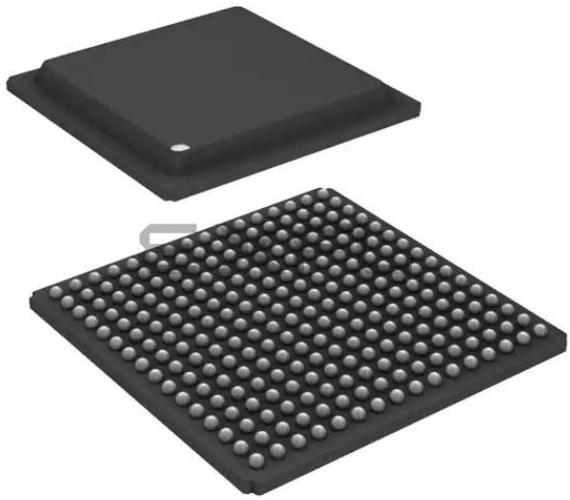

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850decvr50bu

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I^2C port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

Table 1. MPC850 Functionality Matrix

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Additional documentation may be provided for parts listed in Table 1.

2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:

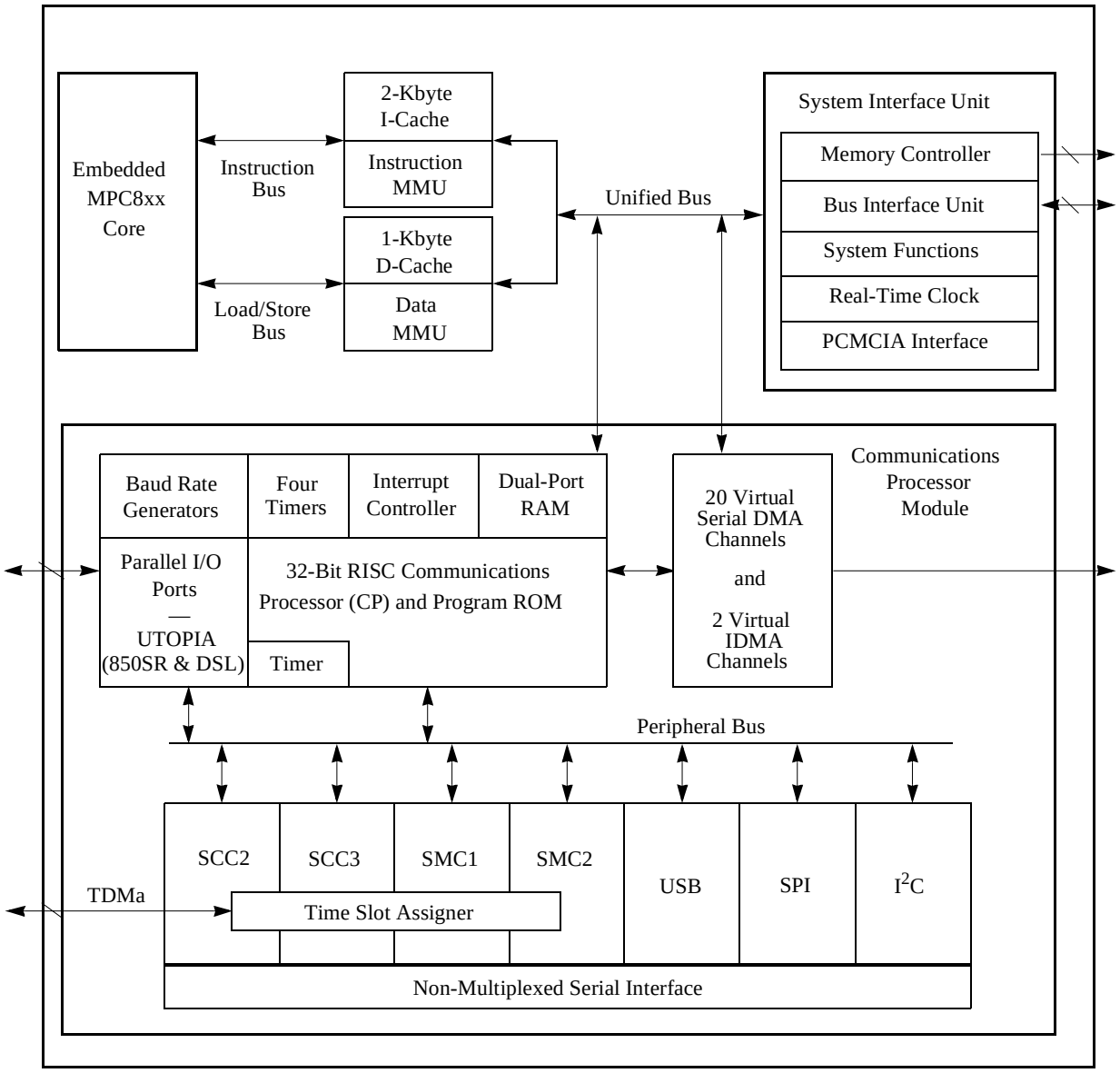

Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

  - Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
  - Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - The MPC850 can compare using the =, ≠, <, and > conditions to generate watchpoints
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility on all general purpose I/O pins.

3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC850. Table 2 provides the maximum ratings.

Table 2. Maximum Ratings

(GND = 0V)

Rating	Symbol	Value	Unit
Supply voltage	VDDH	-0.3 to 4.0	V
	VDDL	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	VDDSYN	-0.3 to 4.0	V
Input voltage [1]	V_{in}	GND-0.3 to VDDH + 2.5 V	V
Junction temperature [2]	T_j	0 to 95 (standard) -40 to 95 (extended)	°C
Storage temperature range	T_{stg}	-55 to +150	°C

1 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
CAUTION: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC850 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

2 The MPC850, a high-frequency device in a BGA package, does not provide a guaranteed maximum ambient temperature. Only maximum junction temperature is guaranteed. It is the responsibility of the user to consider power dissipation and thermal management. Junction temperature ratings are the same regardless of frequency rating of the device.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}). Table 3 provides the package thermal characteristics for the MPC850.

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA [1]	θ_{JA}	40 [2]	°C/W
	θ_{JA}	31 [3]	°C/W
	θ_{JA}	24 [4]	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

[1] For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

[2] Assumes natural convection and a single layer board (no thermal vias).

[3] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

[4] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

[1] Typical power dissipation is measured at 3.3V

[2] Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B9	CLKOUT to A[6–31] RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3], $\overline{TSIZ}$[0–1], $\overline{REG}$, $\overline{RSV}$, AT[0–3], $\overline{PTR}$ high-Z	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion	5.00	11.00	7.58	13.58	6.25	12.25	0.250	50.00	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion, (When driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	—	50.00	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	—	50.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ high-Z	5.00	19.00	7.58	21.58	6.25	20.25	0.250	50.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ high-Z, (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion	2.50	10.00	2.50	10.00	2.50	10.00	—	50.00	ns
B15	CLKOUT to $\overline{TEA}$ high-Z	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT(setup time) [5]	9.75	—	9.75	—	9.75	—	—	50.00	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, valid to CLKOUT (setup time) [5]	10.00	—	10.00	—	10.00	—	—	50.00	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid to CLKOUT (setup time) [6]	8.50	—	8.50	—	8.50	—	—	50.00	ns
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (Hold time).[5]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, except $\overline{TEA}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B18	D[0–31], DP[0–3] valid to CLKOUT rising edge (setup time) [7]	6.00	—	6.00	—	6.00	—	—	50.00	ns
B19	CLKOUT rising edge to D[0–31], DP[0–3] valid (hold time) [7]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B20	D[0–31], DP[0–3] valid to CLKOUT falling edge (setup time) [8]	4.00	—	4.00	—	4.00	—	—	50.00	ns
B21	CLKOUT falling edge to D[0–31], DP[0–3] valid (hold time) [8]	2.00	—	2.00	—	2.00	—	—	—	—

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B33a	CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B34	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B34a	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B34b	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B35	A[6–31] to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B35a	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by BST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B35b	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B36	A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B37	UPWAIT valid to CLKOUT falling edge [10]	6.00	—	6.00	—	6.00	—	—	50.00	ns
B38	CLKOUT falling edge to UPWAIT valid [10]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [11]	7.00	—	7.00	—	7.00	—	—	50.00	ns
B40	A[6–31], TSIZ[0–1], RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge.	7.00	—	7.00	—	7.00	—	—	50.00	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	—	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	TBD	—	—	50.00	ns

1 The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR)$$

For maxima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR) + 1ns(CAP\ LOAD - 50) / 10$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

D_{50} is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

2 Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.

3 If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

4 The timing for $\overline{BR}$ output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC850 is selected to work with internal bus arbiter.

5 The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).

6 The timing required for $\overline{BR}$ input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC850 is selected to work with the external bus arbiter.

7 The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

8 The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

9 The timing B30 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE[0:3]}$ when CSNT = '0'.

10 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.

11 The $\overline{AS}$ signal is considered asynchronous to CLKOUT.

Figure 2 is the control timing diagram.

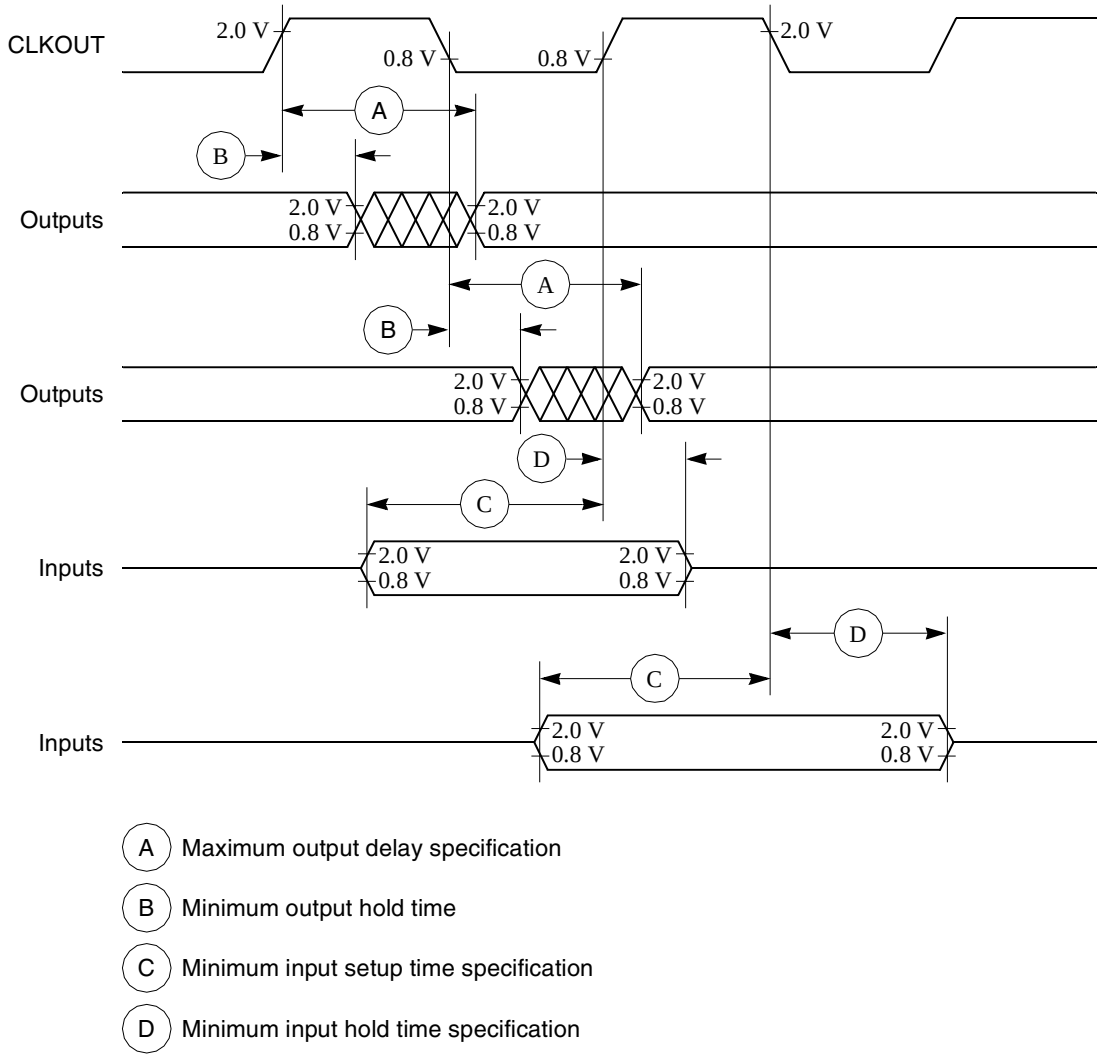

Figure 2. Control Timing

Figure 3 provides the timing for the external clock.

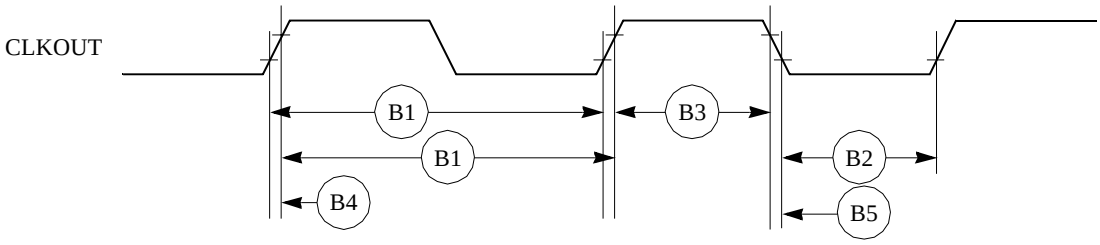

Figure 3. External Clock Timing

Figure 4 provides the timing for the synchronous output signals.

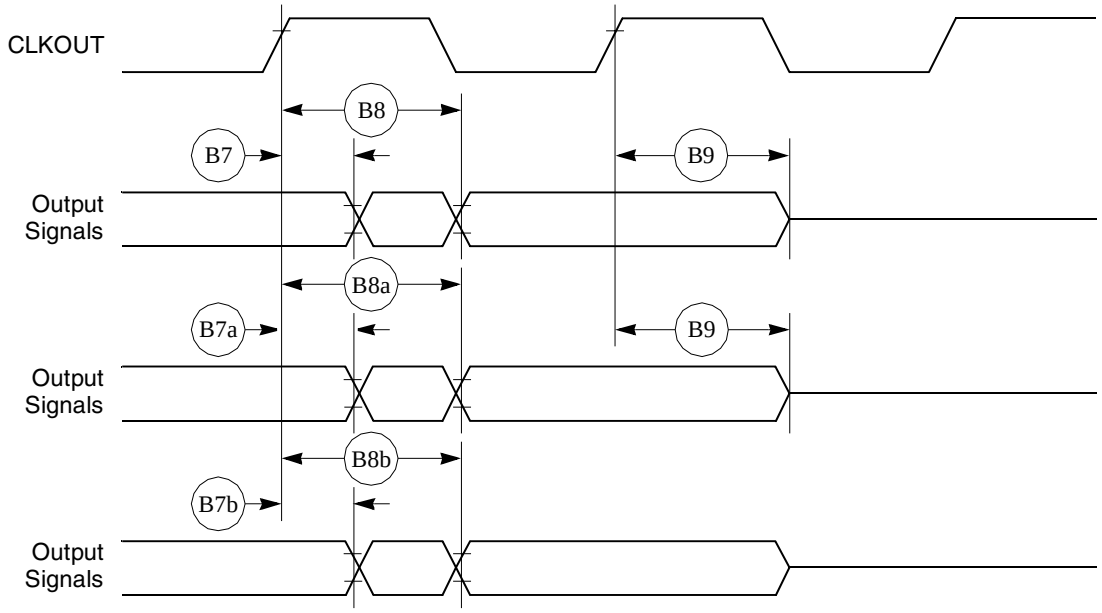

Figure 4. Synchronous Output Signals Timing

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.

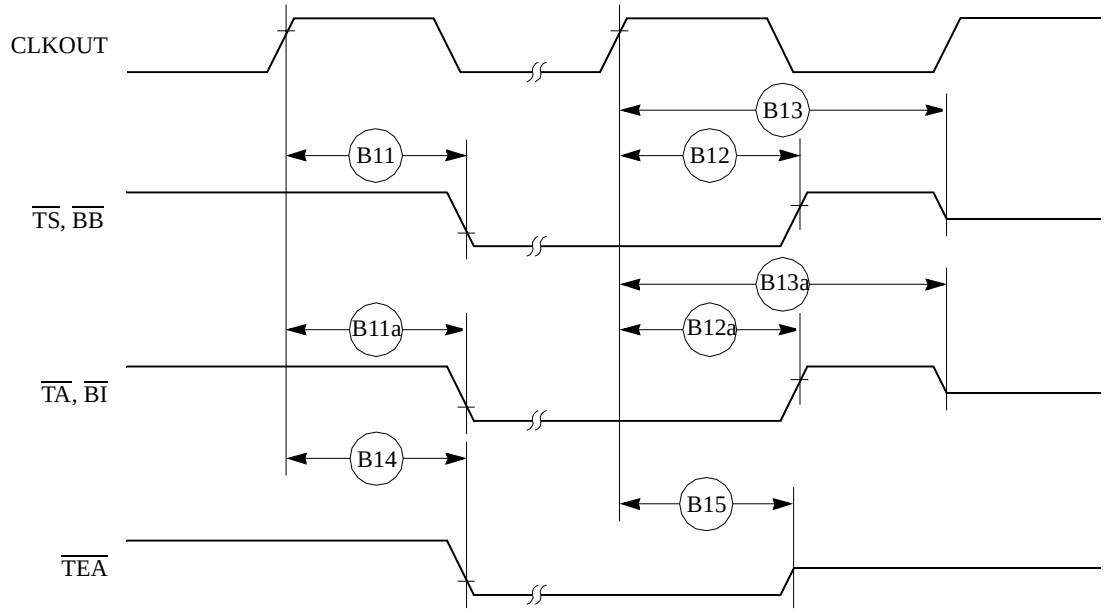

Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing

Figure 6 provides the timing for the synchronous input signals.

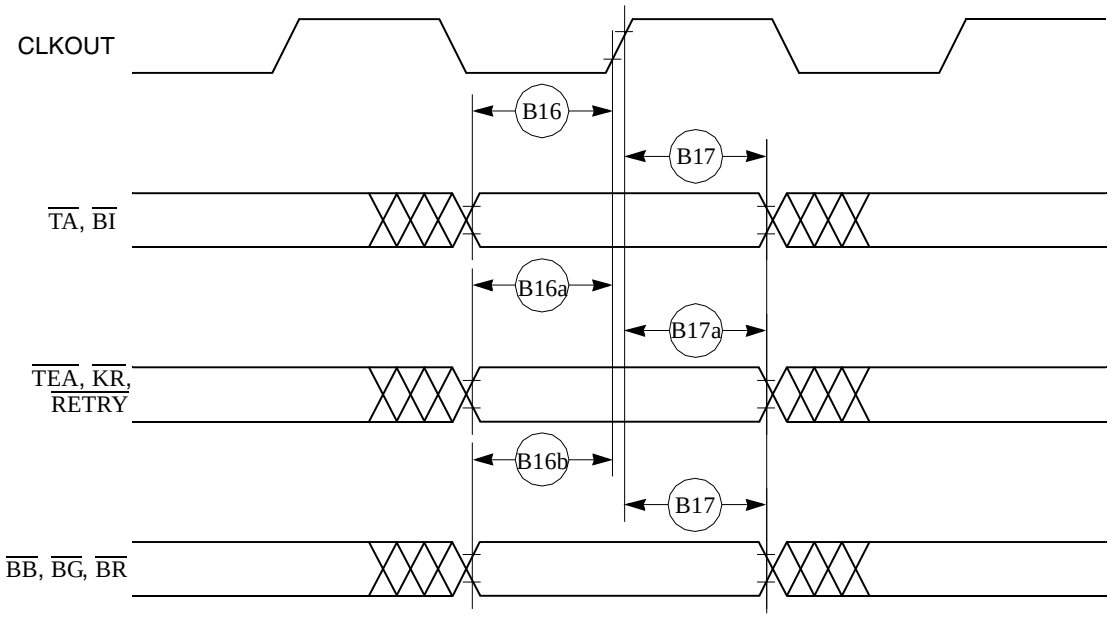

Figure 6. Synchronous Input Signals Timing

Figure 7 provides normal case timing for input data.

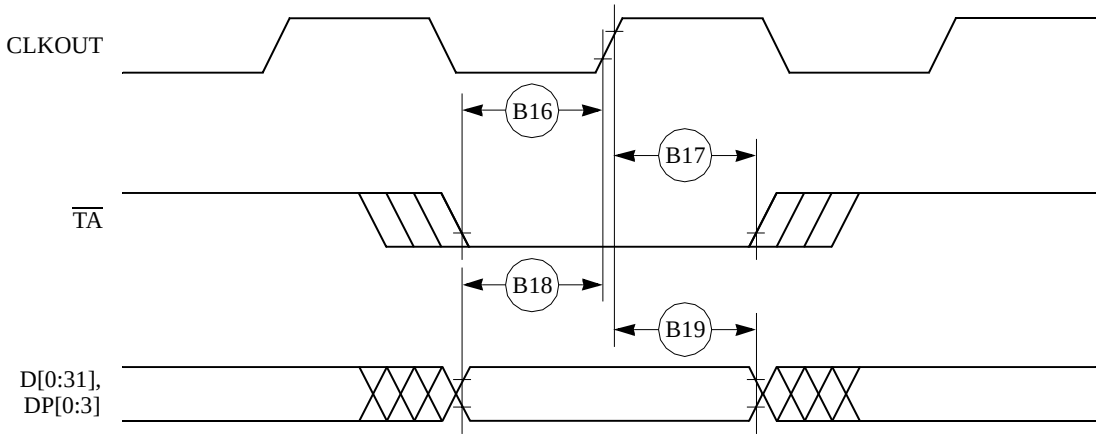

Figure 7. Input Data Timing in Normal Case

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

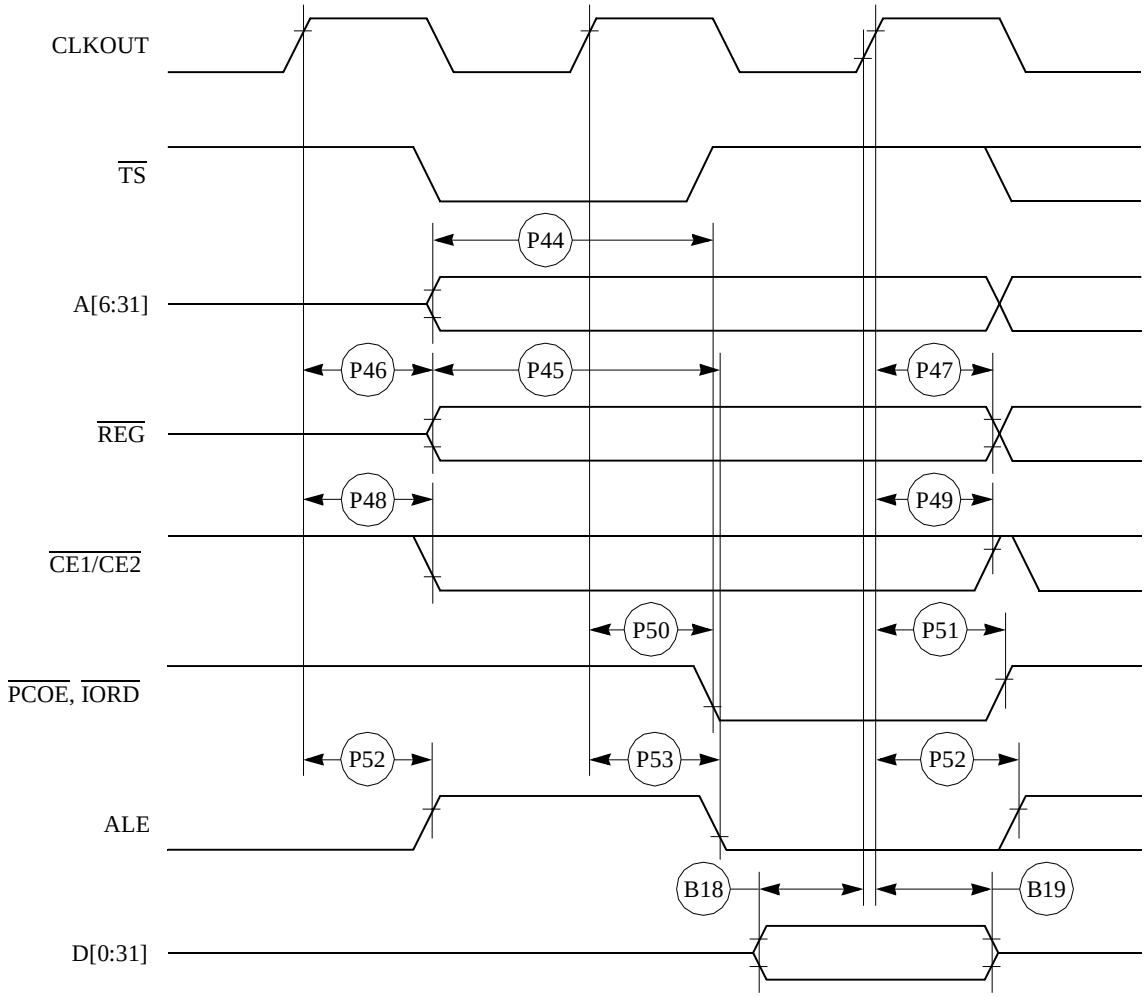

Figure 24. PCMCIA Access Cycles Timing External Bus Read

Table 11 shows the reset timing for the MPC850.

Table 11. Reset Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	340.00	—	515.00	—	425.00	—	17.000	ns
R72		—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R80	DSDI, DSCK set up	60.00	—	90.00	—	75.00	—	3.000	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns

Figure 31 shows the reset timing for the data bus configuration.

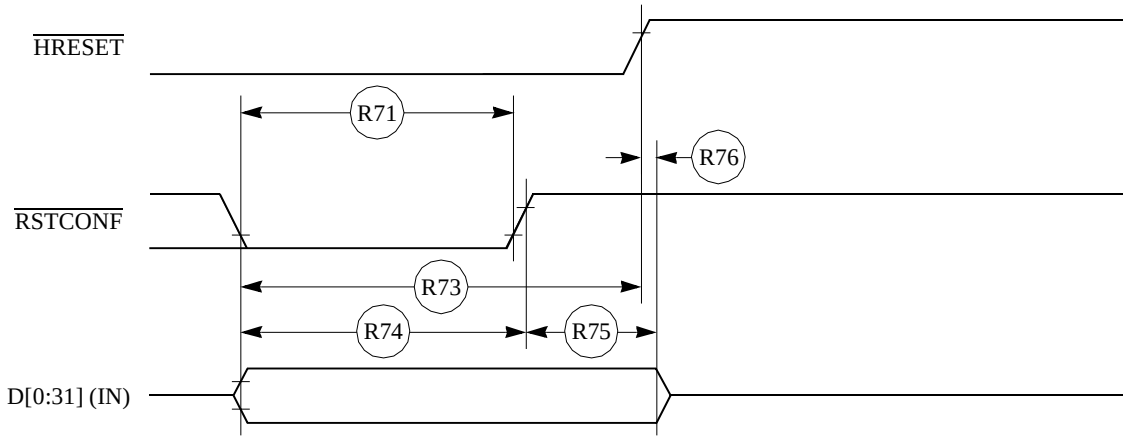

Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

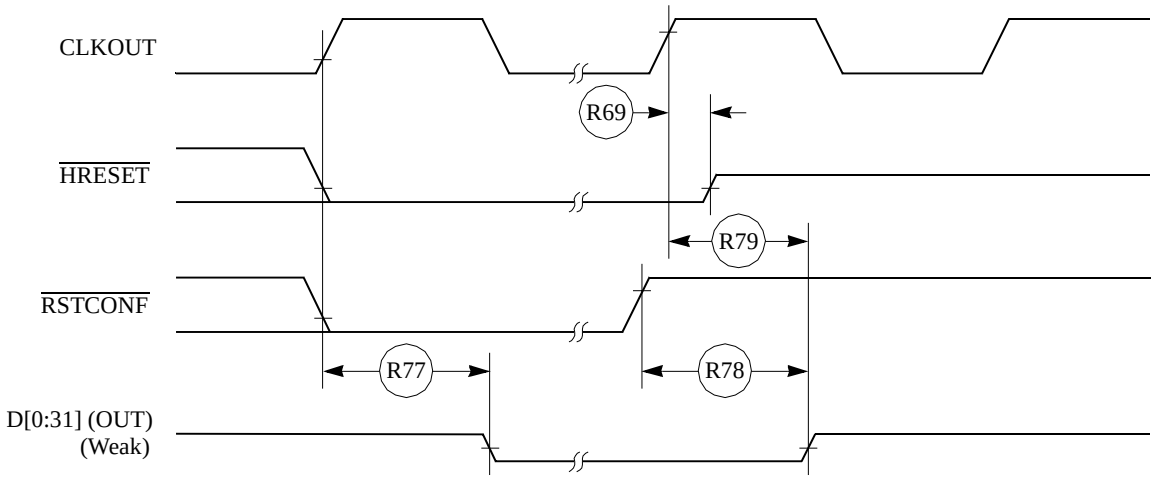

Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

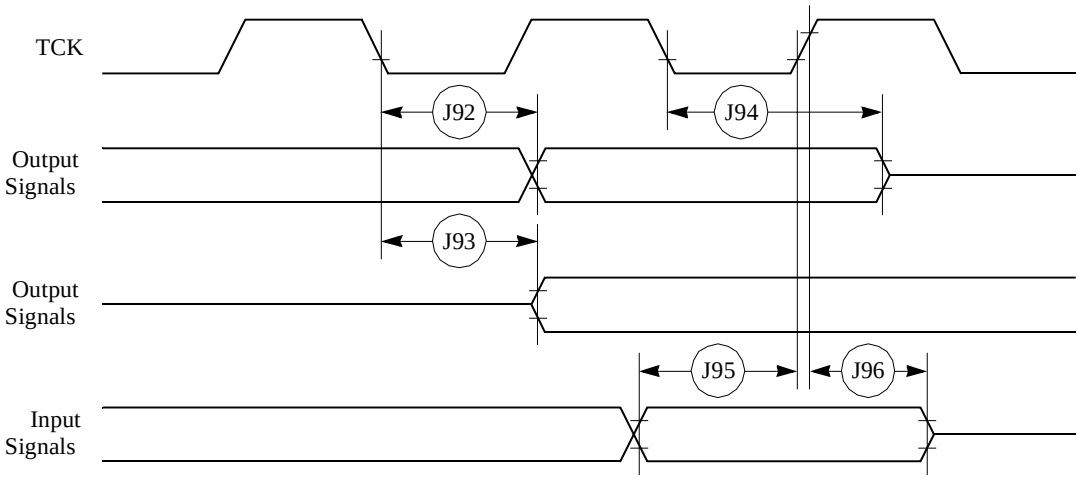

Figure 37. Boundary Scan (JTAG) Timing Diagram

8 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC850.

8.1 PIO AC Electrical Specifications

Table 13 provides the parallel I/O timings for the MPC850 as shown in Figure 38.

Table 13. Parallel I/O Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

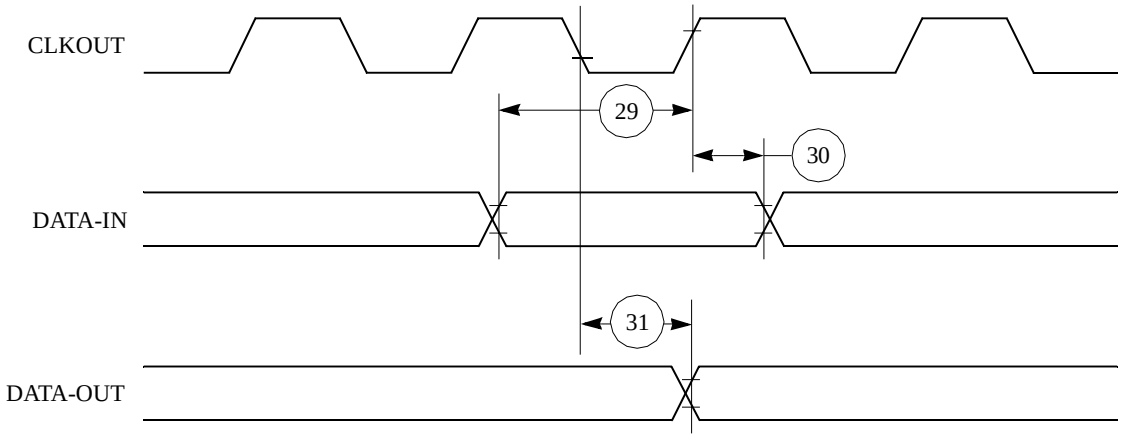

Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Table 14. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7.00	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3.00	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12.00	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12.00	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20.00	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15.00	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7.00	—	ns

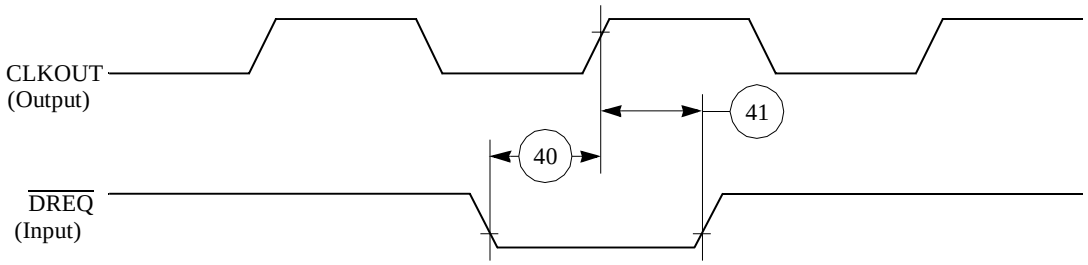

Figure 39. IDMA External Requests Timing Diagram

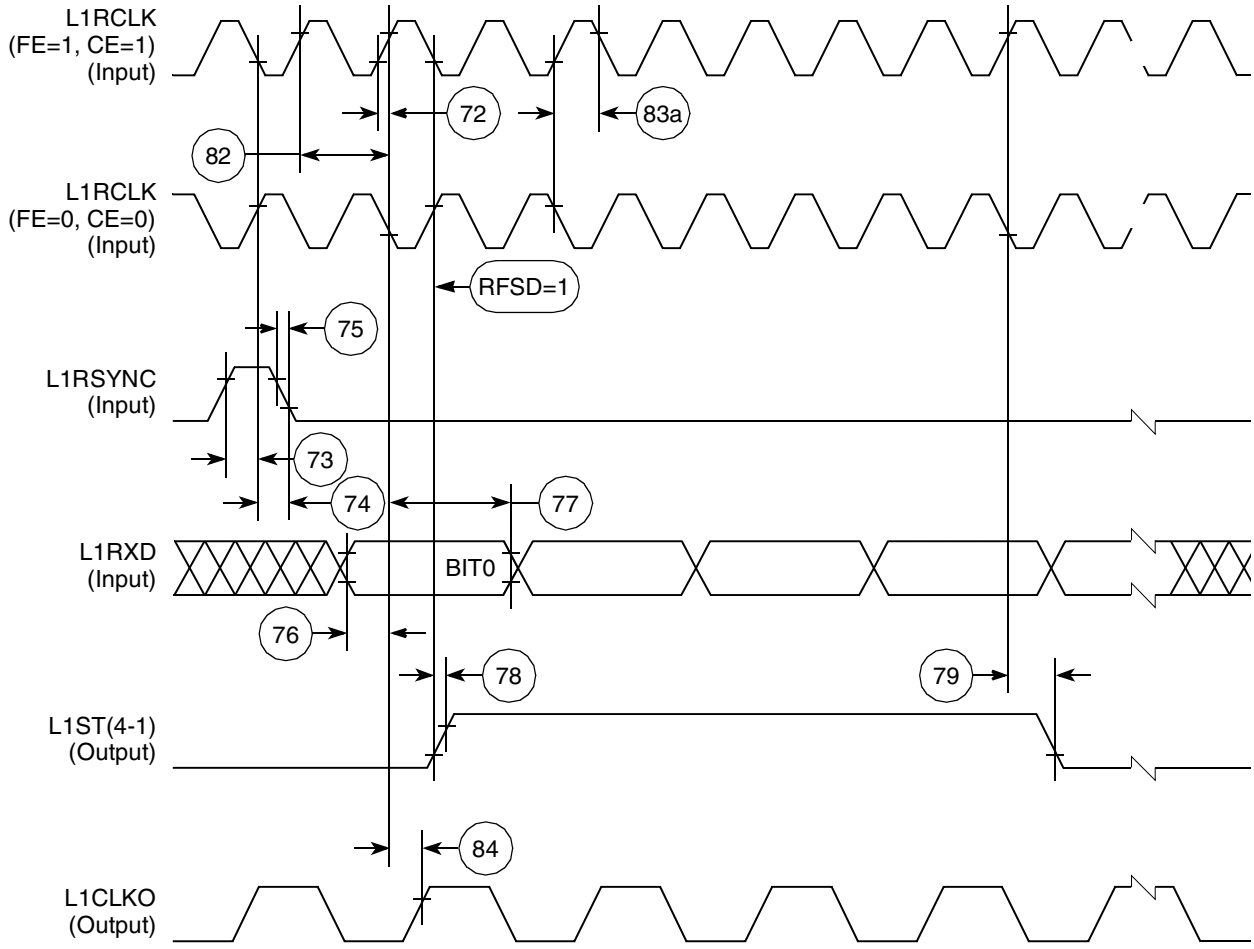

Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

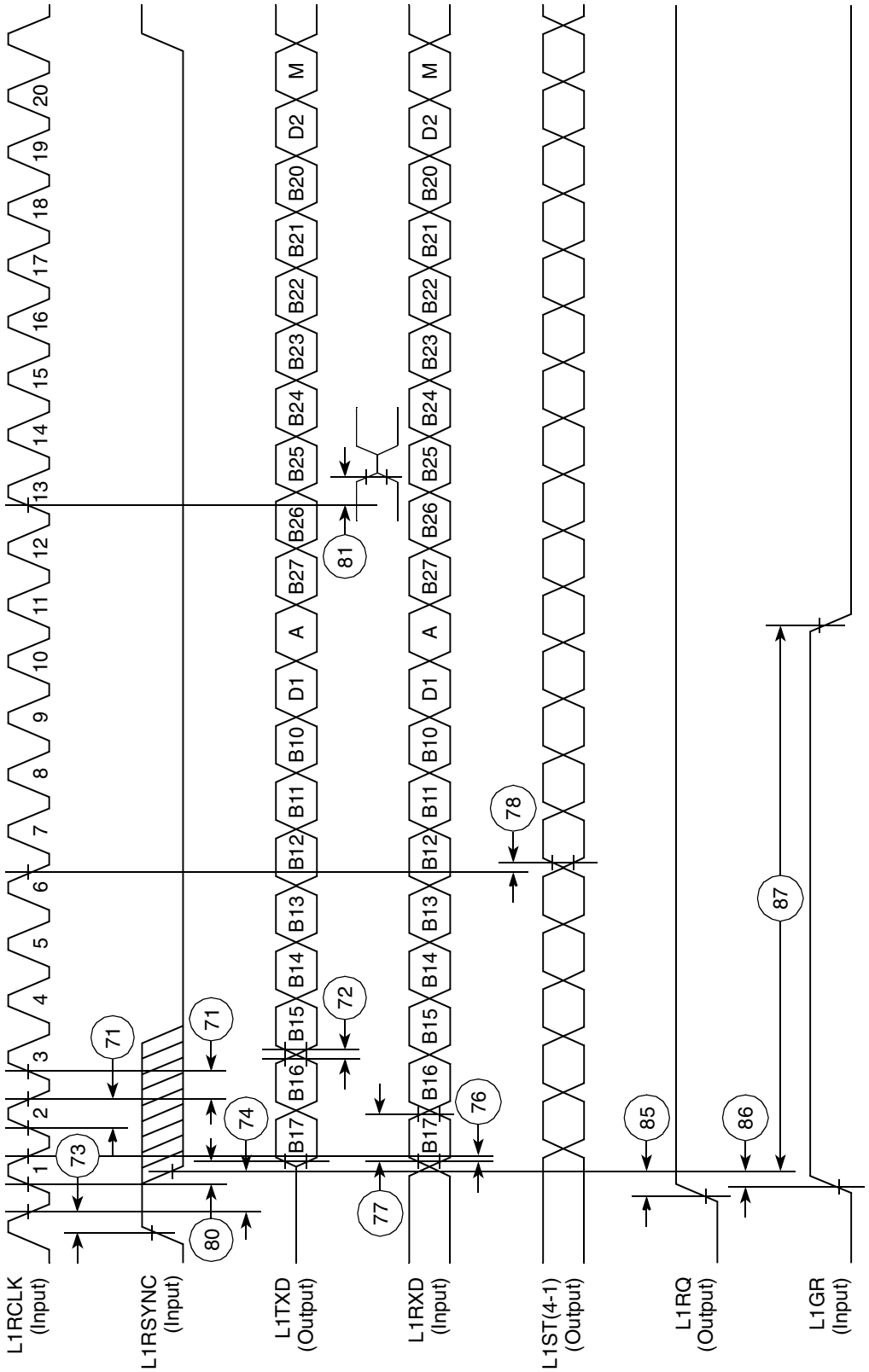

Figure 49. IDL Timing

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

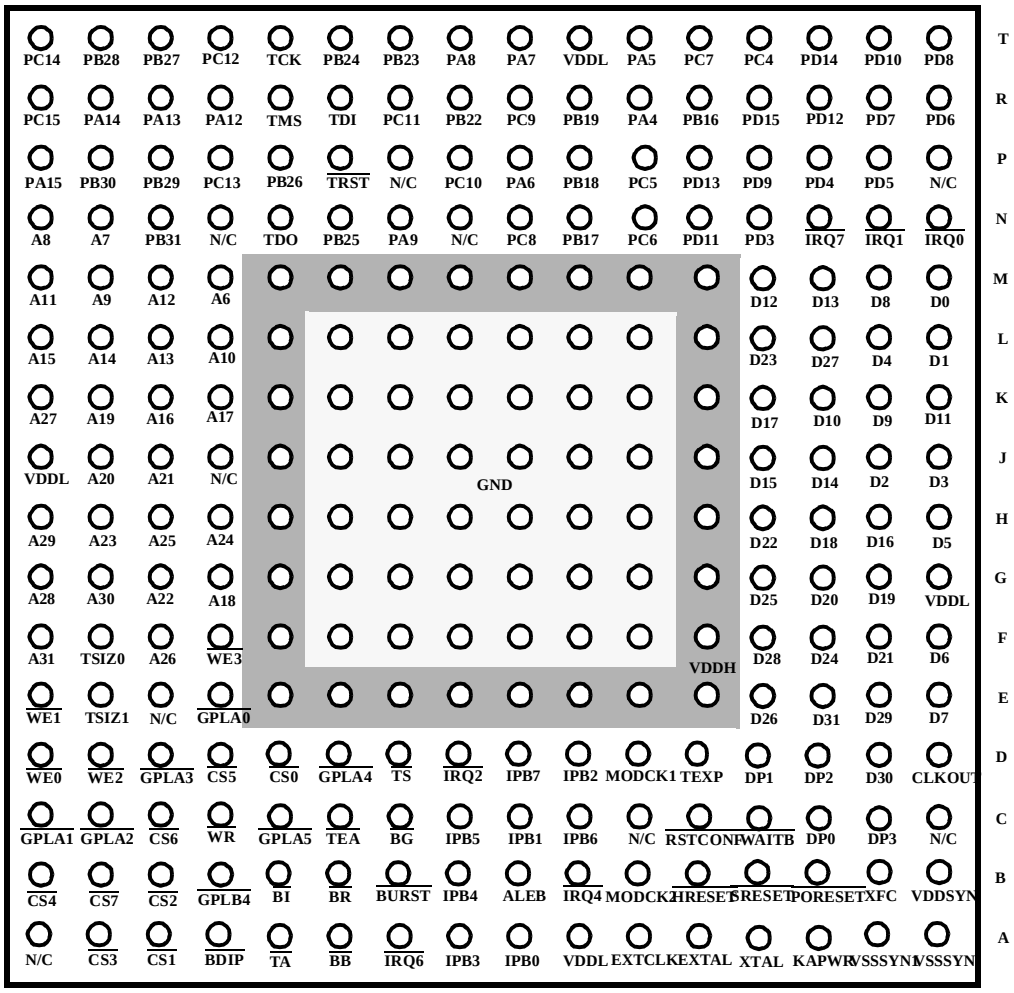

Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface.

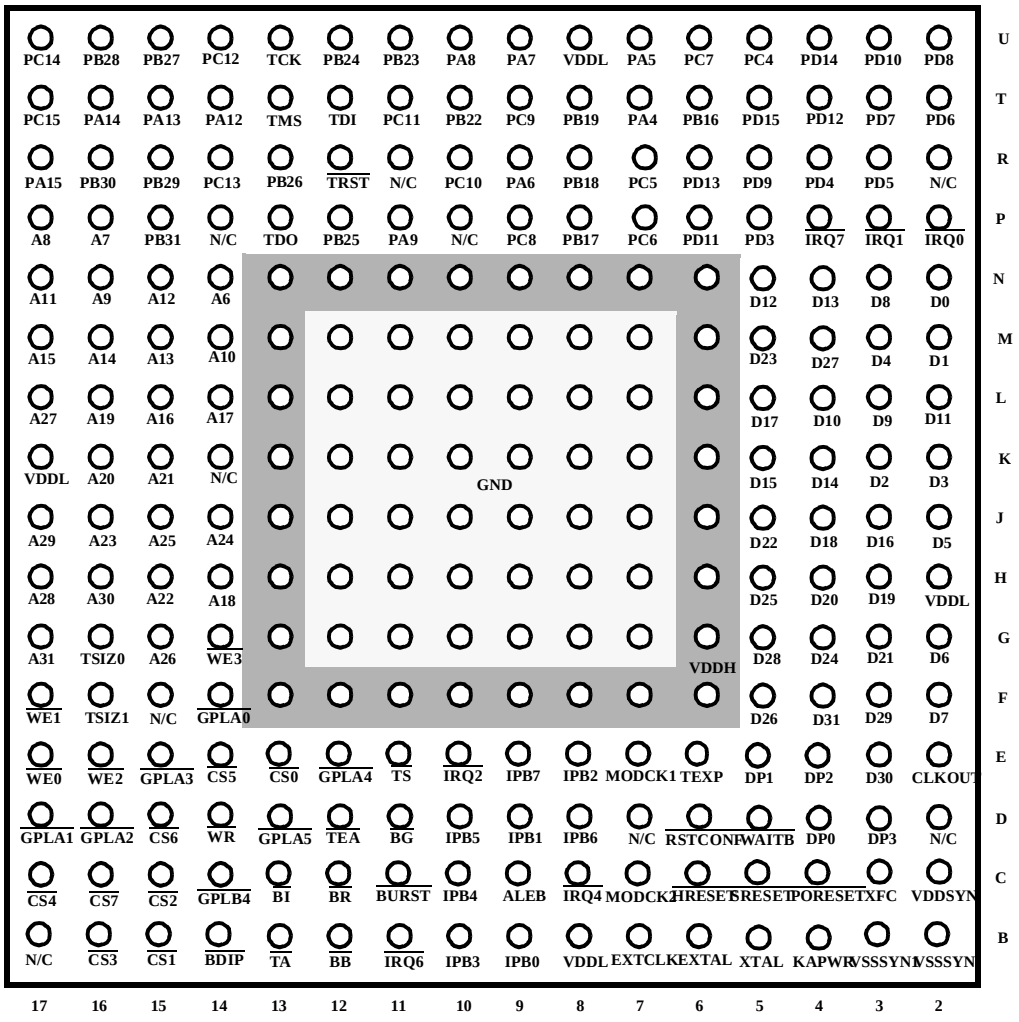

Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.