



Welcome to [E-XFL.COM](#)

### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850deczq66bu">https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850deczq66bu</a>

- Gate mode can enable/disable counting
- Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

$\theta_{JA}$  = Package thermal resistance, junction to ambient, °C/W

$$P_D = P_{INT} + P_{I/O}$$

$$P_{INT} = I_{DD} \times V_{DD}, \text{ watts—chip internal power}$$

$P_{I/O}$  = Power dissipation on input and output pins—user determined

For most applications  $P_{I/O} < 0.3 \bullet P_{INT}$  and can be neglected. If  $P_{I/O}$  is neglected, an approximate relationship between  $P_D$  and  $T_J$  is:

$$P_D = K \div (T_J + 273^\circ\text{C})(2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273^\circ\text{C}) + \theta_{JA} \bullet P_D^2(3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving equations (1) and (2) iteratively for any value of  $T_A$ .

## 5.1 Layout Practices

Each  $V_{CC}$  pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The  $V_{CC}$  power supply should be bypassed to ground using at least four 0.1  $\mu\text{F}$  by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip  $V_{CC}$  and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as  $V_{CC}$  and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the  $V_{CC}$  and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

## 6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at <http://www.mot.com/netcomm>.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

Table 6. Bus Operation Timing <sup>1</sup> (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B9	CLKOUT to A[6–31] RD/WR, BURST, D[0–31], DP[0–3], TSIZ[0–1], REG, RSV, AT[0–3], PTR high-Z	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B11	CLKOUT to $\overline{TS}$ , $\overline{BB}$ assertion	5.00	11.00	7.58	13.58	6.25	12.25	0.250	50.00	ns
B11a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ assertion, (When driven by the memory controller or PCMCIA interface)	2.50	9.25	2.50	9.25	2.50	9.25	—	50.00	ns
B12	CLKOUT to $\overline{TS}$ , $\overline{BB}$ negation	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B12a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface)	2.50	11.00	2.50	11.00	2.50	11.00	—	50.00	ns
B13	CLKOUT to $\overline{TS}$ , $\overline{BB}$ high-Z	5.00	19.00	7.58	21.58	6.25	20.25	0.250	50.00	ns
B13a	CLKOUT to $\overline{TA}$ , $\overline{BI}$ high-Z, (when driven by the memory controller or PCMCIA interface)	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion	2.50	10.00	2.50	10.00	2.50	10.00	—	50.00	ns
B15	CLKOUT to $\overline{TEA}$ high-Z	2.50	15.00	2.50	15.00	2.50	15.00	—	50.00	ns
B16	$\overline{TA}$ , $\overline{BI}$ valid to CLKOUT (setup time) <sup>5</sup>	9.75	—	9.75	—	9.75	—	—	50.00	ns
B16a	$\overline{TEA}$ , $\overline{KR}$ , $\overline{RETRY}$ , valid to CLKOUT (setup time) <sup>5</sup>	10.00	—	10.00	—	10.00	—	—	50.00	ns
B16b	$\overline{BB}$ , $\overline{BG}$ , $\overline{BR}$ valid to CLKOUT (setup time) <sup>6</sup>	8.50	—	8.50	—	8.50	—	—	50.00	ns
B17	CLKOUT to $\overline{TA}$ , $\overline{TEA}$ , $\overline{BI}$ , $\overline{BB}$ , $\overline{BG}$ , $\overline{BR}$ valid (Hold time). <sup>5</sup>	1.00	—	1.00	—	1.00	—	—	50.00	ns
B17a	CLKOUT to $\overline{KR}$ , $\overline{RETRY}$ , except $\overline{TEA}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B18	D[0–31], DP[0–3] valid to CLKOUT rising edge (setup time) <sup>7</sup>	6.00	—	6.00	—	6.00	—	—	50.00	ns
B19	CLKOUT rising edge to D[0–31], DP[0–3] valid (hold time) <sup>7</sup>	1.00	—	1.00	—	1.00	—	—	50.00	ns
B20	D[0–31], DP[0–3] valid to CLKOUT falling edge (setup time) <sup>8</sup>	4.00	—	4.00	—	4.00	—	—	50.00	ns
B21	CLKOUT falling edge to D[0–31], DP[0–3] valid (hold time) <sup>8</sup>	2.00	—	2.00	—	2.00	—	—	—	—

Table 6. Bus Operation Timing <sup>1</sup> (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0,1	—	8.00	—	8.00	—	8.00	—	50.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	—	50.00	ns
B24	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0.	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B24a	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B25	CLKOUT rising edge to $\overline{OE}$ , WE[0–3] asserted	—	9.00	—	9.00	—	9.00	—	50.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	—	50.00	ns
B27	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	23.00	—	36.00	—	29.00	—	1.250	50.00	ns
B27a	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B28	CLKOUT rising edge to WE[0–3] negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	50.00	ns
B28a	CLKOUT falling edge to WE[0–3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	—	12.00	—	14.00	—	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing <sup>1</sup> (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B33	CLKOUT falling edge to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns

Figure 6 provides the timing for the synchronous input signals.

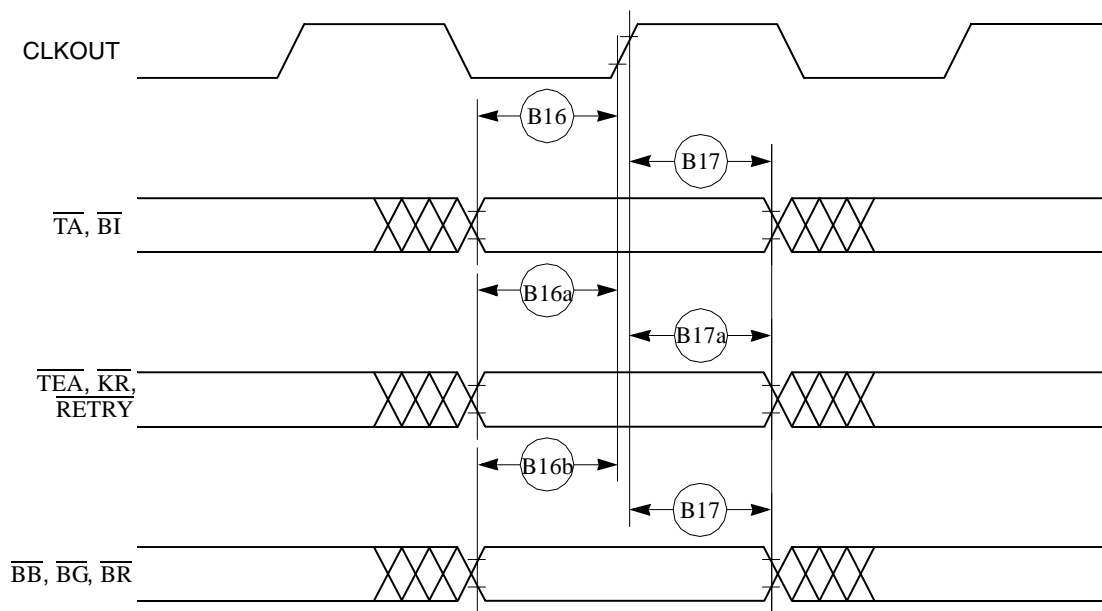


Figure 6. Synchronous Input Signals Timing

Figure 7 provides normal case timing for input data.

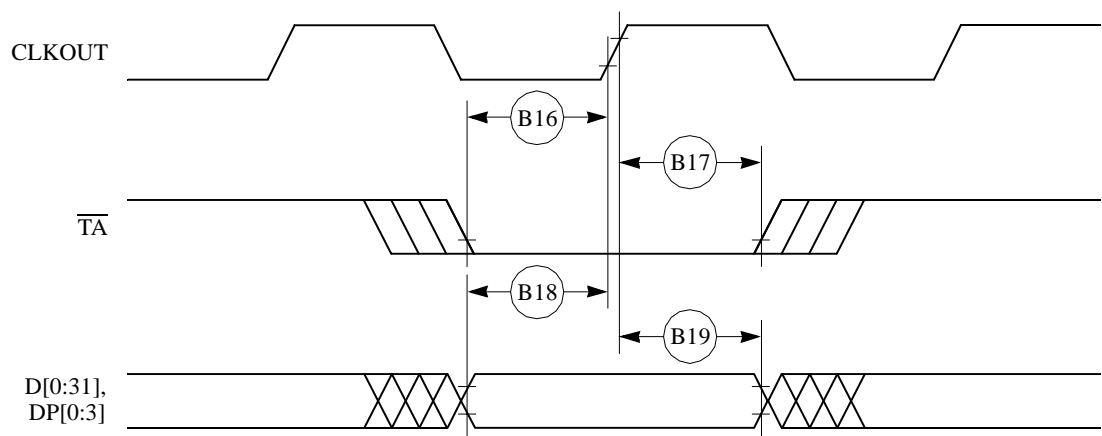
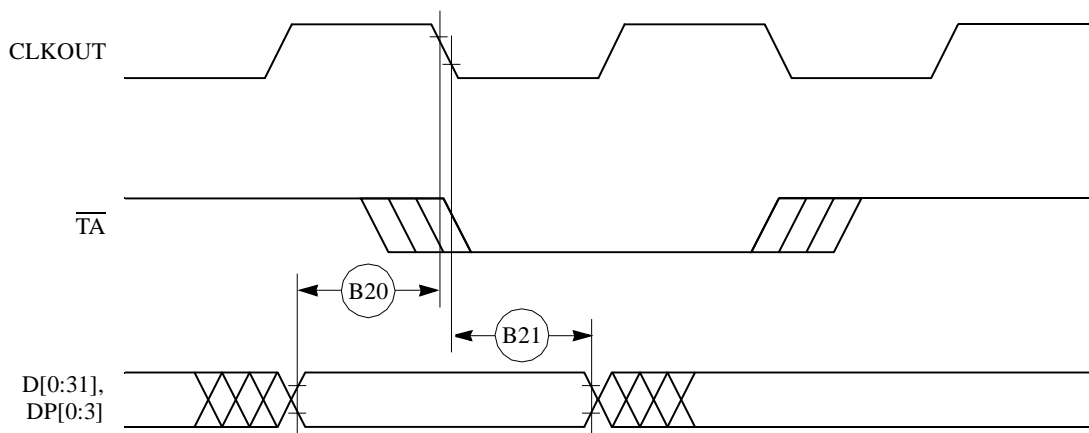


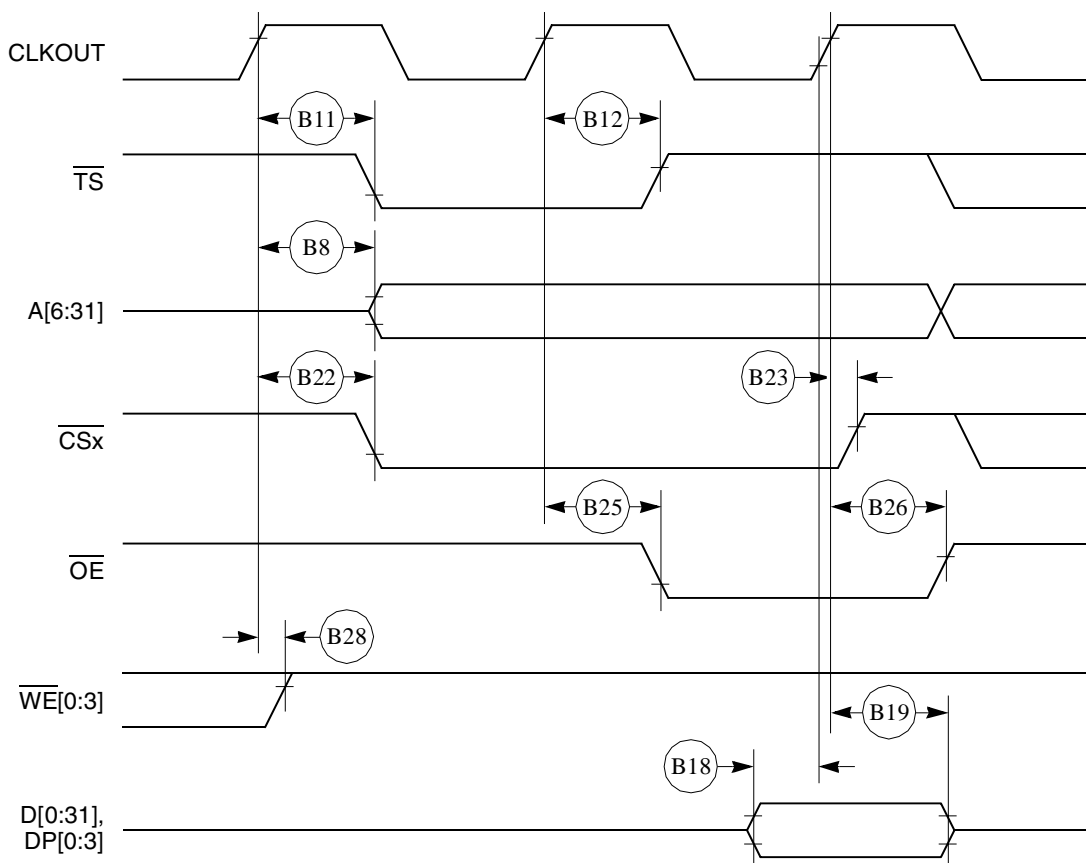
Figure 7. Input Data Timing in Normal Case

Figure 8 provides the timing for the input data controlled by the UPM in the memory controller.



**Figure 8. Input Data Timing when Controlled by UPM in the Memory Controller**

Figure 9 through Figure 12 provide the timing for the external bus read controlled by various GPCM factors.



**Figure 9. External Bus Read Timing (GPCM Controlled—ACS = 00)**



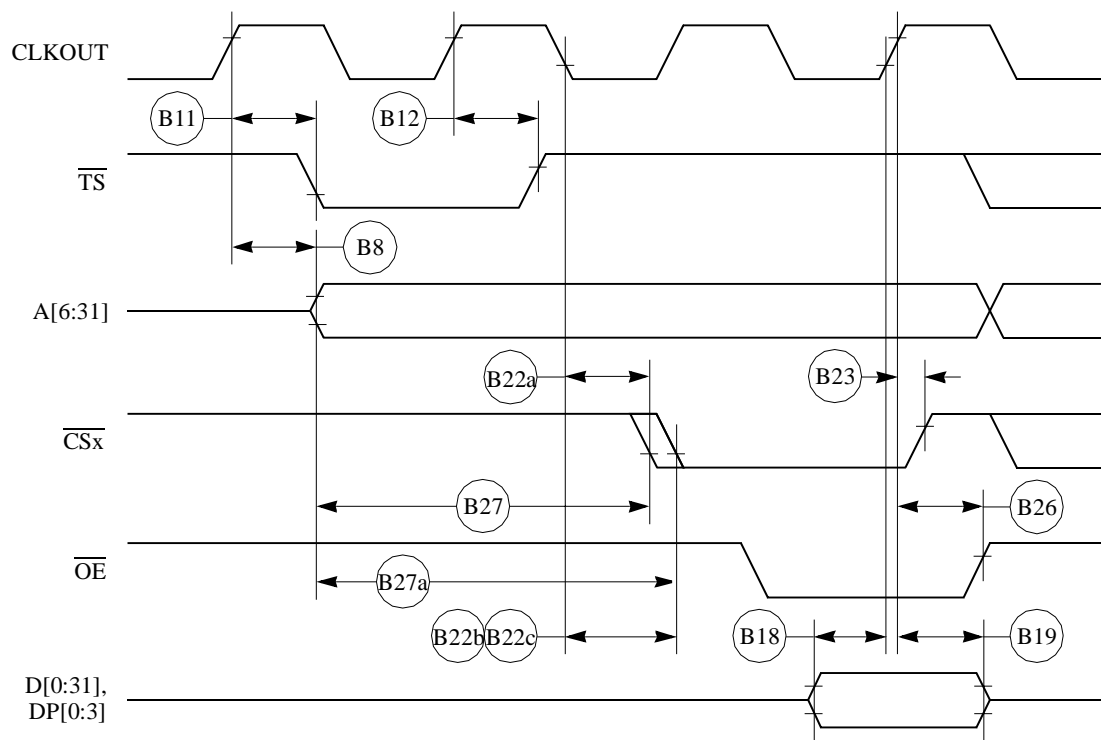


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

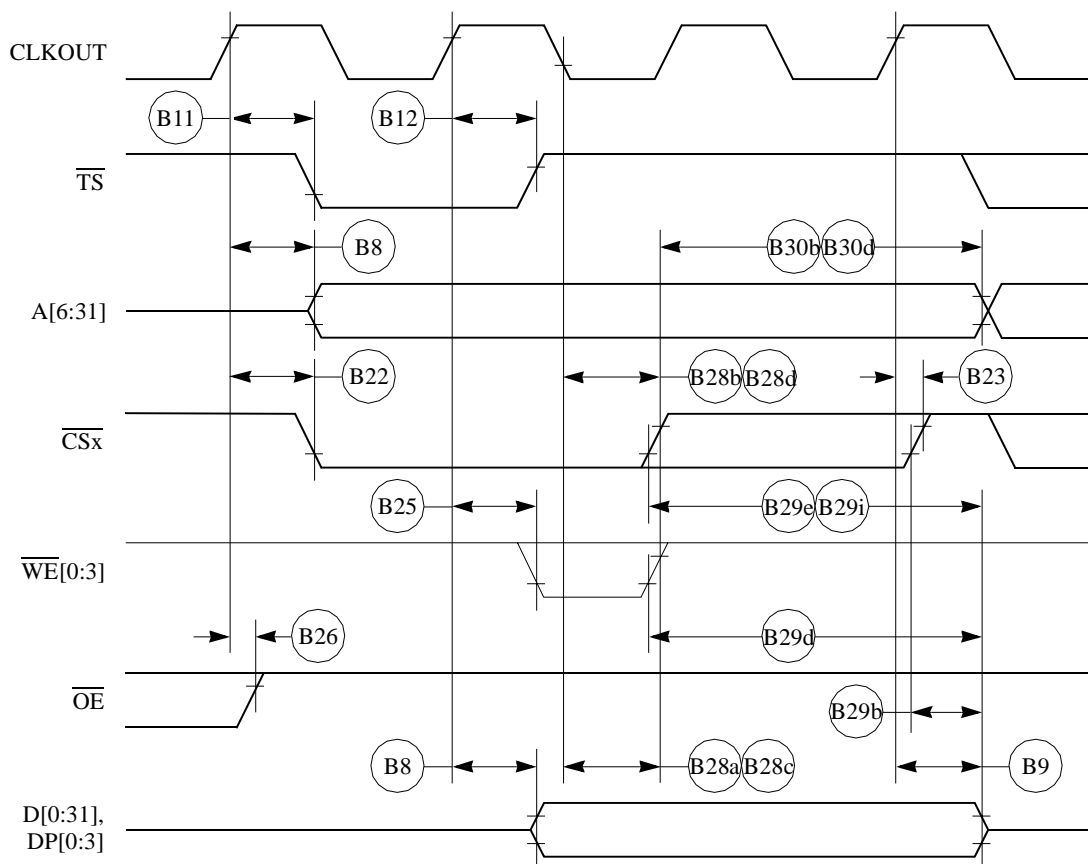


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

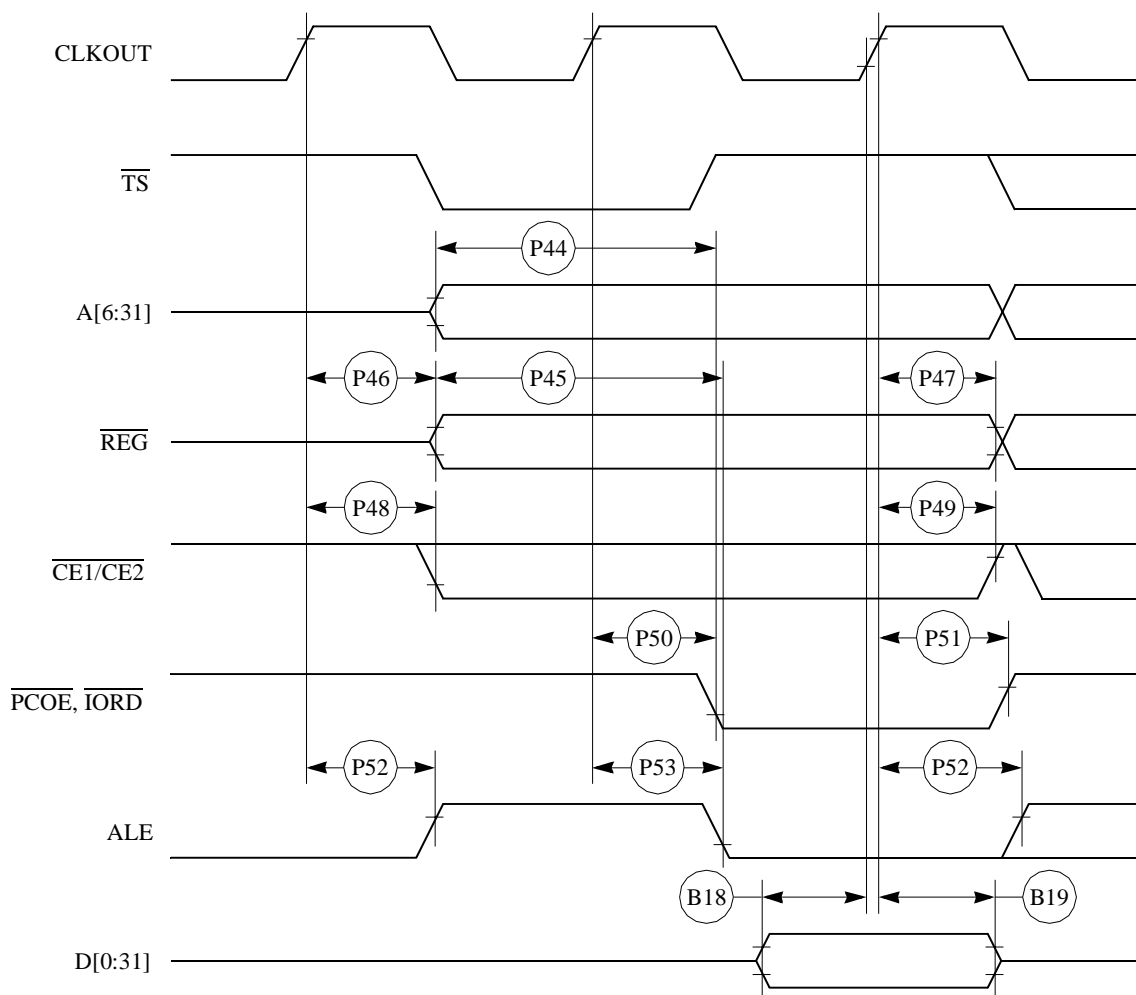


Figure 24. PCMCIA Access Cycles Timing External Bus Read

Table 11 shows the reset timing for the MPC850.

**Table 11. Reset Timing**

Num	Characteristic	50 MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	340.00	—	515.00	—	425.00	—	17.000	ns
R72		—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R80	DSDI, DSCK set up	60.00	—	90.00	—	75.00	—	3.000	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns

Figure 31 shows the reset timing for the data bus configuration.

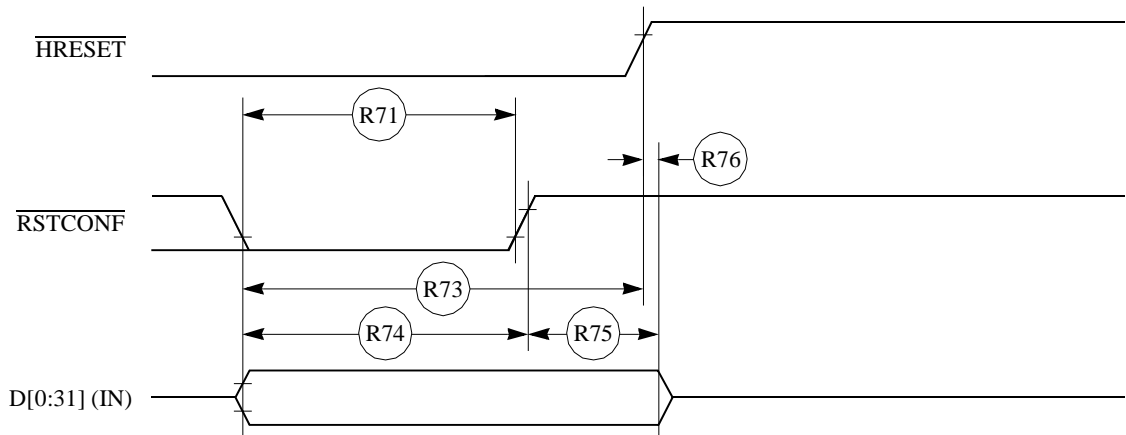


Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

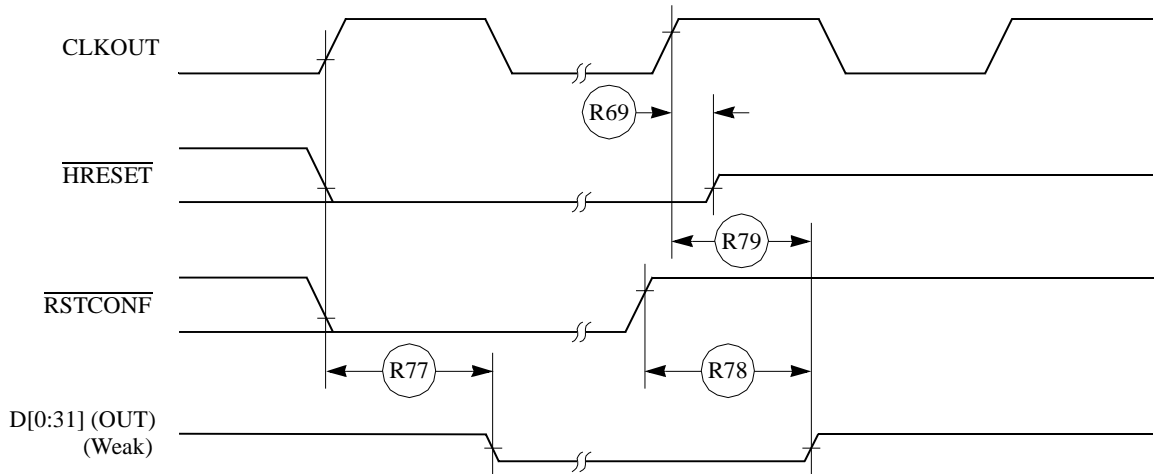


Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

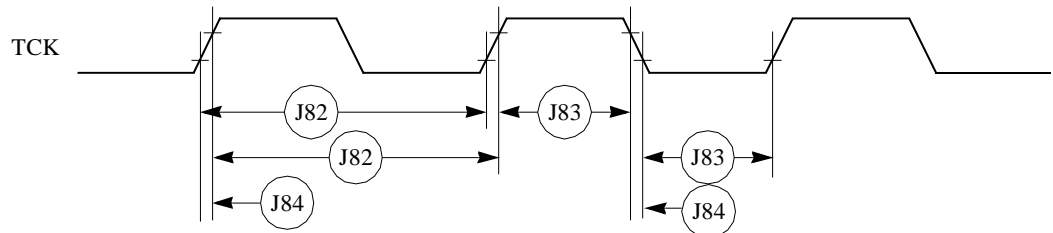


Figure 34. JTAG Test Clock Input Timing

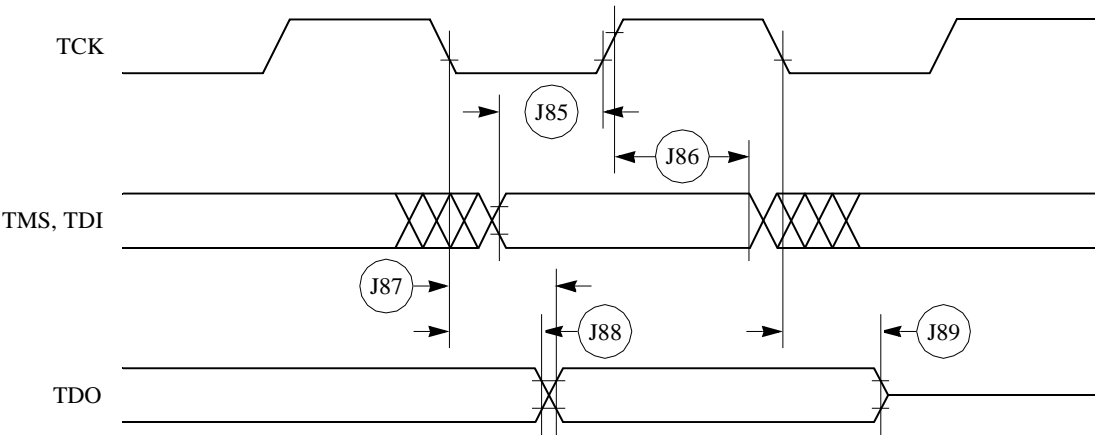


Figure 35. JTAG Test Access Port Timing Diagram

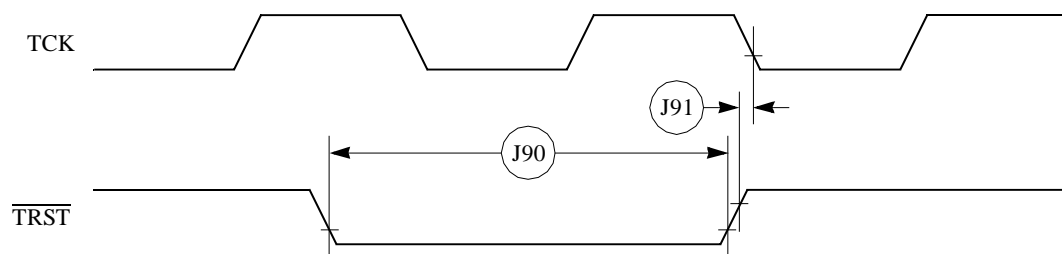


Figure 36. JTAG  $\overline{\text{TRST}}$  Timing Diagram

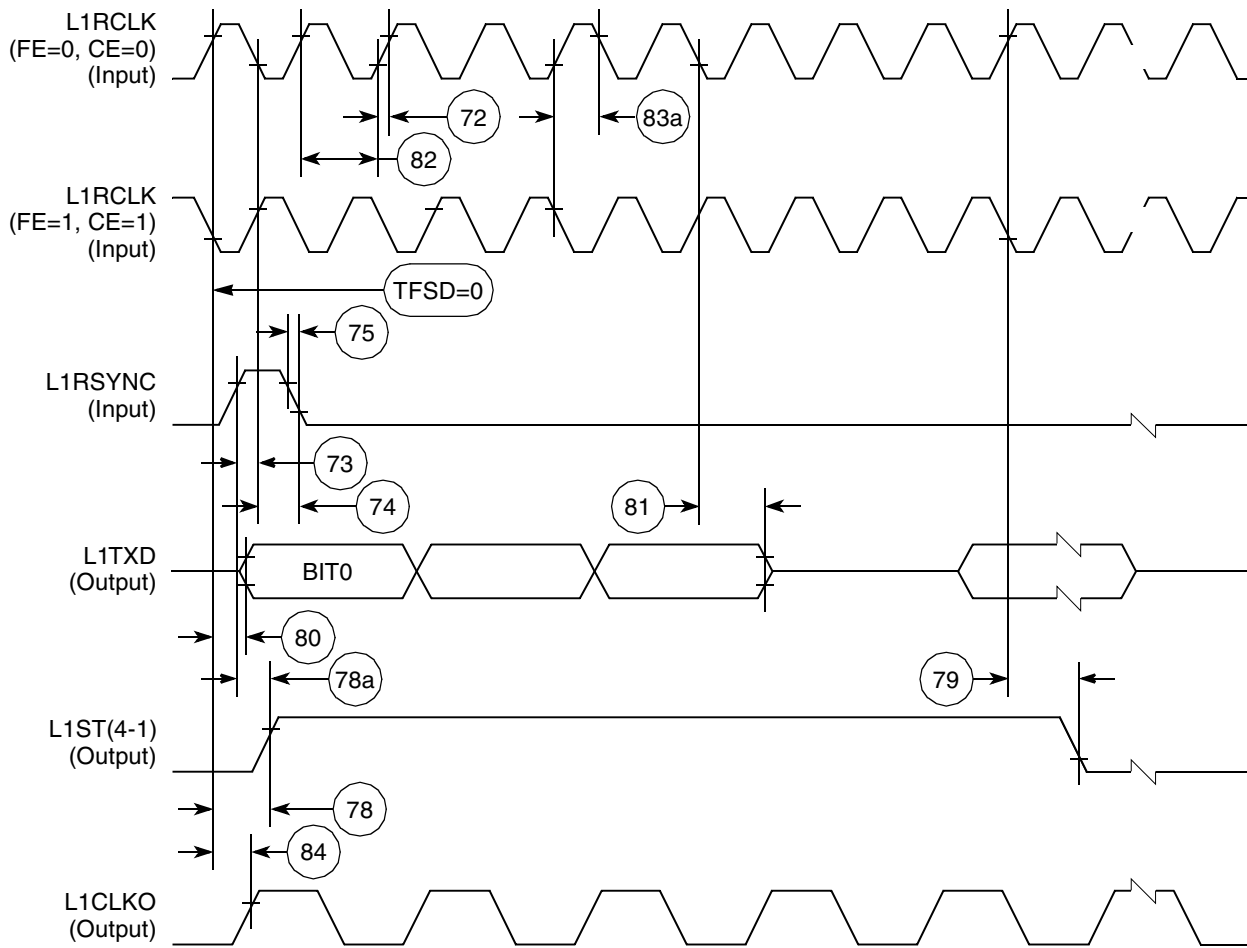


Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)

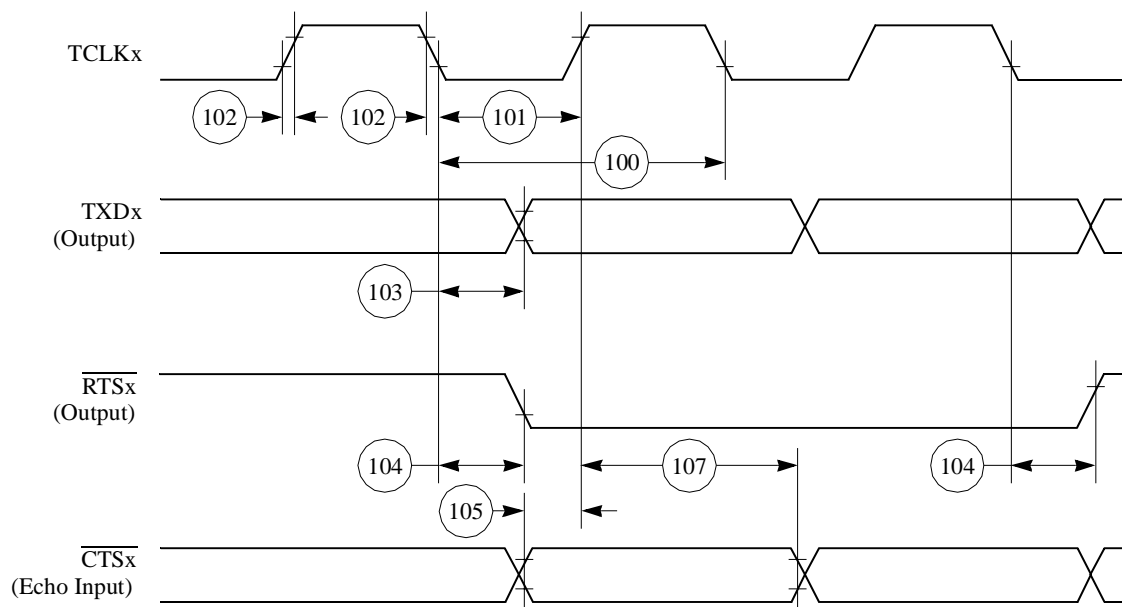


Figure 52. HDLC Bus Timing Diagram

## 8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period <sup>1</sup>	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period <sup>1</sup>	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns



Table 20. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to $\overline{\text{SDACK}}$ asserted <sup>2</sup>	—	20.00	ns
139	CLKOUT low to $\overline{\text{SDACK}}$ negated <sup>2</sup>	—	20.00	ns

<sup>1</sup> The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

<sup>2</sup>  $\overline{\text{SDACK}}$  is asserted whenever the SDMA writes the incoming frame destination address into memory.

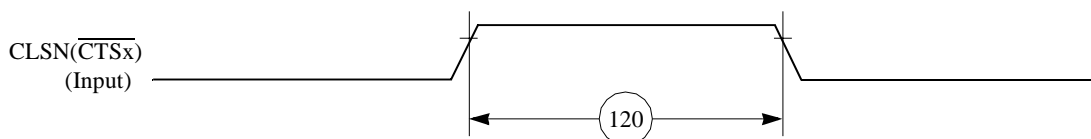


Figure 53. Ethernet Collision Timing Diagram

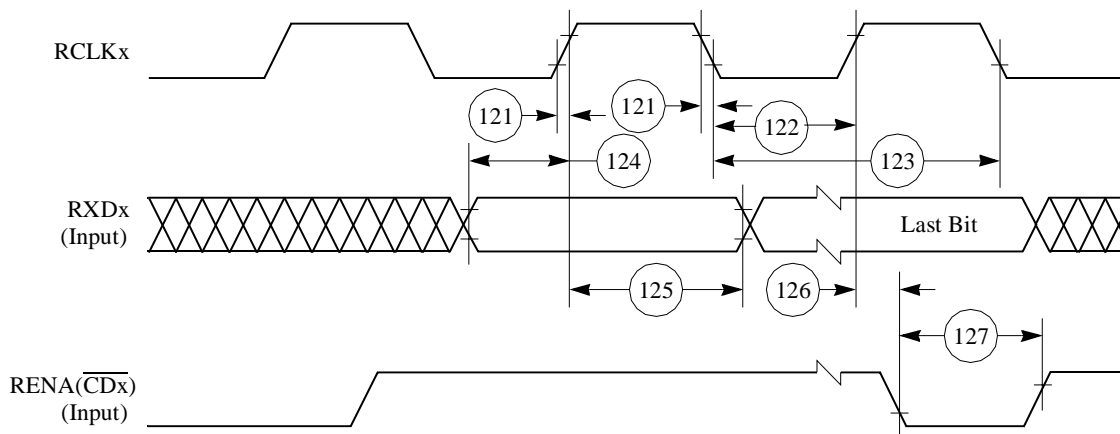


Figure 54. Ethernet Receive Timing Diagram

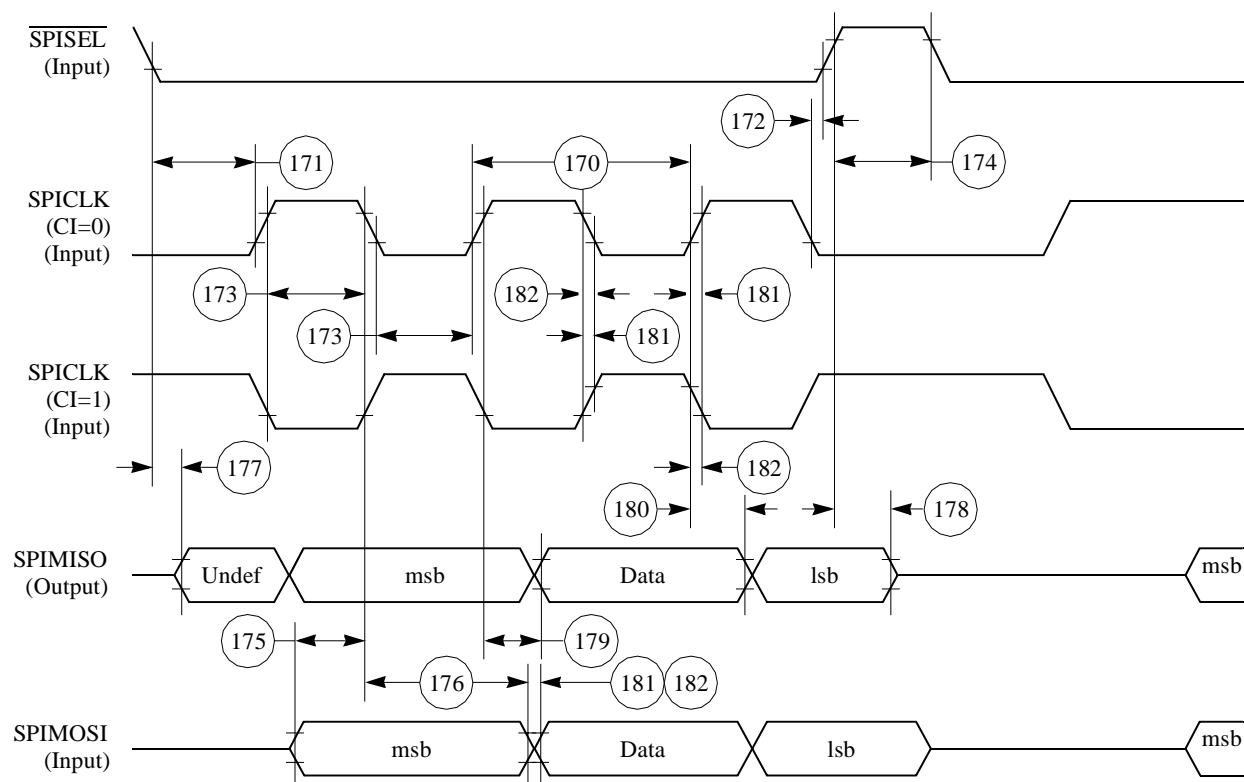


Figure 60. SPI Slave (CP = 1) Timing Diagram

## 8.11 I<sup>2</sup>C AC Electrical Specifications

Table 24 provides the I<sup>2</sup>C (SCL < 100 KHz) timings.

Table 24. I<sup>2</sup>C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) <sup>1</sup>	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	—	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	—	ns
209	SDL/SCL rise time	—	1.00	μs

## 9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

**Table 26. MPC850 Family Derivatives**

Device	Ethernet Support	Number of SCCs <sup>1</sup>	32-Channel HDLC Support	64-Channel HDLC Support <sup>2</sup>
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

<sup>1</sup> Serial Communication Controller (SCC)

<sup>2</sup> 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

**Table 27. MPC850 Package/Frequency/Availability**

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

### 9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

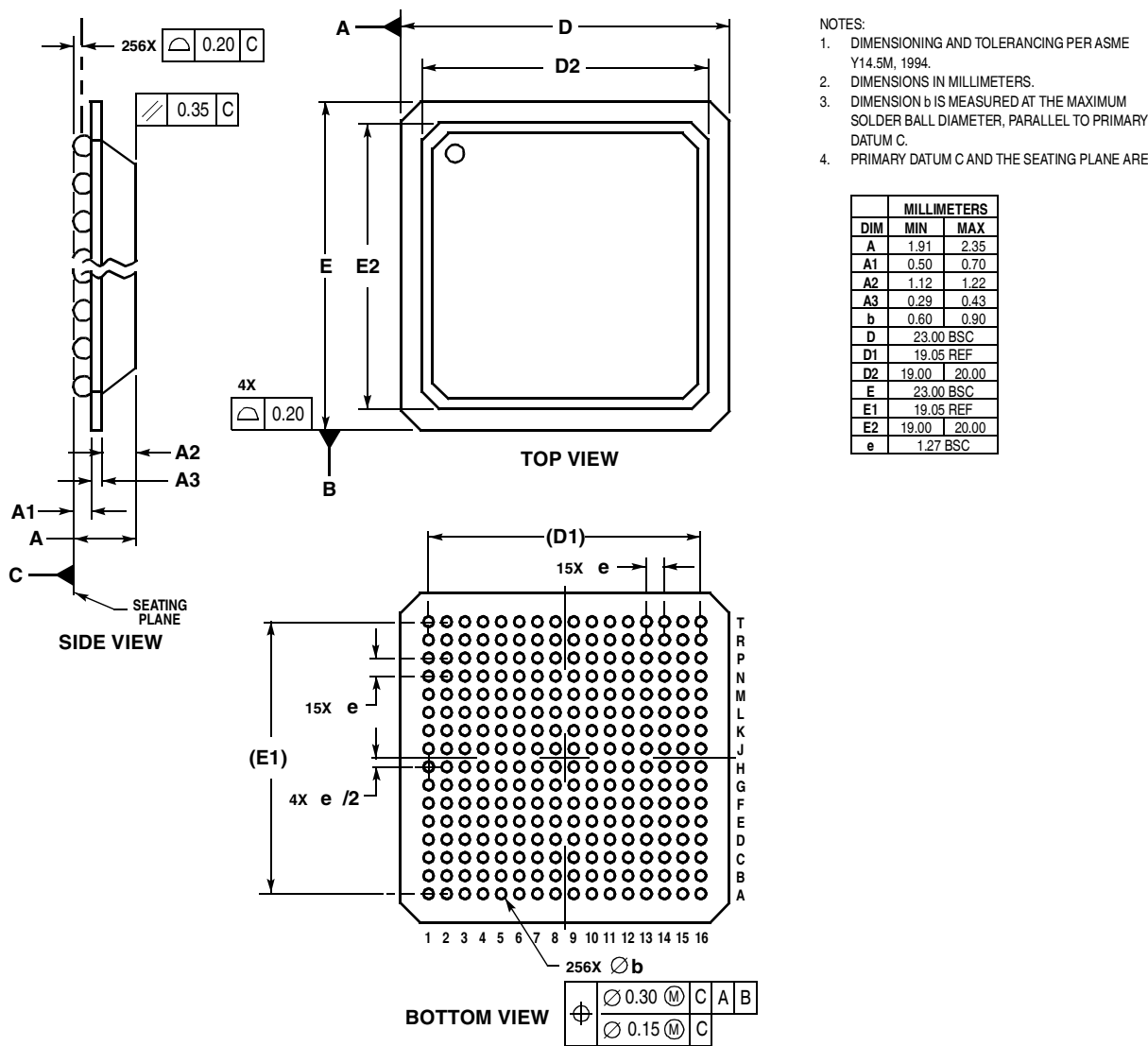


Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard

**THIS PAGE INTENTIONALLY LEFT BLANK**