



Welcome to [E-XFL.COM](#)

### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850devr50bur2">https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850devr50bur2</a>

Table 6. Bus Operation Timing <sup>1</sup> (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACTOR	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	TBD	—	—	50.00	ns

<sup>1</sup> The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{\text{FFACTOR} \times 1000}{F} + (D_{50} - 20 \times \text{FFACTOR})$$

For maxima:

$$D = \frac{\text{FFACTOR} \times 1000}{F} + (D_{50} - 20 \times \text{FFACTOR}) + 1\text{ns}(\text{CAP LOAD} - 50) / 10$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

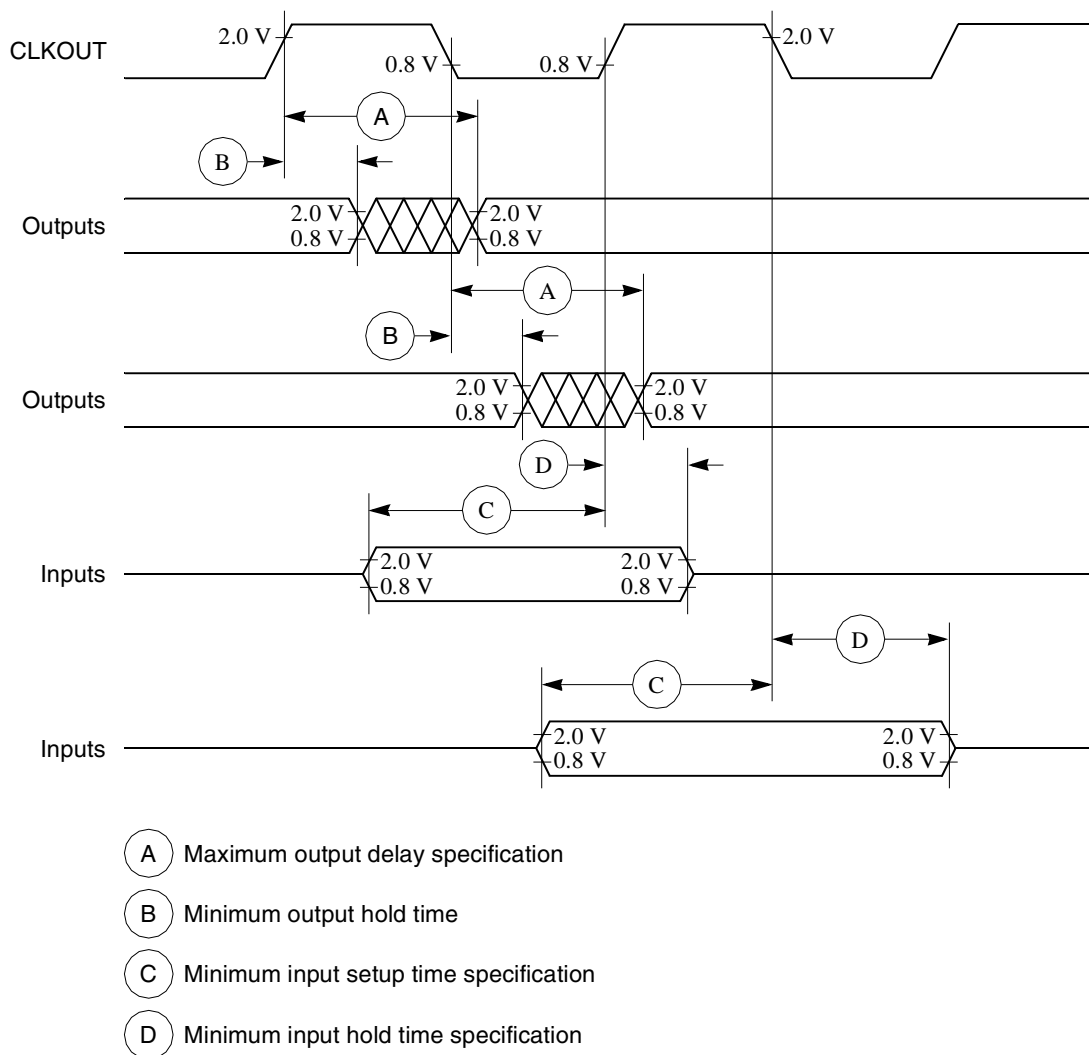
D<sub>50</sub> is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

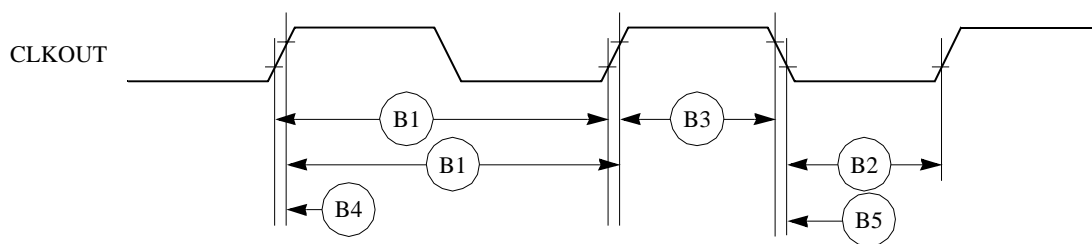
- <sup>2</sup> Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.
- <sup>3</sup> If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.
- <sup>4</sup> The timing for  $\overline{BR}$  output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for  $\overline{BG}$  output is relevant when the MPC850 is selected to work with internal bus arbiter.
- <sup>5</sup> The setup times required for  $\overline{TA}$ ,  $\overline{TEA}$ , and  $\overline{BI}$  are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).
- <sup>6</sup> The timing required for  $\overline{BR}$  input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for  $\overline{BG}$  input is relevant when the MPC850 is selected to work with the external bus arbiter.
- <sup>7</sup> The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the  $\overline{TA}$  input signal is asserted.
- <sup>8</sup> The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.
- <sup>9</sup> The timing B30 refers to  $\overline{CS}$  when ACS = '00' and to  $\overline{WE}[0:3]$  when CSNT = '0'.
- <sup>10</sup> The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.
- <sup>11</sup> The  $\overline{AS}$  signal is considered asynchronous to CLKOUT.

Figure 2 is the control timing diagram.



**Figure 2. Control Timing**

Figure 3 provides the timing for the external clock.



**Figure 3. External Clock Timing**

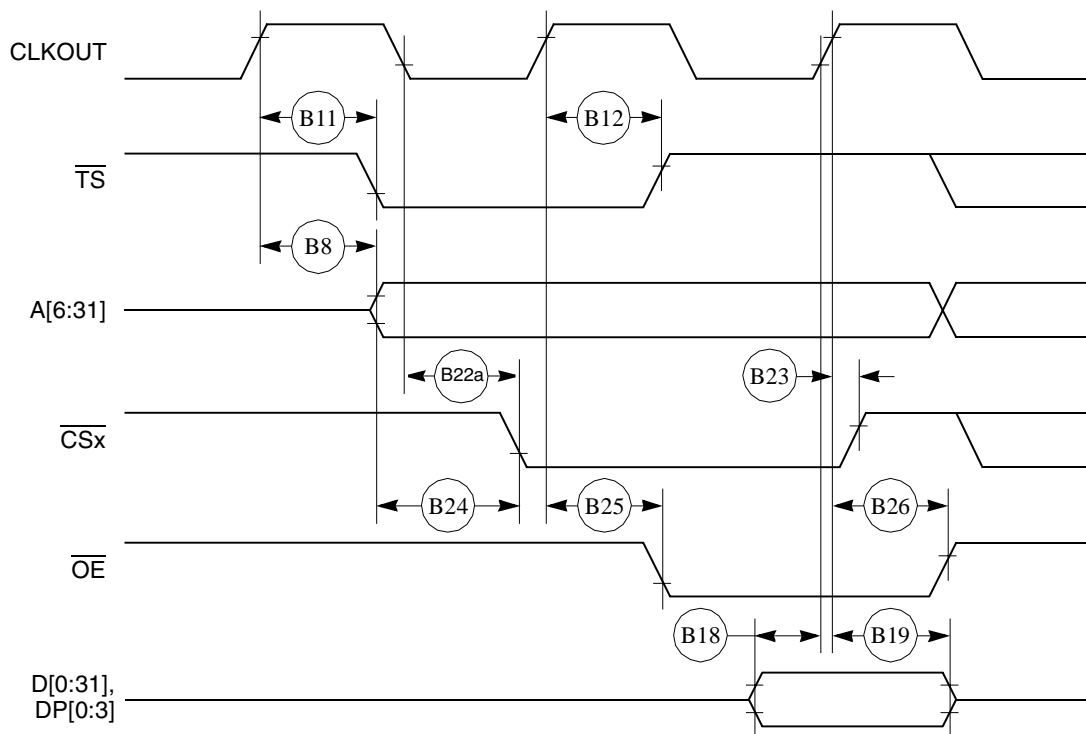


Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

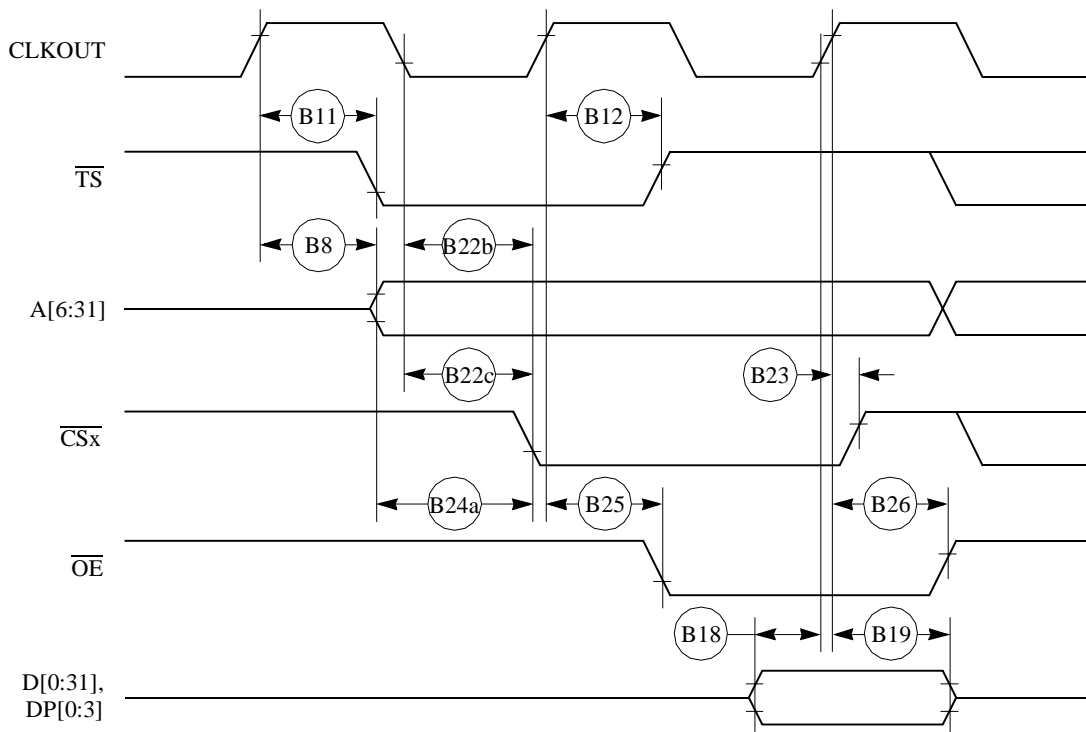


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

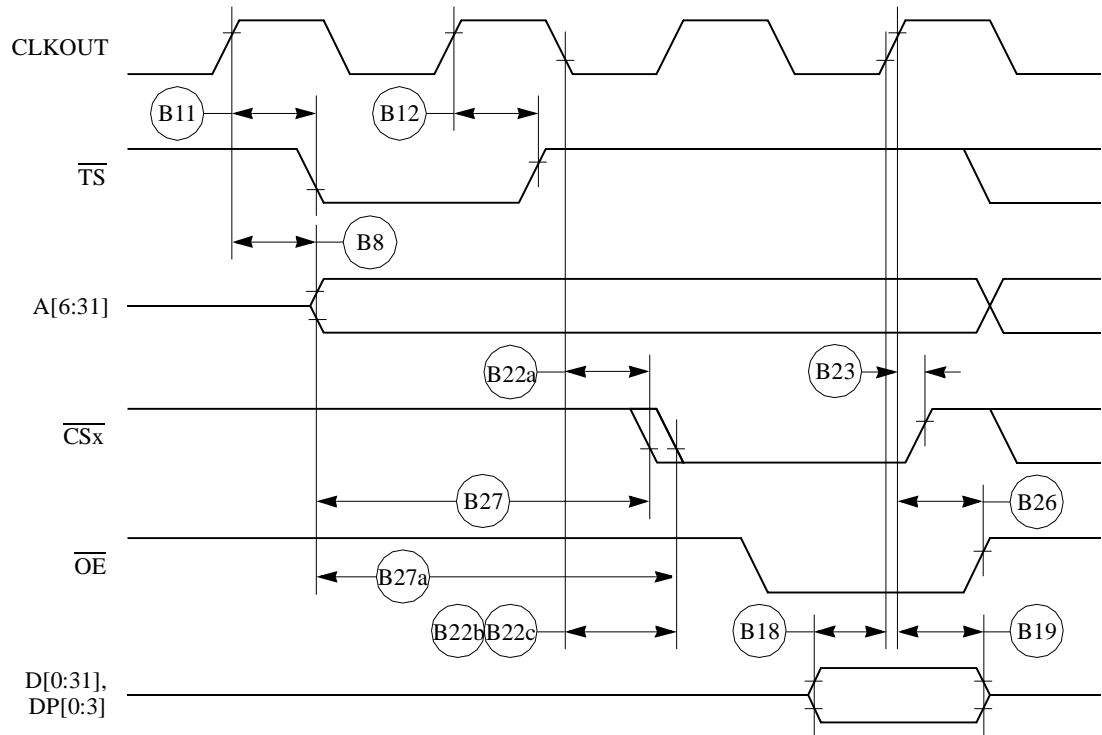


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

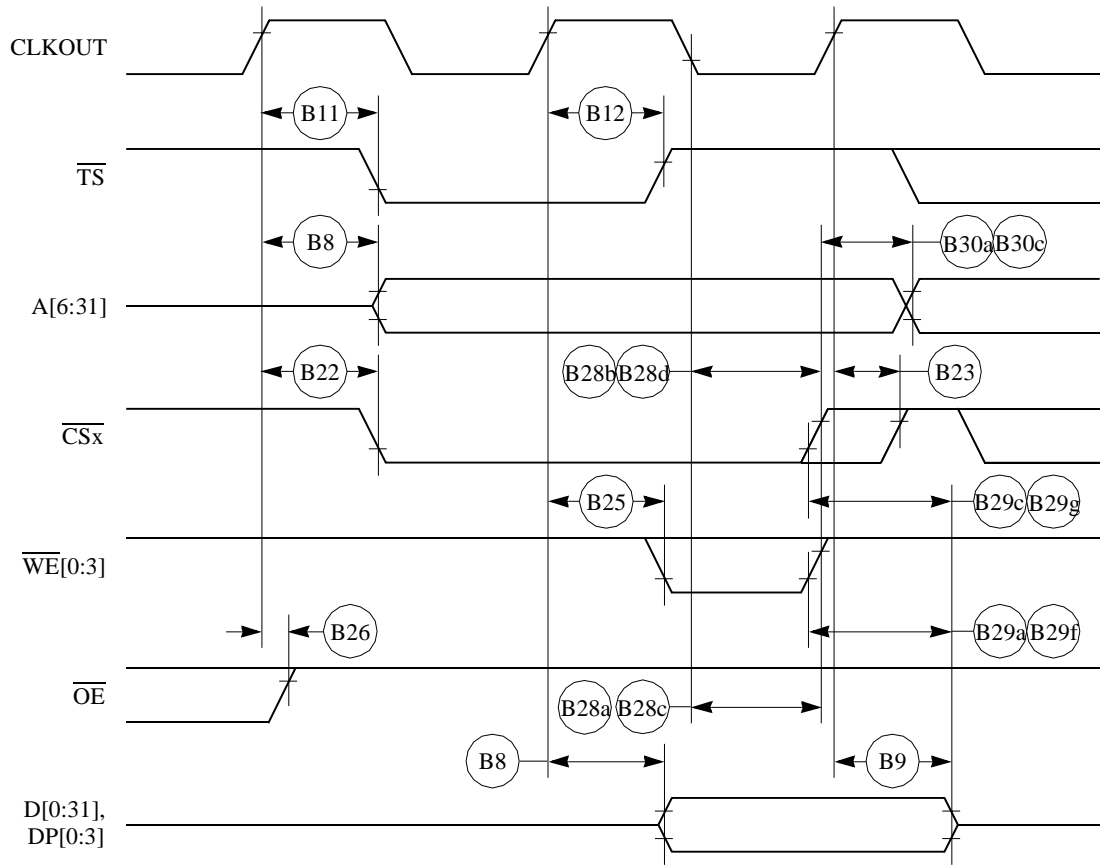


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Figure 16 provides the timing for the external bus controlled by the UPM.

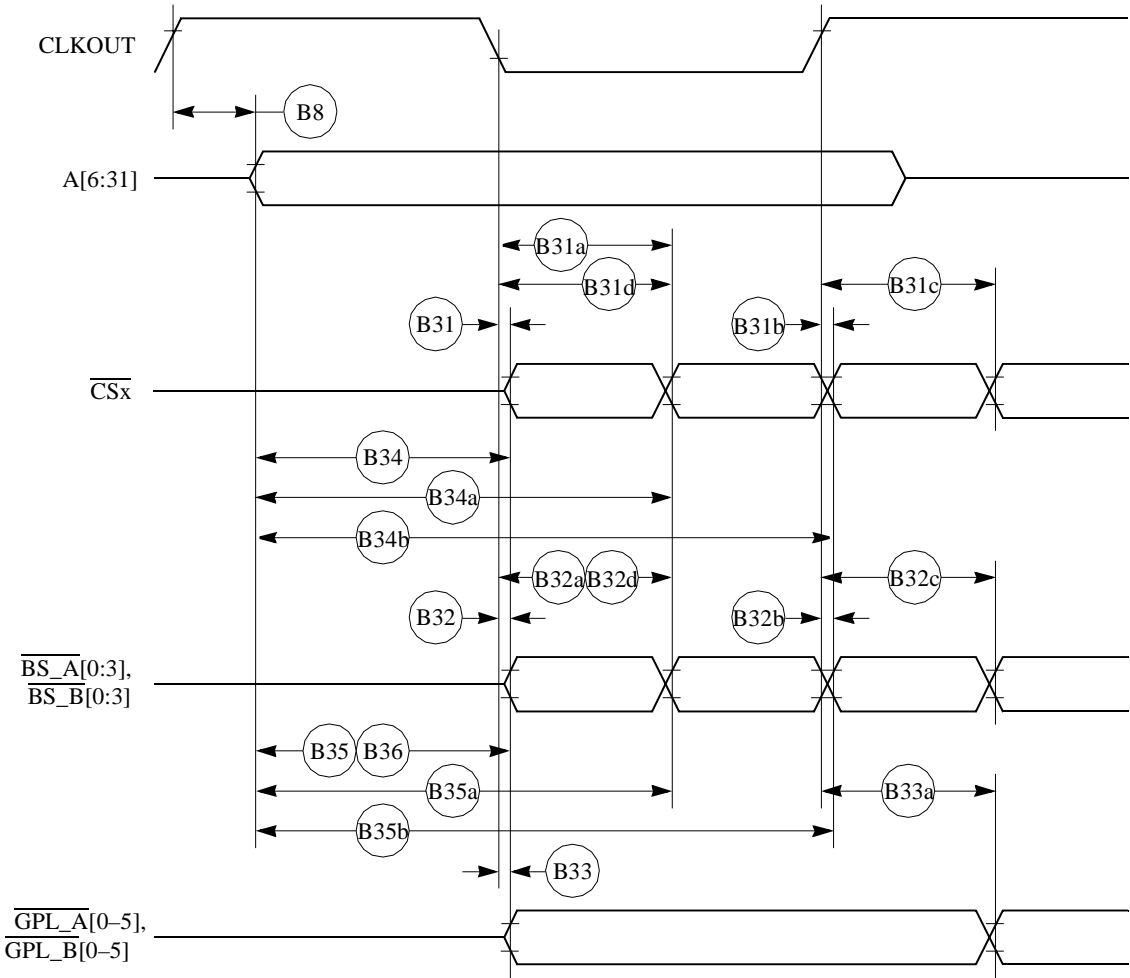


Figure 16. External Bus Timing (UPM Controlled Signals)

Table 8 shows the PCMCIA timing for the MPC850.

**Table 8. PCMCIA Timing**

Num	Characteristic	50MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
P44	A[6–31], $\overline{\text{REG}}$ valid to PCMCIA strobe asserted. <sup>1</sup>	13.00	—	21.00	—	17.00	—	0.750	ns
P45	A[6–31], $\overline{\text{REG}}$ valid to ALE negation. <sup>1</sup>	18.00	—	28.00	—	23.00	—	1.000	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid.	6.00	—	9.00	—	7.00	—	0.250	ns
P48	CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ asserted.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	
P49	CLKOUT to $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ negated.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P50	CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ assert time.	—	11.00	—	11.00	—	11.00	—	ns
P51	CLKOUT to $\overline{\text{PCOE}}$ , $\overline{\text{IORD}}$ , $\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negate time.	2.00	11.00	2.00	11.00	2.00	11.00	—	ns
P52	CLKOUT to ALE assert time	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P53	CLKOUT to ALE negate time	—	13.00	—	16.00	—	14.00	0.250	ns
P54	$\overline{\text{PCWE}}$ , $\overline{\text{IOWR}}$ negated to D[0–31] invalid. <sup>1</sup>	3.00	—	6.00	—	4.00	—	0.250	ns
P55	$\overline{\text{WAIT\_B}}$ valid to CLKOUT rising edge. <sup>1</sup>	8.00	—	8.00	—	8.00	—	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAIT\_B}}$ invalid. <sup>1</sup>	2.00	—	2.00	—	2.00	—	—	ns

<sup>1</sup> PSST = 1. Otherwise add PSST times cycle time.  
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the  $\overline{\text{WAIT\_B}}$  signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The  $\overline{\text{WAIT\_B}}$  assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC850 PowerQUICC User's Manual.



Figure 24 provides the PCMCIA access cycle timing for the external bus read.

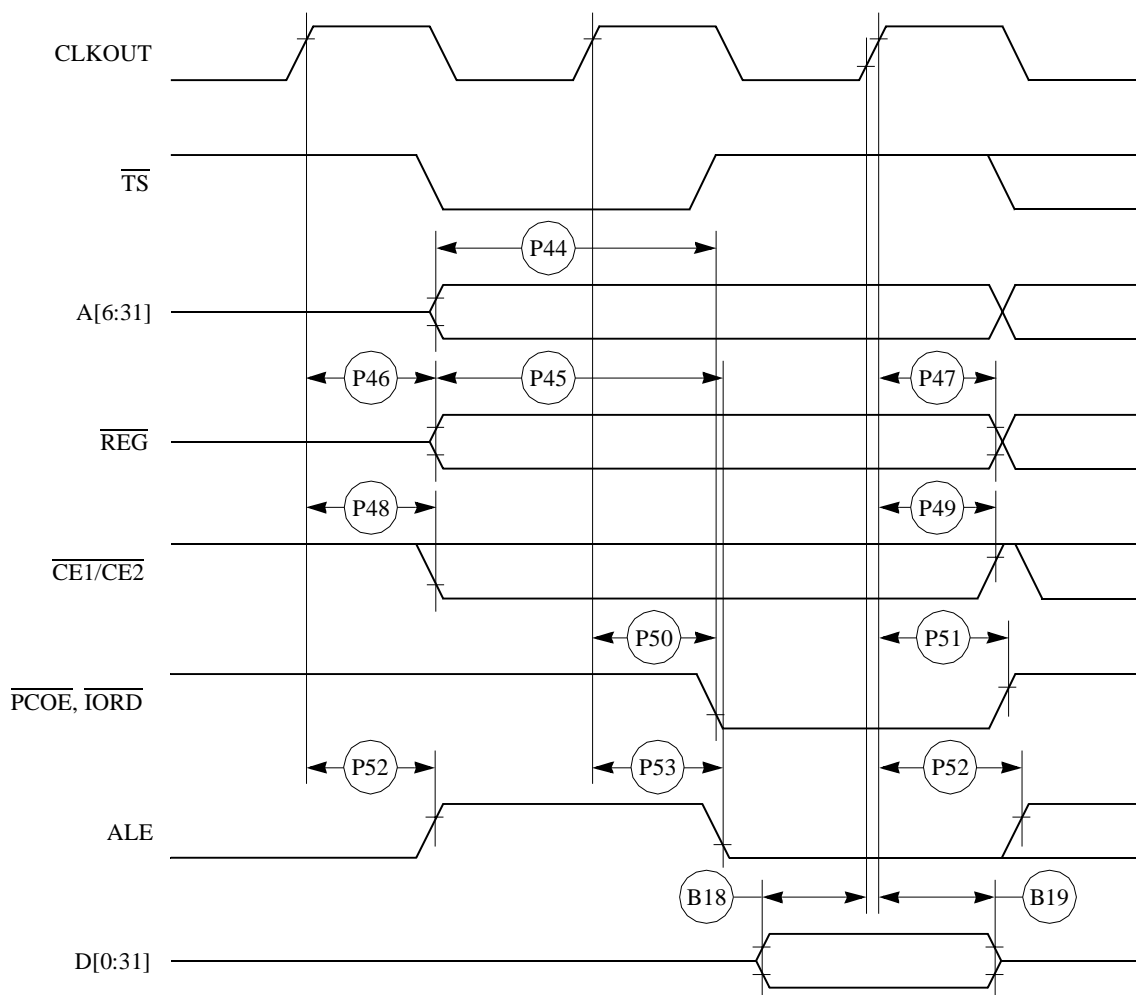


Figure 24. PCMCIA Access Cycles Timing External Bus Read

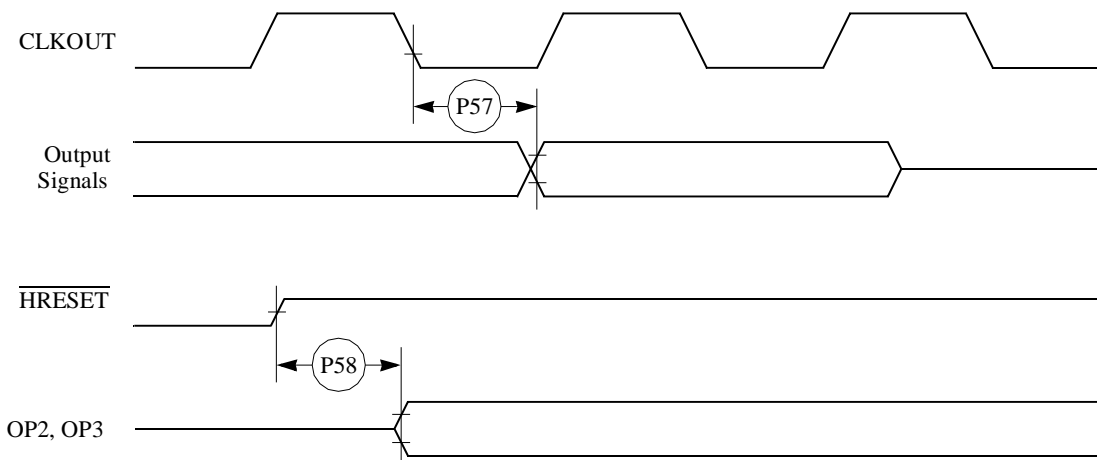
Table 9 shows the PCMCIA port timing for the MPC850.

**Table 9. PCMCIA Port Timing**

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive <sup>1</sup>	18.00	—	26.00	—	22.00	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	ns

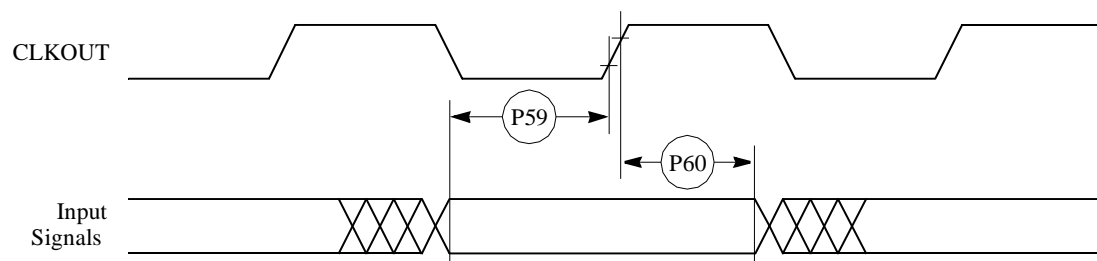
<sup>1</sup> OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.



**Figure 27. PCMCIA Output Port Timing**

Figure 28 provides the PCMCIA output port timing for the MPC850.



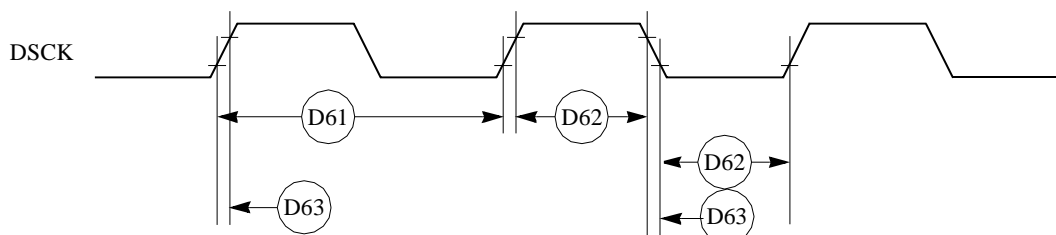
**Figure 28. PCMCIA Input Port Timing**

Table 10 shows the debug port timing for the MPC850.

**Table 10. Debug Port Timing**

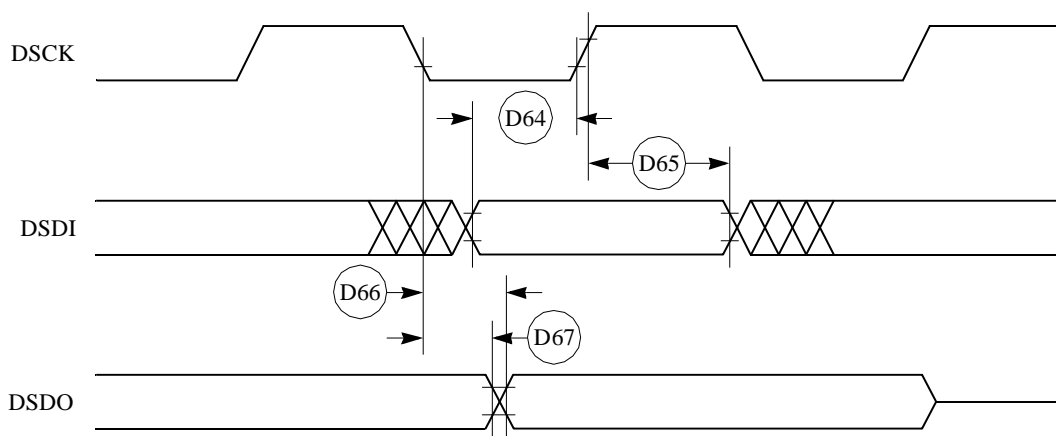
Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
D61	DSCK cycle time	60.00	—	91.00	—	75.00	—	ns
D62	DSCK clock pulse width	25.00	—	38.00	—	31.00	—	ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	8.00	—	8.00	—	ns
D65	DSDI data hold time	5.00	—	5.00	—	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	0.00	2.00	ns

Figure 29 provides the input timing for the debug port clock.



**Figure 29. Debug Port Clock Input Timing**

Figure 30 provides the timing for the debug port.



**Figure 30. Debug Port Timings**

Table 11 shows the reset timing for the MPC850.

**Table 11. Reset Timing**

Num	Characteristic	50 MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	340.00	—	515.00	—	425.00	—	17.000	ns
R72		—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R80	DSDI, DSCK set up	60.00	—	90.00	—	75.00	—	3.000	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns

Figure 33 provides the reset timing for the debug port configuration.

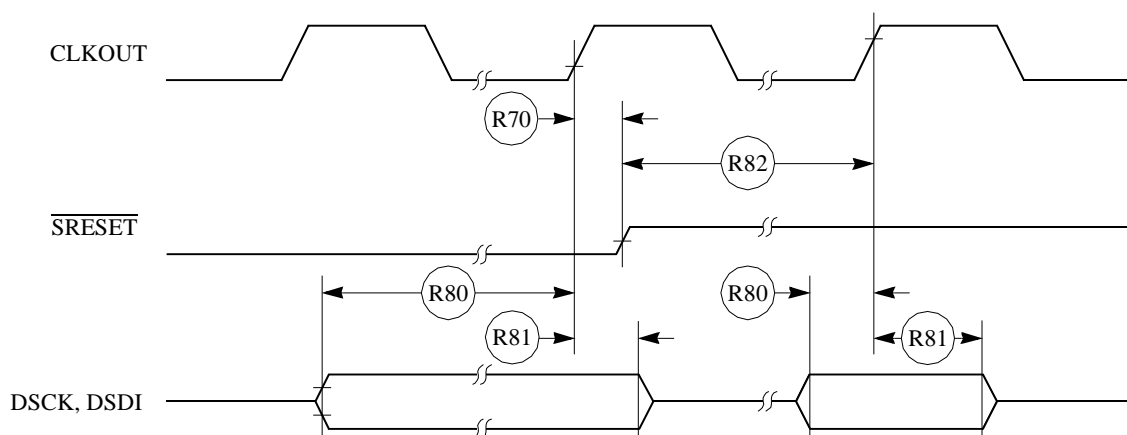


Figure 33. Reset Timing—Debug Port Configuration

## 7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

Table 12. JTAG Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
J82	TCK cycle time	100.00	—	100.00	—	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	40.00	—	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	5.00	—	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	25.00	—	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	—	27.00	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	0.00	—	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	—	20.00	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	100.00	—	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	40.00	—	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	—	50.00	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	—	50.00	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	—	50.00	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	50.00	—	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	50.00	—	50.00	—	ns

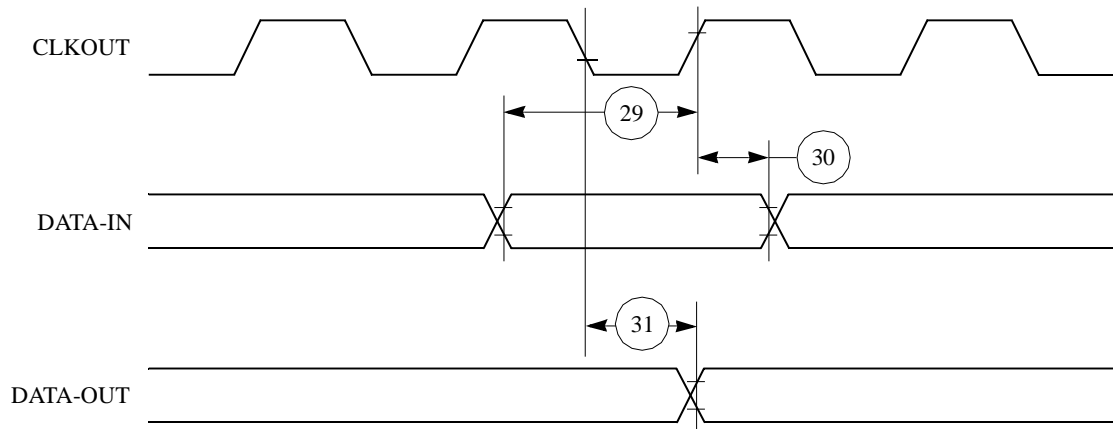


Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

## 8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Table 14. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7.00	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3.00	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12.00	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12.00	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20.00	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15.00	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$ )	7.00	—	ns

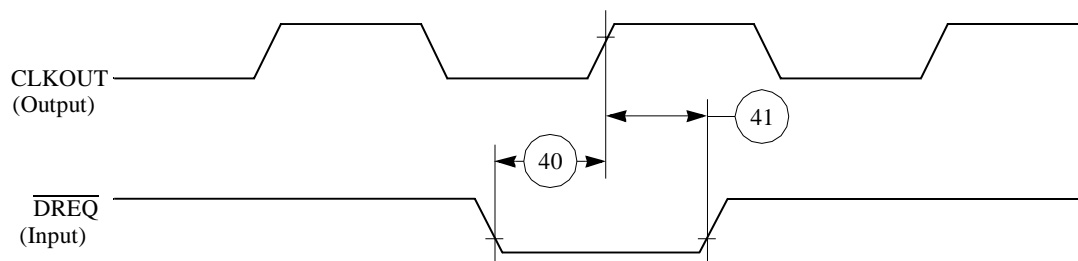


Figure 39. IDMA External Requests Timing Diagram

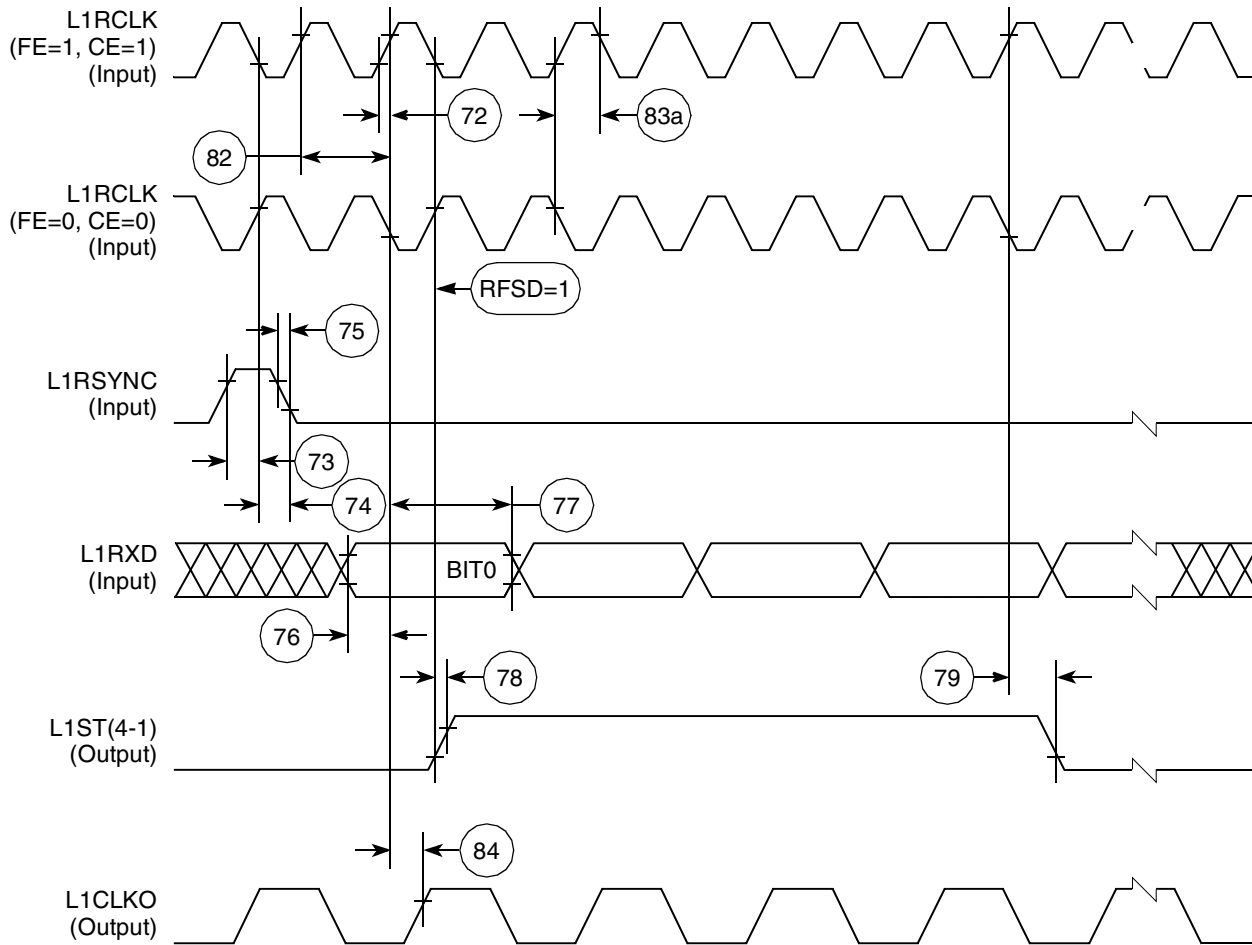


Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

## 8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

**Table 18. NMSI External Clock Timing**

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency <sup>1</sup> (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	—	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge <sup>2</sup>	5.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	5.00	—	ns

<sup>1</sup> The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

<sup>2</sup> Also applies to  $\overline{\text{CD}}$  and  $\overline{\text{CTS}}$  hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

**Table 19. NMSI Internal Clock Timing**

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency <sup>1</sup> (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time	—	—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	40.00	—	ns
106	RXDx setup time to RCLKx rising edge	40.00	—	ns
107	RXDx hold time from RCLKx rising edge <sup>2</sup>	0.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	40.00	—	ns

<sup>1</sup> The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

<sup>2</sup> Also applies to  $\overline{\text{CD}}$  and  $\overline{\text{CTS}}$  hold time when they are used as an external sync signals.



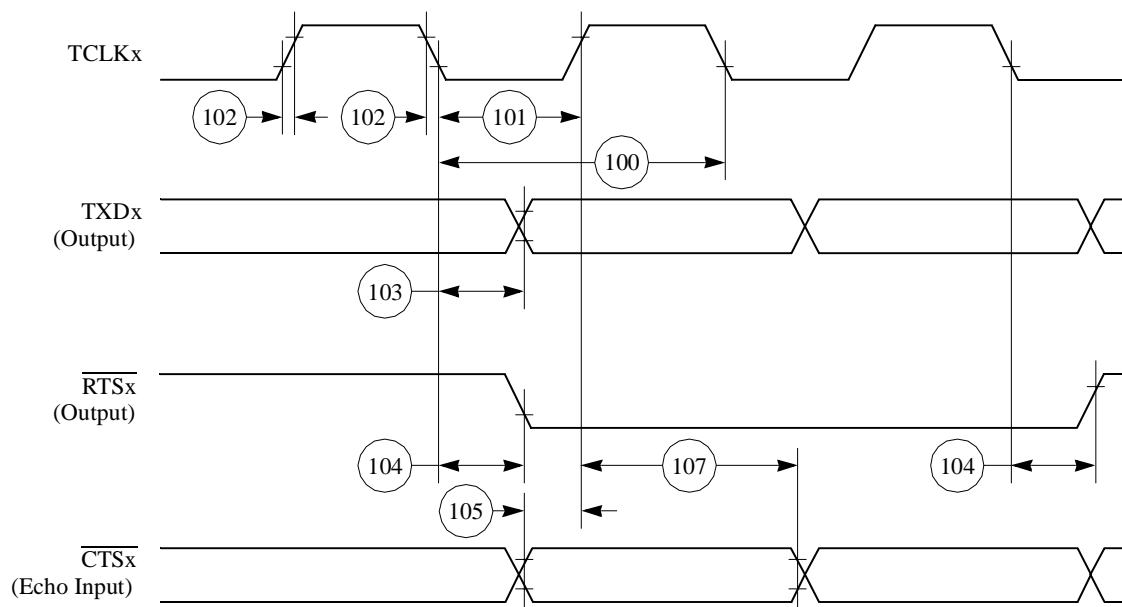


Figure 52. HDLC Bus Timing Diagram

## 8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period <sup>1</sup>	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period <sup>1</sup>	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns

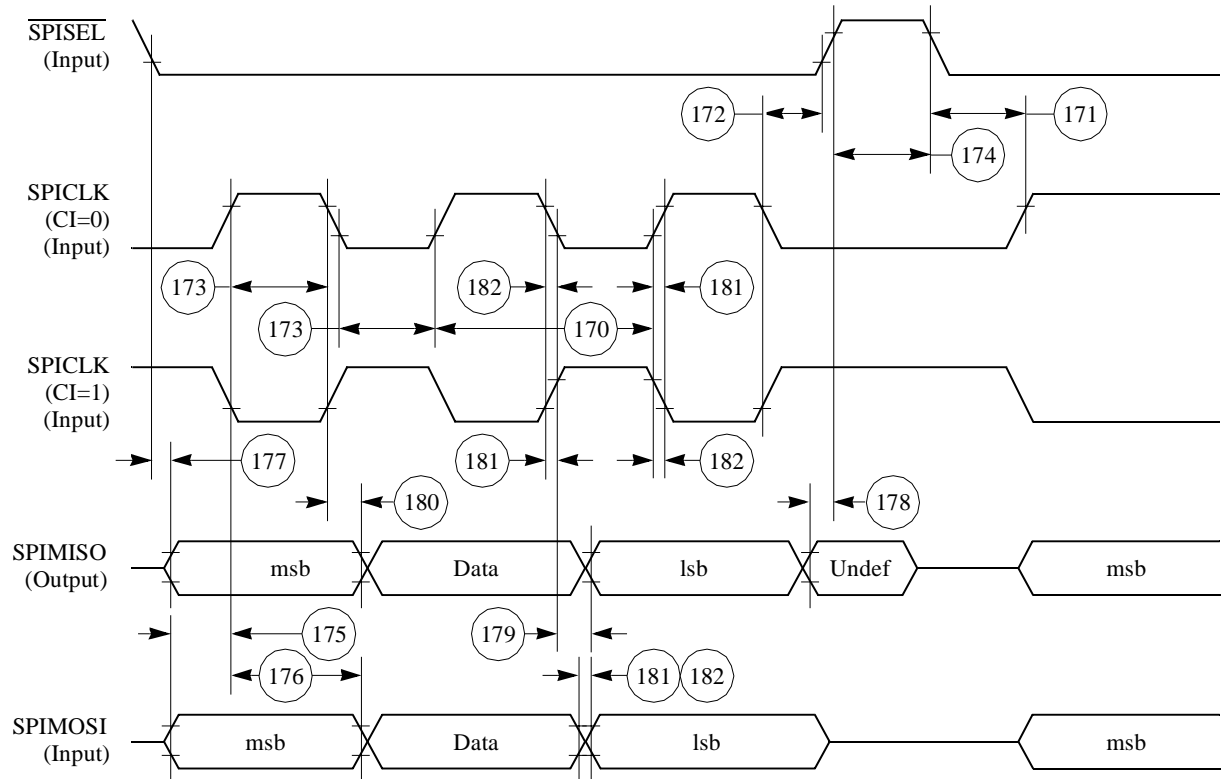


Figure 59. SPI Slave (CP = 0) Timing Diagram

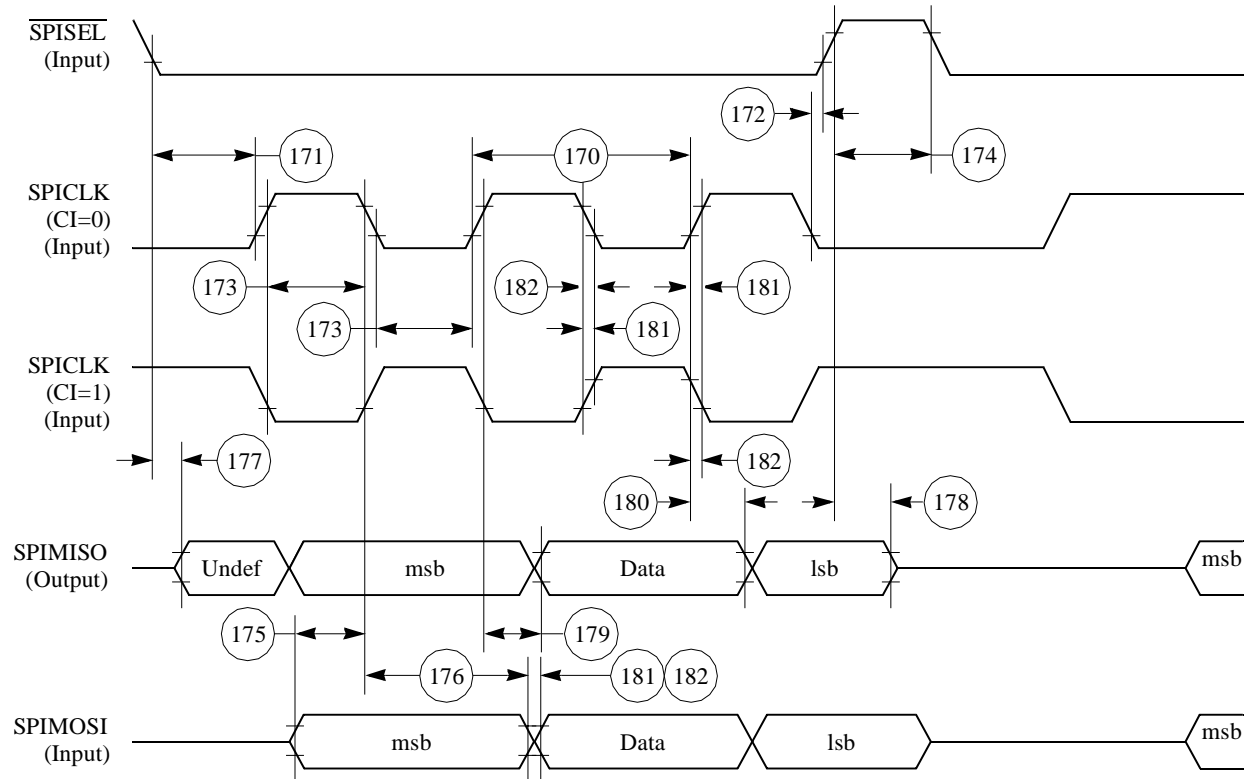


Figure 60. SPI Slave (CP = 1) Timing Diagram

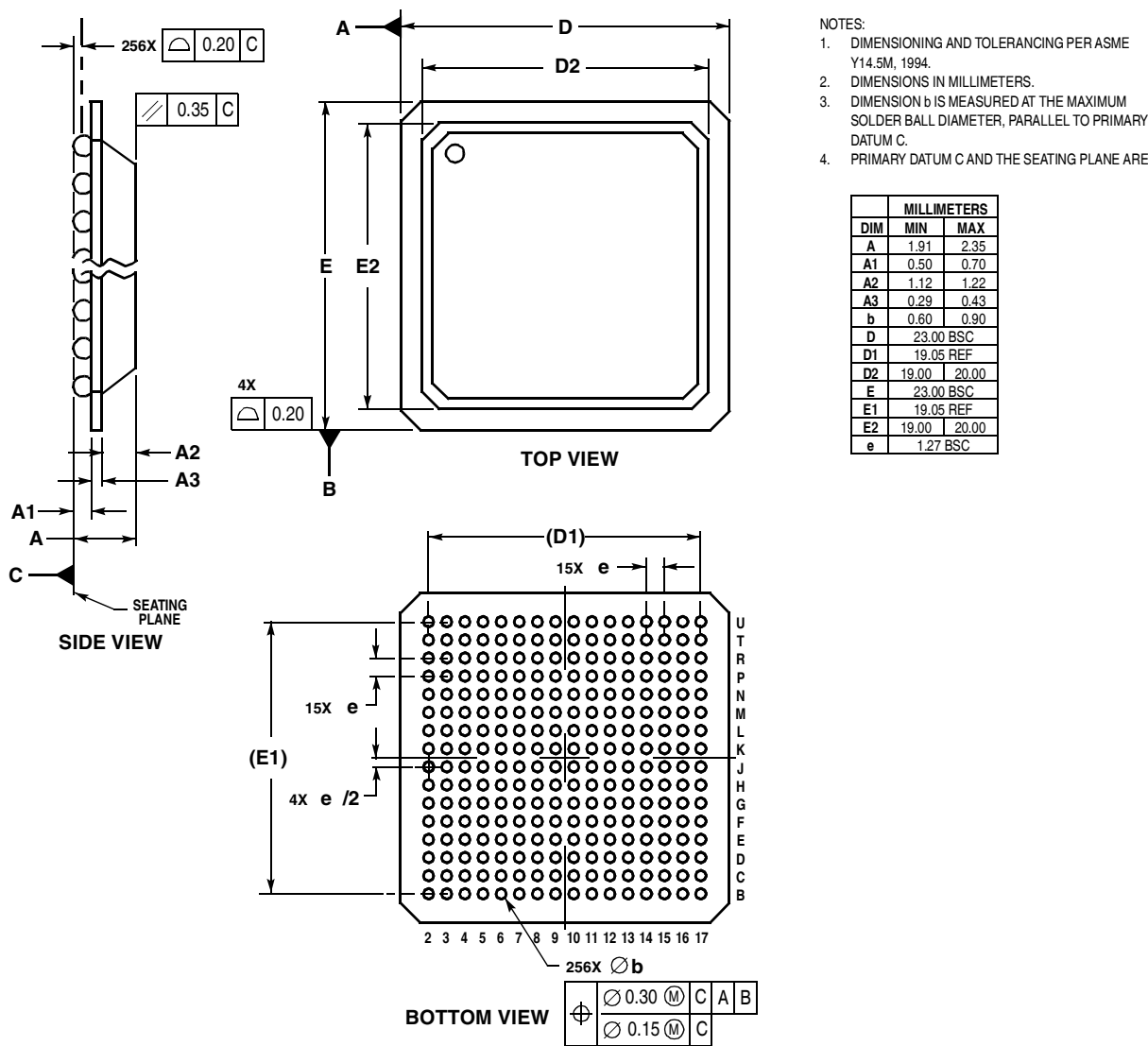
## 8.11 I<sup>2</sup>C AC Electrical Specifications

Table 24 provides the I<sup>2</sup>C (SCL < 100 KHz) timings.

Table 24. I<sup>2</sup>C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) <sup>1</sup>	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	—	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	—	ns
209	SDL/SCL rise time	—	1.00	μs

Figure 65 shows the JEDEC package dimensions of the PBGA.



CASE 1130-01  
ISSUE B

Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **email:**

[support@freescale.com](mailto:support@freescale.com)

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
(800) 521-6274  
480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku  
Tokyo 153-0064, Japan  
0120 191014  
+81 2666 8080  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate,  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor  
Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
(800) 441-2447  
303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2005.