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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850devr80bu

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I²C port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

Table 1. MPC850 Functionality Matrix

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Additional documentation may be provided for parts listed in Table 1.



- Gate mode can enable/disable counting
- Interrupt can be masked on reference match and event capture

Interrupts

- Eight external interrupt request (IRQ) lines
- Twelve port pins with interrupt capability
- Fifteen internal interrupt sources
- Programmable priority among SCCs and USB
- Programmable highest-priority request
- Single socket PCMCIA-ATA interface
 - Master (socket) interface, release 2.1 compliant
 - Single PCMCIA socket
 - Supports eight memory or I/O windows
- Communications processor module (CPM)
 - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
 - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission
 after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD
 closes the receive buffer descriptor)
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 8 Kbytes of dual-port RAM
 - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
 - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
 - Can be connected to any SCC, SMC, or USB
 - Allow changes during operation
 - Autobaud support option
- Two SCCs (serial communications controllers)
 - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
 - HDLC/SDLCTM (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support PPP (point-to-point protocol)
 - AppleTalk[®]
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))

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Table 6. Bus Operation Timing ¹ (continued)

Nivers	Oh avaataviatia	50 I	MHz	66 1	ИНz	80 1	ИНz	FFACT	Cap Load	I I m i A
Num	Characteristic	Min	Max	Min	Max	Min	Max	FFACT	(default 50 pF)	Unit
B22	CLKOUT rising edge to CS asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0,1	_	8.00	_	8.00	_	8.00	_	50.00	ns
B22b	CLKOUT falling edge to CS asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	_	50.00	ns
B24	A[6-31] to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0.	3.00	_	6.00	_	4.00	_	0.250	50.00	ns
B24a	A[6–31] to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0	8.00	_	13.00	_	11.00	_	0.500	50.00	ns
B25	CLKOUT rising edge to OE, WE[0-3] asserted	_	9.00	_	9.00	_	9.00	_	50.00	ns
B26	CLKOUT rising edge to OE negated	2.00	9.00	2.00	9.00	2.00	9.00	_	50.00	ns
B27	A[6–31] to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 1	23.00	_	36.00	_	29.00	_	1.250	50.00	ns
B27a	A[6–31] to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 1	28.00	_	43.00	_	36.00	_	1.500	50.00	ns
B28	CLKOUT rising edge to WE[0-3] negated GPCM write access CSNT = 0	_	9.00	_	9.00	_	9.00	_	50.00	ns
B28a	CLKOUT falling edge to WE[0-3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	_	12.00	_	14.00	_	13.00	0.250	50.00	ns



Table 6. Bus Operation Timing ¹ (continued)

Num	Chavastavistis	50 I	ИНz	66 I	ИНz	80 1	ИНz	FEACT	Cap Load	l lmit
Num	Characteristic	Min	Max	Min	Max	Min	Max	FFACT	(default 50 pF)	Unit
B28c	CLKOUT falling edge to WE[0-3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to CS negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	_	14.00	_	18.00	_	16.00	0.375	50.00	ns
B29	WE[0-3] negated to D[0-31], DP[0-3] high-Z GPCM write access, CSNT = 0	3.00	_	6.00	_	4.00	_	0.250	50.00	ns
B29a	WE[0-3] negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	_	13.00	_	11.00	_	0.500	50.00	ns
B29b	CS negated to D[0-31], DP[0-3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	_	6.00	_	4.00	_	0.250	50.00	ns
B29c	CS negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	_	13.00	_	11.00	_	0.500	50.00	ns
B29d	WE[0-3] negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	_	43.00	_	36.00	_	1.500	50.00	ns
B29e	CS negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	_	43.00	_	36.00	_	1.500	50.00	ns
B29f	WE[0-3] negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	_	9.00	_	7.00	_	0.375	50.00	ns
B29g	CS negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	_	9.00	_	7.00	_	0.375	50.00	ns



Figure 4 provides the timing for the synchronous output signals.

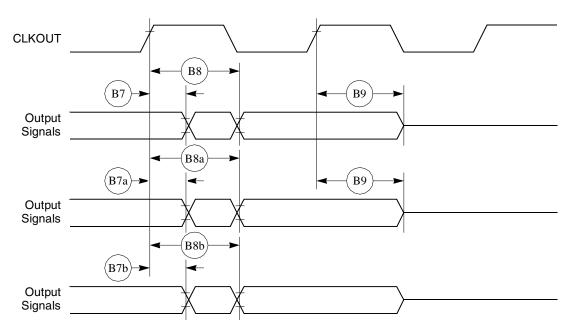


Figure 4. Synchronous Output Signals Timing

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.

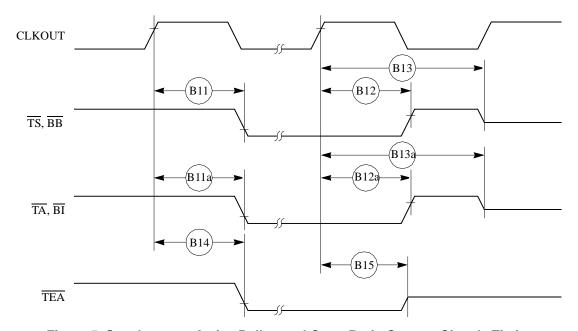


Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing

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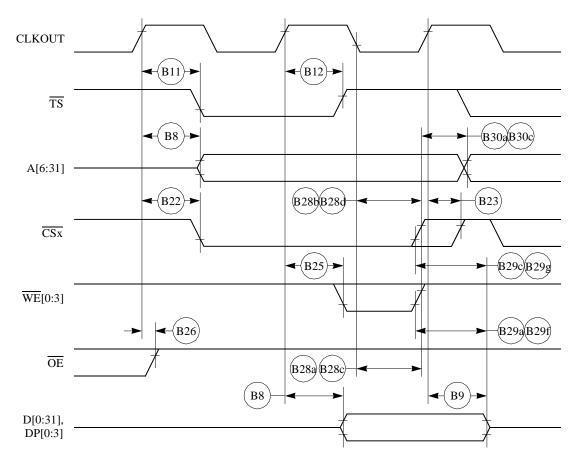


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)



Figure 25 provides the PCMCIA access cycle timing for the external bus write.

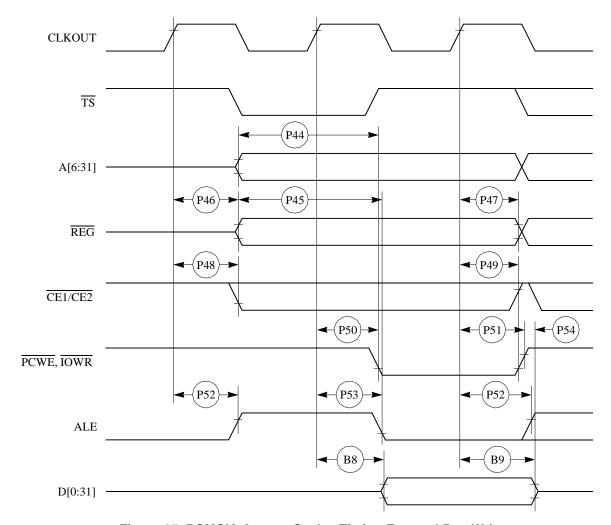


Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.

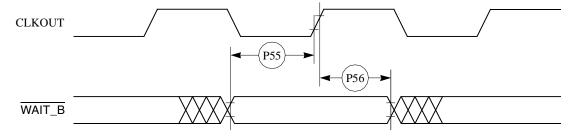


Figure 26. PCMCIA WAIT Signal Detection Timing

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Table 10 shows the debug port timing for the MPC850.

Table 10. Debug Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
Num	Characteristic	Min	Max	Min	Max	Min	Max	Oilit
D61	DSCK cycle time	60.00	_	91.00	_	75.00	_	ns
D62	DSCK clock pulse width	25.00	_	38.00	_	31.00	_	ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00	_	8.00	_	8.00	_	ns
D65	DSDI data hold time	5.00	_	5.00	_	5.00	_	ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	0.00	2.00	ns

Figure 29 provides the input timing for the debug port clock.

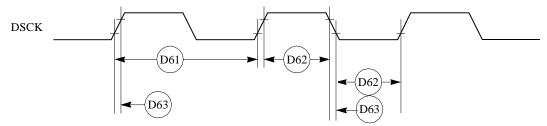


Figure 29. Debug Port Clock Input Timing

Figure 30 provides the timing for the debug port.

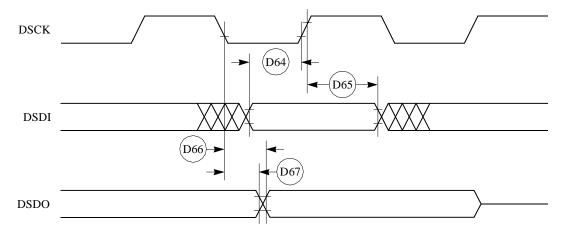


Figure 30. Debug Port Timings

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Table 11 shows the reset timing for the MPC850.

Table 11. Reset Timing

Num	Characteristic	50 N	ЛНz	66N	ЛHz	80 1	ИНz	FFACTOR	Unit
INUIII	Characteristic	Min	Max	Min	Max	Min	Max	FFACION	Onit
R69	CLKOUT to HRESET high impedance	_	20.00	_	20.00	_	20.00	_	ns
R70	CLKOUT to SRESET high impedance	_	20.00	_	20.00	_	20.00	_	ns
R71	RSTCONF pulse width	340.00	_	515.00	_	425.00	_	17.000	ns
R72		_	_	_	_	_	_	_	
R73	Configuration data to HRESET rising edge set up time	350.00	_	505.00	_	425.00	_	15.000	ns
R74	Configuration data to RSTCONF rising edge set up time	350.00	_	350.00	_	350.00	_	_	ns
R75	Configuration data hold time after RSTCONF negation	0.00	_	0.00	_	0.00	_	_	ns
R76	Configuration data hold time after HRESET negation	0.00	_	0.00	_	0.00	_	_	ns
R77	HRESET and RSTCONF asserted to data out drive	_	25.00	_	25.00	_	25.00	_	ns
R78	RSTCONF negated to data out high impedance.	_	25.00	_	25.00	_	25.00	_	ns
R79	CLKOUT of last rising edge before chip tristates HRESET to data out high impedance.	_	25.00	_	25.00	_	25.00	_	ns
R80	DSDI, DSCK set up	60.00	_	90.00	_	75.00	_	3.000	ns
R81	DSDI, DSCK hold time	0.00	_	0.00	_	0.00	_	_	ns
R82	SRESET negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	_	242.00	_	200.00	_	8.000	ns



Figure 31 shows the reset timing for the data bus configuration.

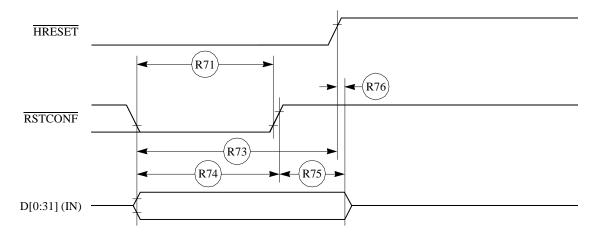


Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

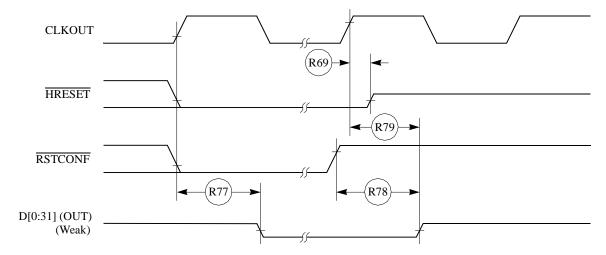


Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

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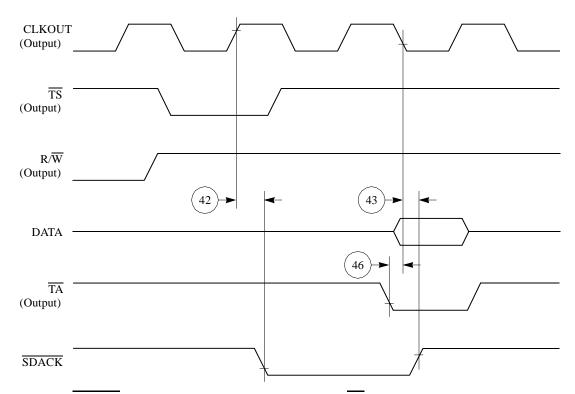


Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock



Table 20	Ethernet	Timing ((continued)
I abic 20.		I IIIIIIII	(COIILIIIA C A)

Num	Characteristic	All Fred	Unit	
	Offactoristic		Max	Oilit
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to SDACK asserted ²		20.00	ns
139	CLKOUT low to SDACK negated ²	_	20.00	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame destination address into memory.

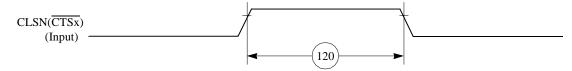


Figure 53. Ethernet Collision Timing Diagram

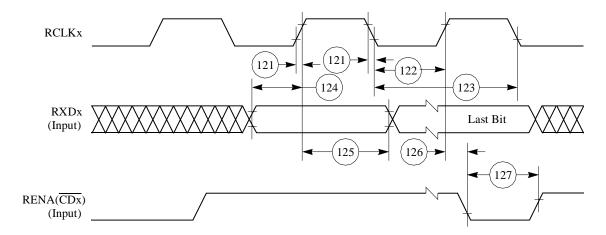
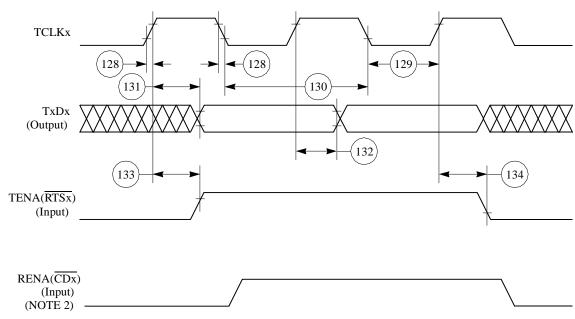


Figure 54. Ethernet Receive Timing Diagram

CPM Electrical Characteristics



- NOTES:
 - 1. Transmit clock invert (TCI) bit in GSMR is set.
 - If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 55. Ethernet Transmit Timing Diagram

8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

Table 21. Serial Management Controller Timing

Num	Characteristic	All Frequ	Unit	
Num	um ondiaoteristio		Max	Oilit
150	SMCLKx clock period ¹	100.00	_	ns
151	SMCLKx width low	50.00	_	ns
151a	SMCLKx width high	50.00	_	ns
152	SMCLKx rise/fall time	_	15.00	ns
153	SMTXDx active delay (from SMCLKx falling edge)	10.00	50.00	ns
154	SMRXDx/SMSYNx setup time	20.00	_	ns
155	SMRXDx/SMSYNx hold time	5.00	_	ns

¹ The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.



CPM Electrical Characteristics

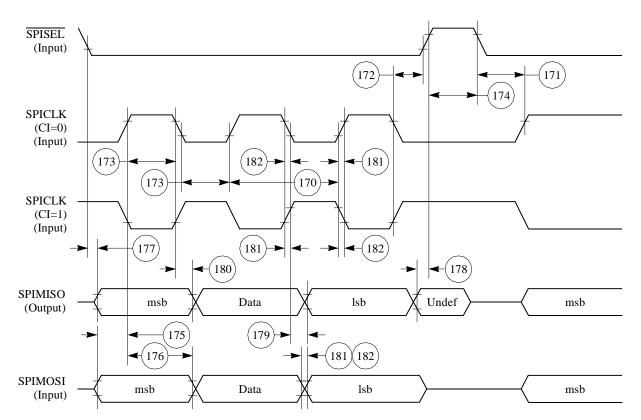


Figure 59. SPI Slave (CP = 0) Timing Diagram



Table 24. I²C Timing (SCL < 100 KHz) (CONTINUED)

Num	Num Characteristic		encies	Unit
Num	Onaracteristic	Min	Max	Ome
210	SDL/SCL fall time	_	300.00	ns
211	Stop condition setup time	4.70	_	μs

SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I^2C (SCL > 100 KHz) timings.

Table 25. I^2C Timing (SCL > 100 KHz)

Num	Characteristic	Everencies	All Freq	uencies	Unit
Nulli	Characteristic	Expression	Min	Max	Onit
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) ¹	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	_	S
203	Low period of SCL		1/(2.2 * fSCL)	_	S
204	High period of SCL		1/(2.2 * fSCL)	_	S
205	Start condition setup time		1/(2.2 * fSCL)	_	S
206	Start condition hold time		1/(2.2 * fSCL)	_	s
207	Data hold time		0	_	s
208	Data setup time		1/(40 * fSCL)	_	s
209	SDL/SCL rise time		_	1/(10 * fSCL)	S
210	SDL/SCL fall time		_	1/(33 * fSCL)	S
211	Stop condition setup time		1/2(2.2 * fSCL)	_	S

SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 61 shows the I²C bus timing.

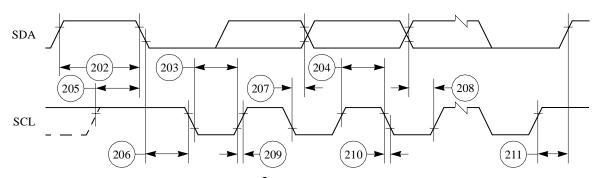


Figure 61. I²C Bus Timing Diagram

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Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface.

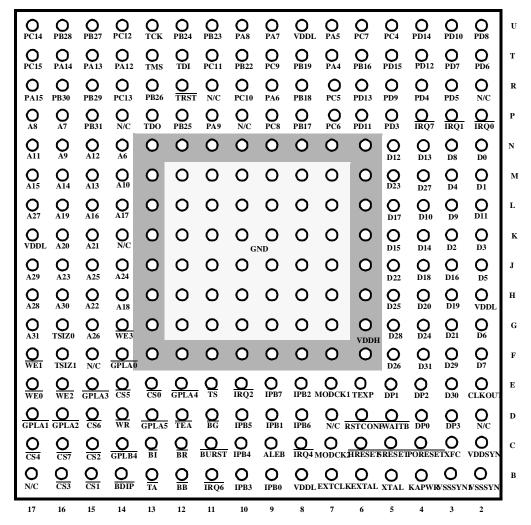


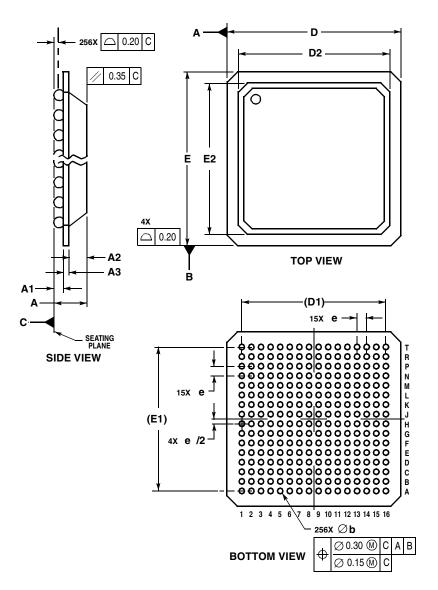
Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.



Mechanical Data and Ordering Information

Figure 64 shows the non-JEDEC package dimensions of the PBGA.



NOTES

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. DIMENSIONS IN MILLIMETERS.
- DIMENSION 6 IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
- 4. PRIMARY DATUM C AND THE SEATING PLANE ARE

	MILLIN	IETERS			
DIM	MIN	MAX			
Α	1.91	2.35			
A 1	0.50	0.70			
A2	1.12	1.22			
A3	0.29	0.43			
b	0.60	0.90			
D	23.00	BSC			
D1	19.05	REF			
D2	19.00	20.00			
Е	23.00	BSC			
E1	19.05 REF				
E2	19.00	20.00			
е	1.27	BSC			

Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard

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Document Revision History

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