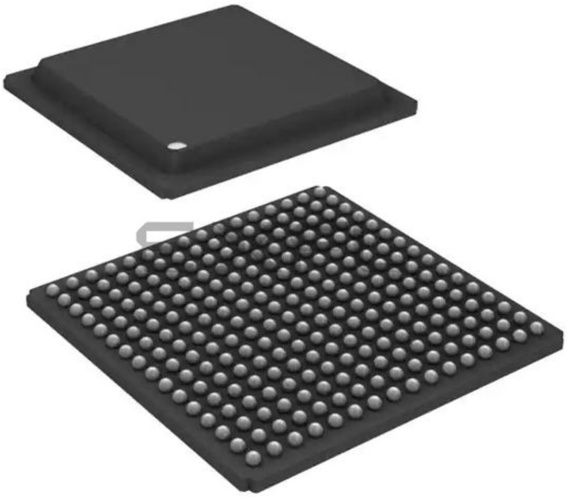

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850dezq66bur2

- 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
  - Caches are two-way, set-associative
  - Physically addressed
  - Cache blocks can be updated with a 4-word line burst
  - Least-recently used (LRU) replacement algorithm
  - Lockable one-line granularity
- Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
- MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups

• Advanced on-chip emulation debug mode

• Data bus dynamic bus sizing for 8, 16, and 32-bit buses
- Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
- Twenty-six external address lines

• Completely static design (0–80 MHz operation)

• System integration unit (SIU)
- Hardware bus monitor
- Spurious interrupt monitor
- Software watchdog
- Periodic interrupt timer
- Low-power stop mode
- Clock synthesizer
- Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
- Reset controller
- IEEE 1149.1 test access port (JTAG)

• Memory controller (eight banks)
- Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
- Memory controller programmable to support most size and speed memory interfaces
- Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
- Variable block sizes, 32 Kbytes to 256 Mbytes
- Selectable write protection
- On-chip bus arbiter supports one external bus master
- Special features for burst mode support

• General-purpose timers
- Four 16-bit timers or two 32-bit timers

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA [1]	θ_{JA}	40 [2]	°C/W
	θ_{JA}	31 [3]	°C/W
	θ_{JA}	24 [4]	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

1 For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, *Plastic Ball Grid Array Application Note* available from your local Freescale sales office.

2 Assumes natural convection and a single layer board (no thermal vias).

3 Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

4 Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

1 Typical power dissipation is measured at 3.3V

2 Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

θ_{JA} = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$P_D = K \div (T_J + 273°C)$(2)

Solving equations (1) and (2) for K gives:

$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$(3)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

5.1 Layout Practices

Each V_{CC} pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B29h	$\overline{\text{WE}}$[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B29i	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B30	$\overline{\text{CS}}$, $\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access [9]	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B30a	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 0, CSNT =1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B30b	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B30c	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	8.00	—	6.00	—	0.375	50.00	ns
B30d	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT =1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

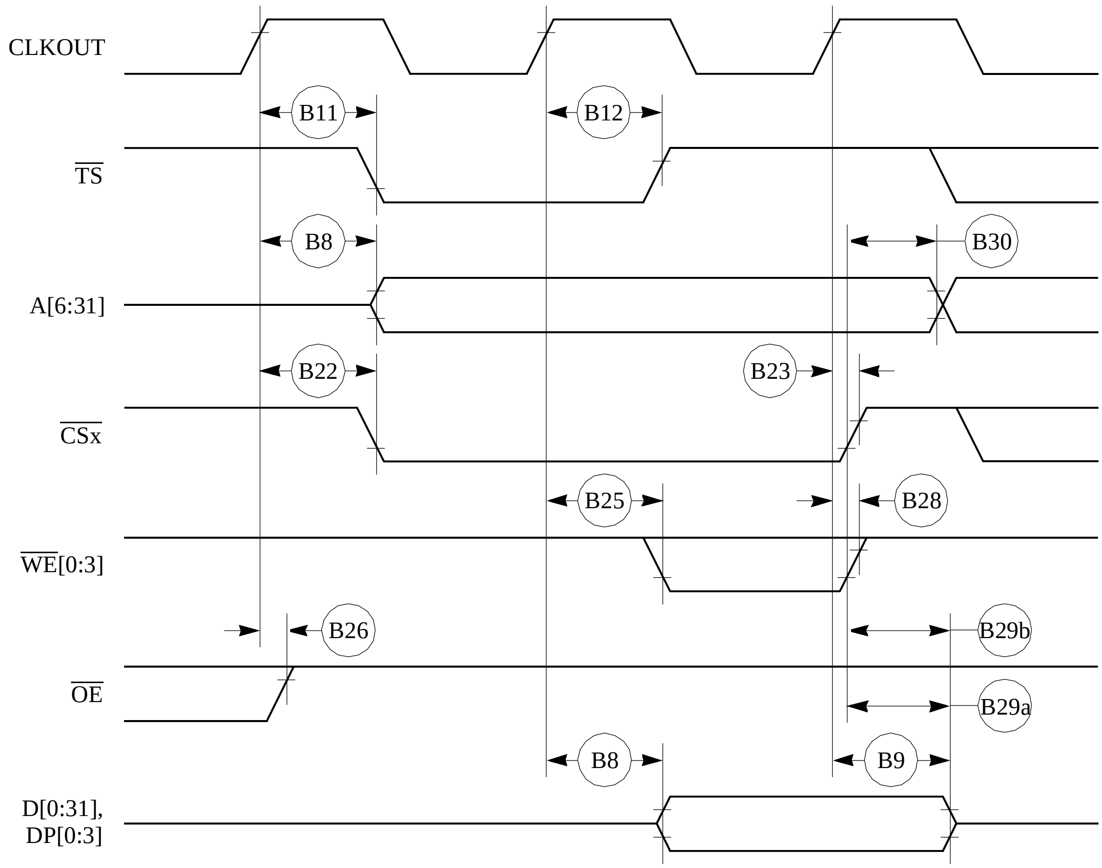


Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

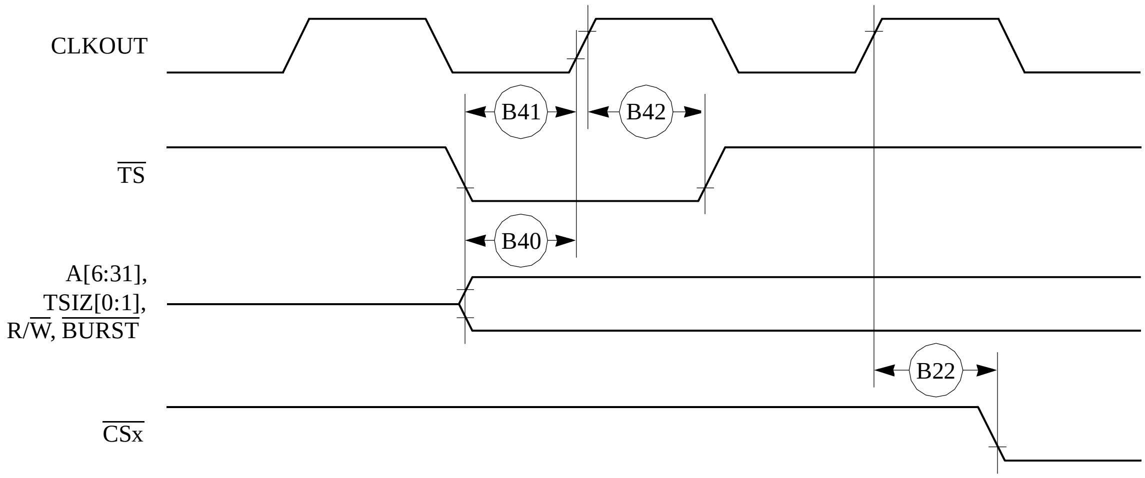


Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.

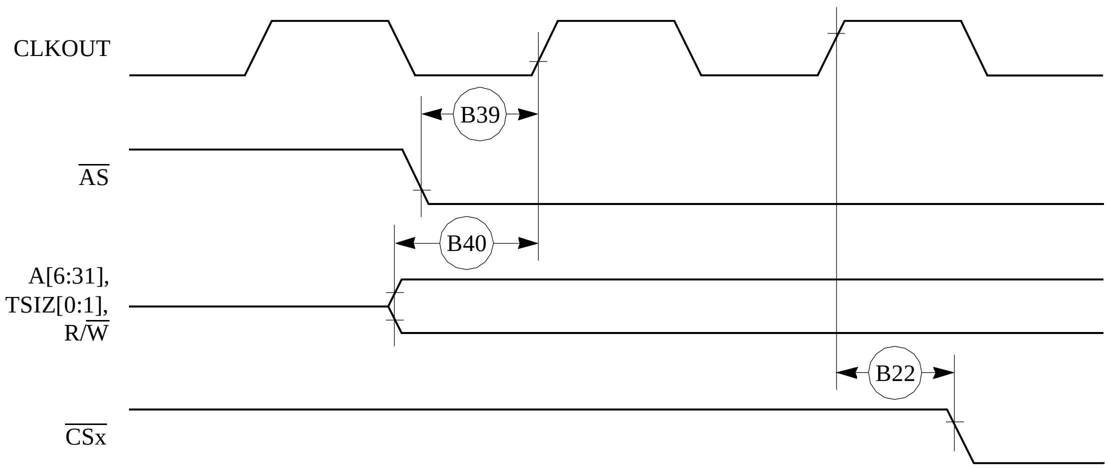


Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 21 provides the timing for the asynchronous external master control signals negation.

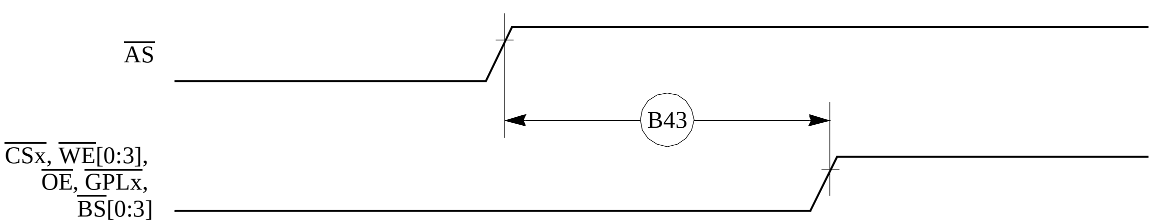


Figure 21. Asynchronous External Master—Control Signals Negation Timing

Table 7 provides interrupt timing for the MPC850.

Table 7. Interrupt Timing

Num	Characteristic [1]	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
I39	$\overline{\text{IRQx}}$ valid to CLKOUT rising edge (set up time)	6.00	—	6.00	—	6.00	—	ns
I40	$\overline{\text{IRQx}}$ hold time after CLKOUT.	2.00	—	2.00	—	2.00	—	ns
I41	$\overline{\text{IRQx}}$ pulse width low	3.00	—	3.00	—	3.00	—	ns
I42	$\overline{\text{IRQx}}$ pulse width high	3.00	—	3.00	—	3.00	—	ns
I43	$\overline{\text{IRQx}}$ edge-to-edge time	80.00	—	121.0	—	100.0	—	ns

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.

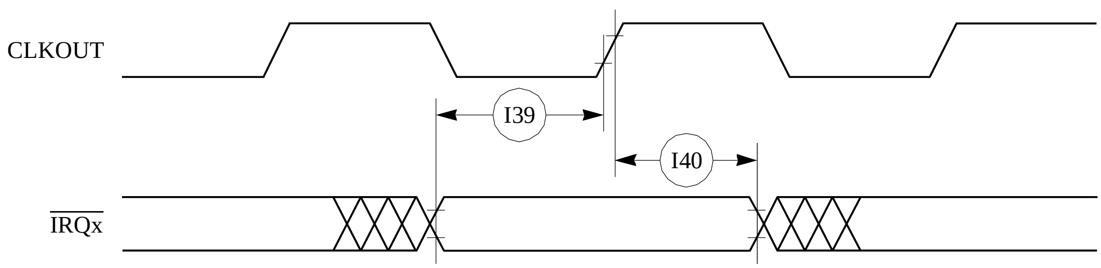


Figure 22. Interrupt Detection Timing for External Level Sensitive Lines

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.

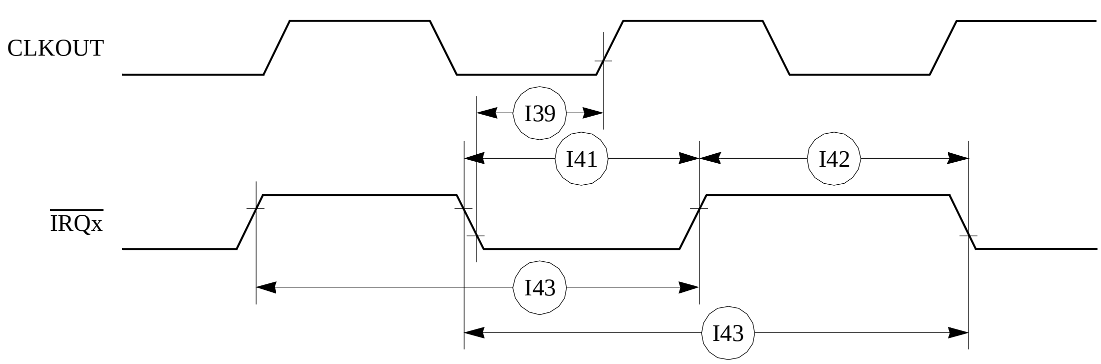


Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines

Table 8 shows the PCMCIA timing for the MPC850.

Table 8. PCMCIA Timing

Num	Characteristic	50MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
P44	A[6–31], $\overline{\text{REG}}$ valid to PCMCIA strobe asserted. [1]	13.00	—	21.00	—	17.00	—	0.750	ns
P45	A[6–31], $\overline{\text{REG}}$ valid to ALE negation.[1]	18.00	—	28.00	—	23.00	—	1.000	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid.	6.00	—	9.00	—	7.00	—	0.250	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time.	—	11.00	—	11.00	—	11.00	—	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time.	2.00	11.00	2.00	11.00	2.00	11.00	—	ns
P52	CLKOUT to ALE assert time	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P53	CLKOUT to ALE negate time	—	13.00	—	16.00	—	14.00	0.250	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D[0–31] invalid.[1]	3.00	—	6.00	—	4.00	—	0.250	ns
P55	$\overline{\text{WAIT\_B}}$ valid to CLKOUT rising edge.[1]	8.00	—	8.00	—	8.00	—	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAIT\_B}}$ invalid.[1]	2.00	—	2.00	—	2.00	—	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAIT\_B}}$ signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAIT\_B}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC850 PowerQUICC User's Manual.

Table 11 shows the reset timing for the MPC850.

Table 11. Reset Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	340.00	—	515.00	—	425.00	—	17.000	ns
R72		—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R80	DSDI, DSCK set up	60.00	—	90.00	—	75.00	—	3.000	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns

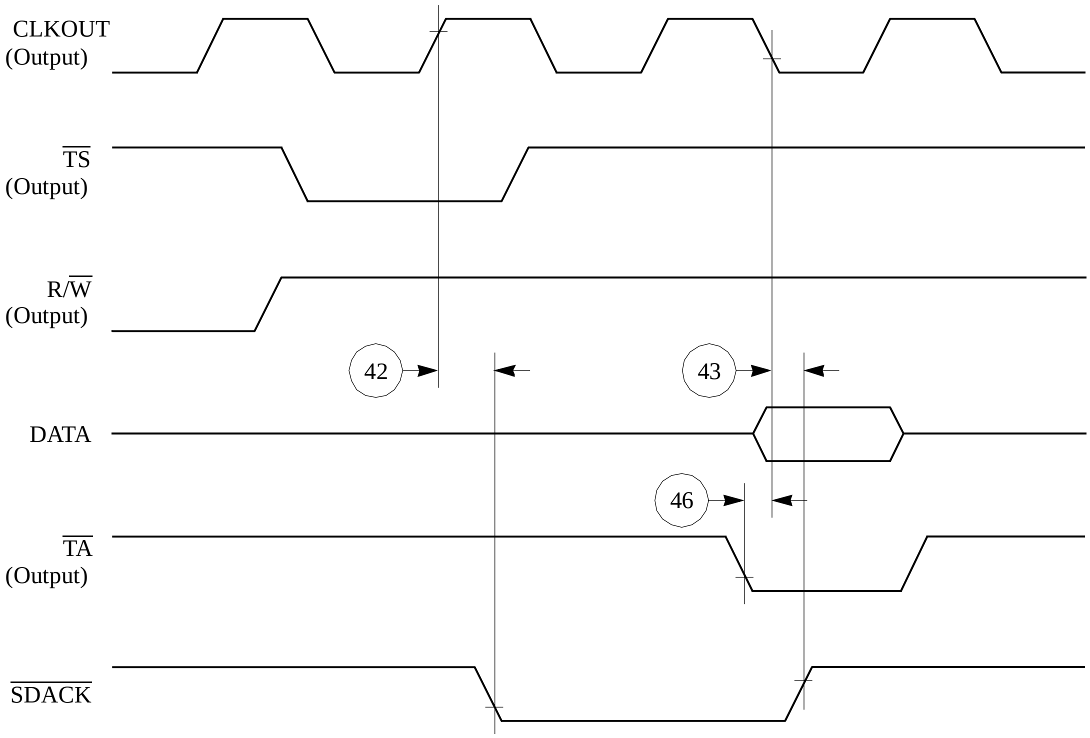


Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock

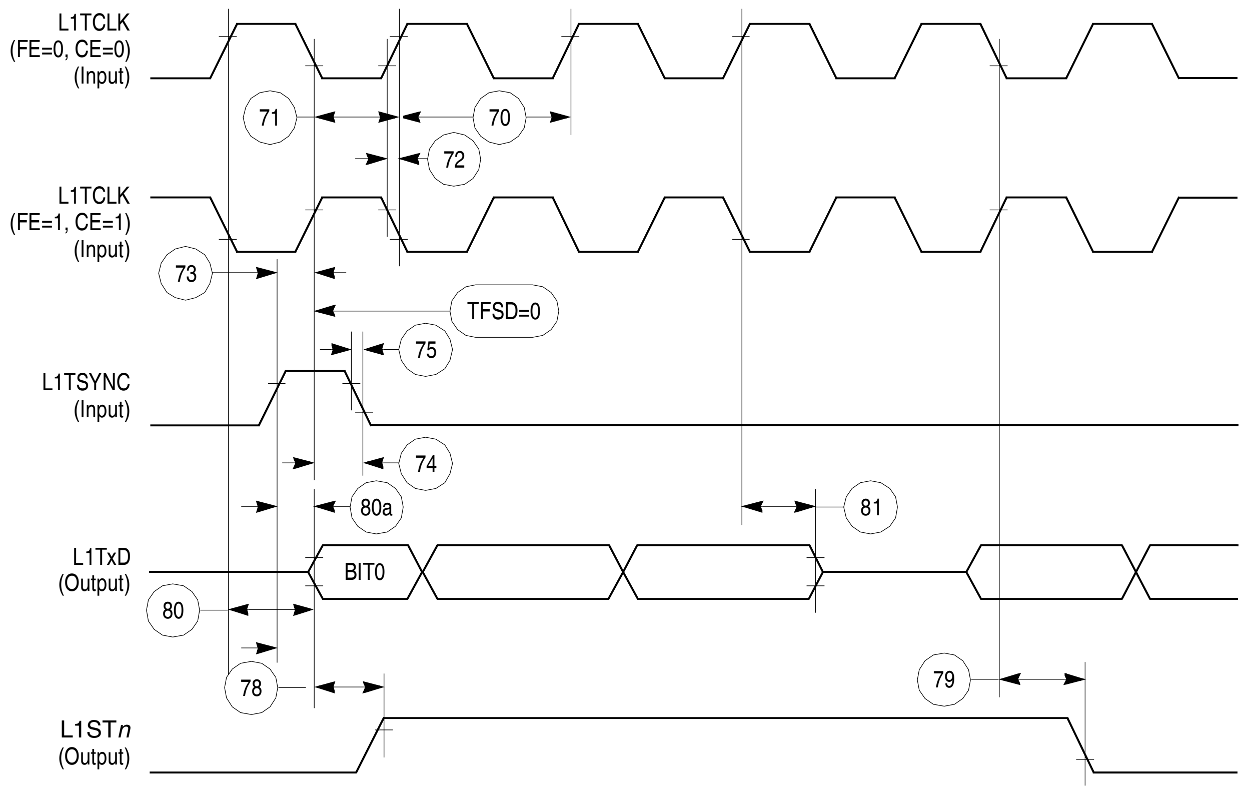


Figure 47. SI Transmit Timing Diagram

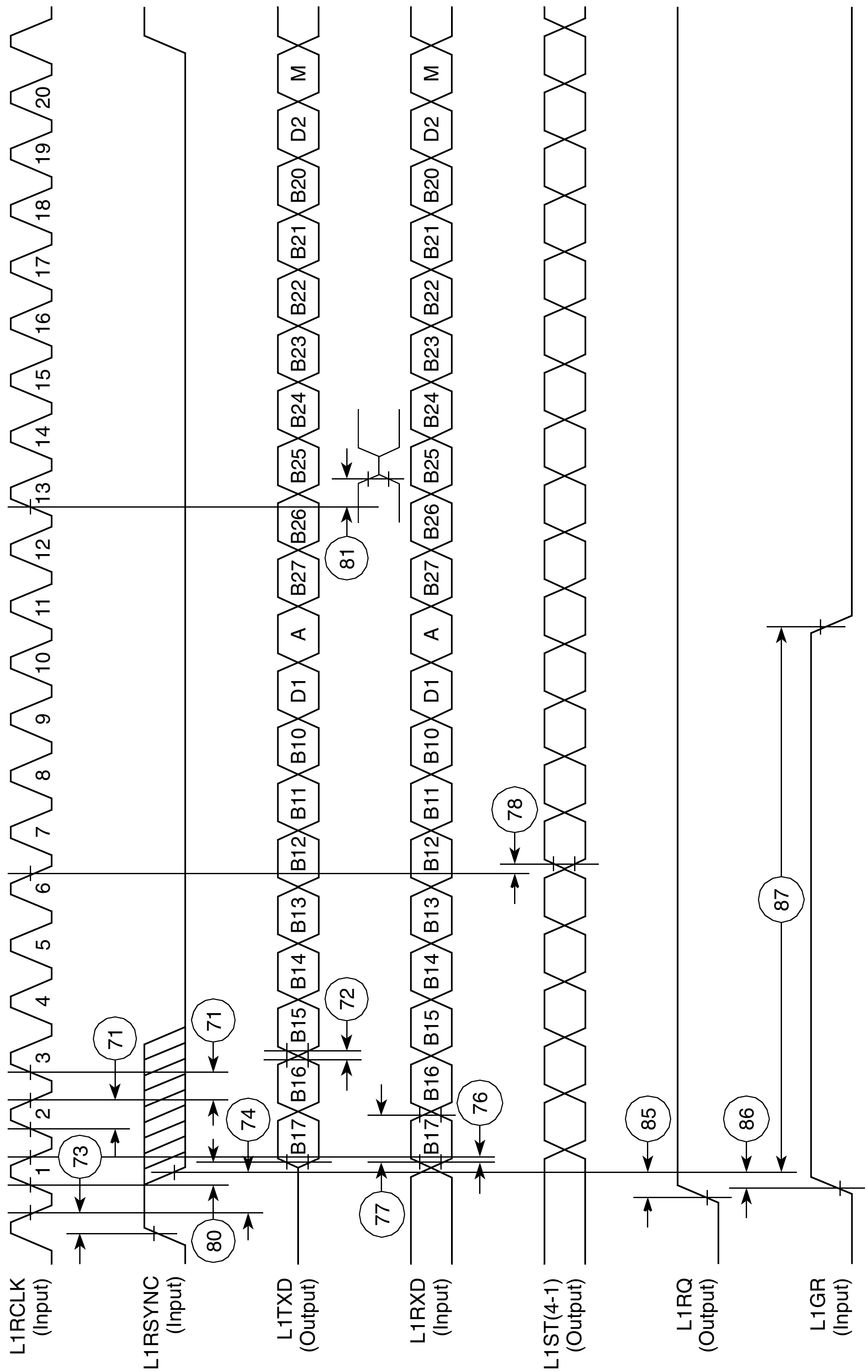


Figure 49. IDL Timing

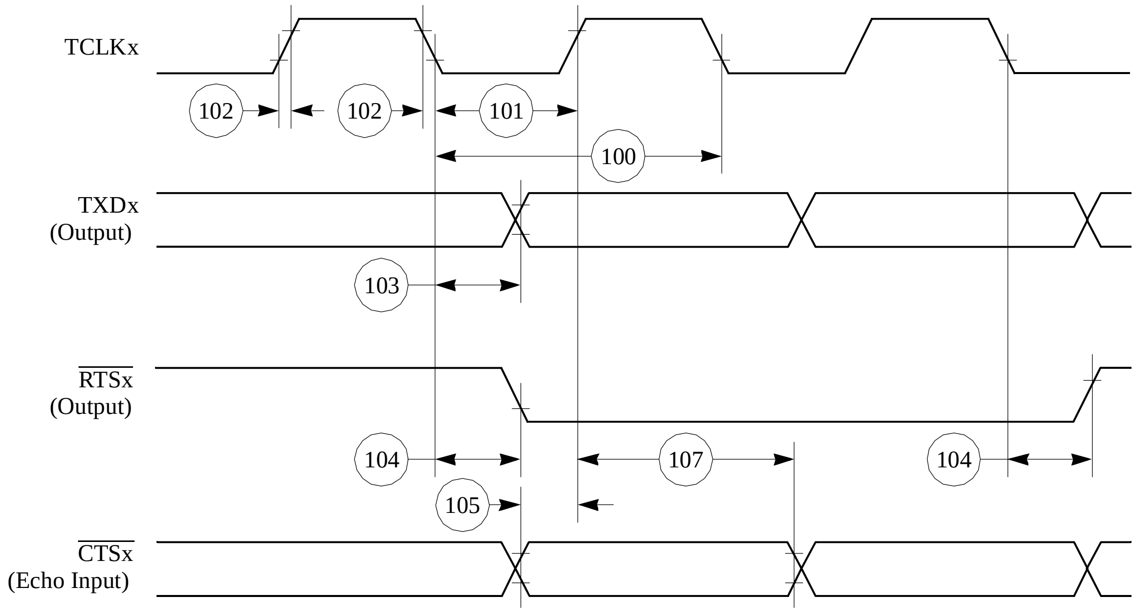


Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period [1]	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period[1]	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns

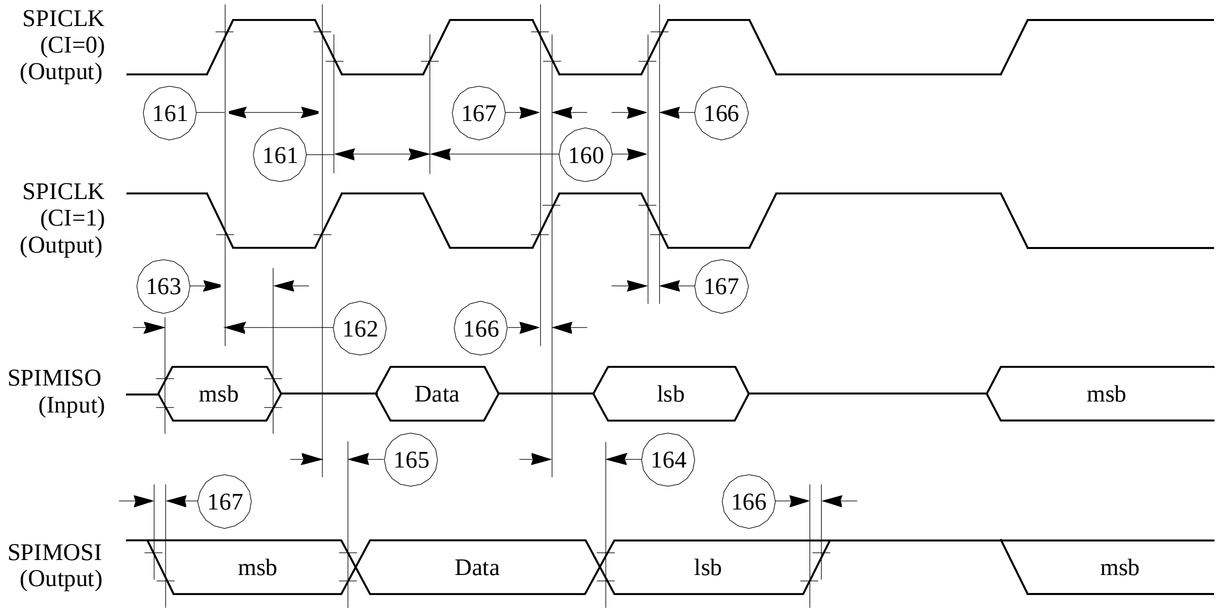


Figure 57. SPI Master (CP = 0) Timing Diagram

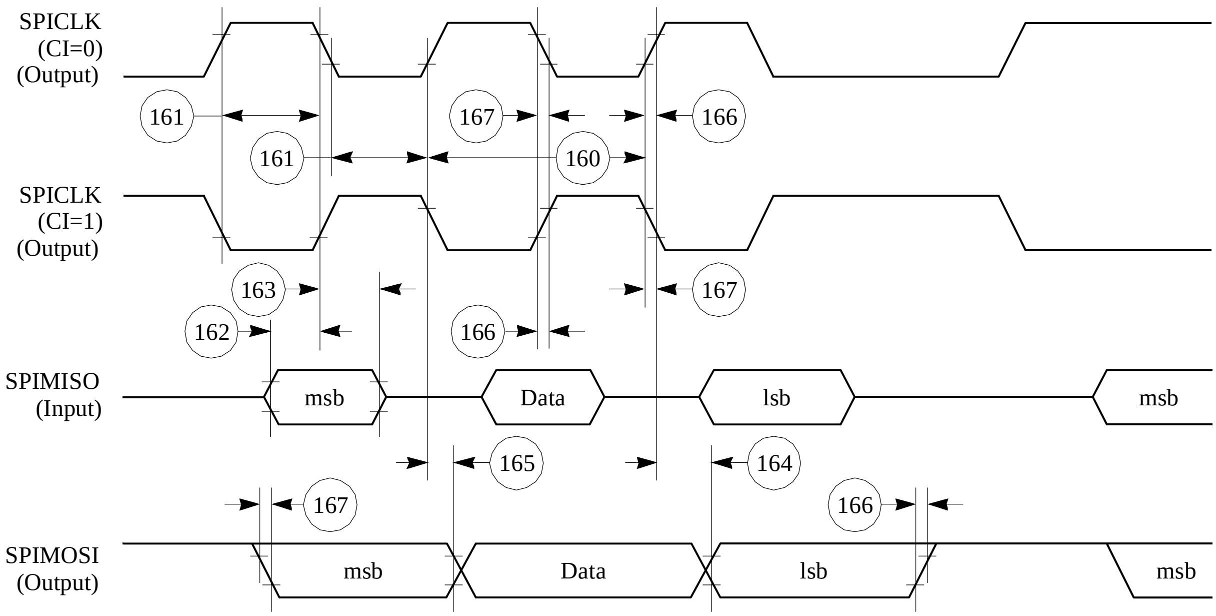


Figure 58. SPI Master (CP = 1) Timing Diagram

Table 24. I^{2}C Timing (SCL < 100 KHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300.00	ns
211	Stop condition setup time	4.70	—	µs

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I^{2}C (SCL > 100 KHz) timings.

Table 25. I^{2}C Timing (SCL > 100 KHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) [1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	s
203	Low period of SCL		1/(2.2 * fSCL)	—	s
204	High period of SCL		1/(2.2 * fSCL)	—	s
205	Start condition setup time		1/(2.2 * fSCL)	—	s
206	Start condition hold time		1/(2.2 * fSCL)	—	s
207	Data hold time		0	—	s
208	Data setup time		1/(40 * fSCL)	—	s
209	SDL/SCL rise time		—	1/(10 * fSCL)	s
210	SDL/SCL fall time		—	1/(33 * fSCL)	s
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

[1] SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 61 shows the I^{2}C bus timing.

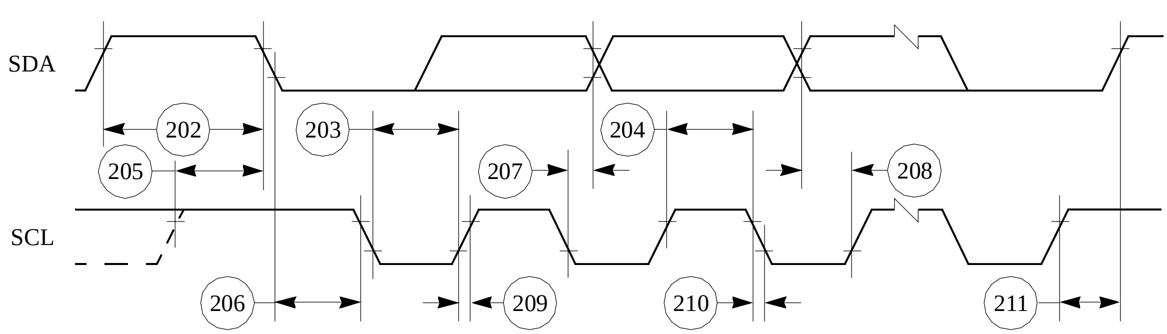


Figure 61. I^{2}C Bus Timing Diagram

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

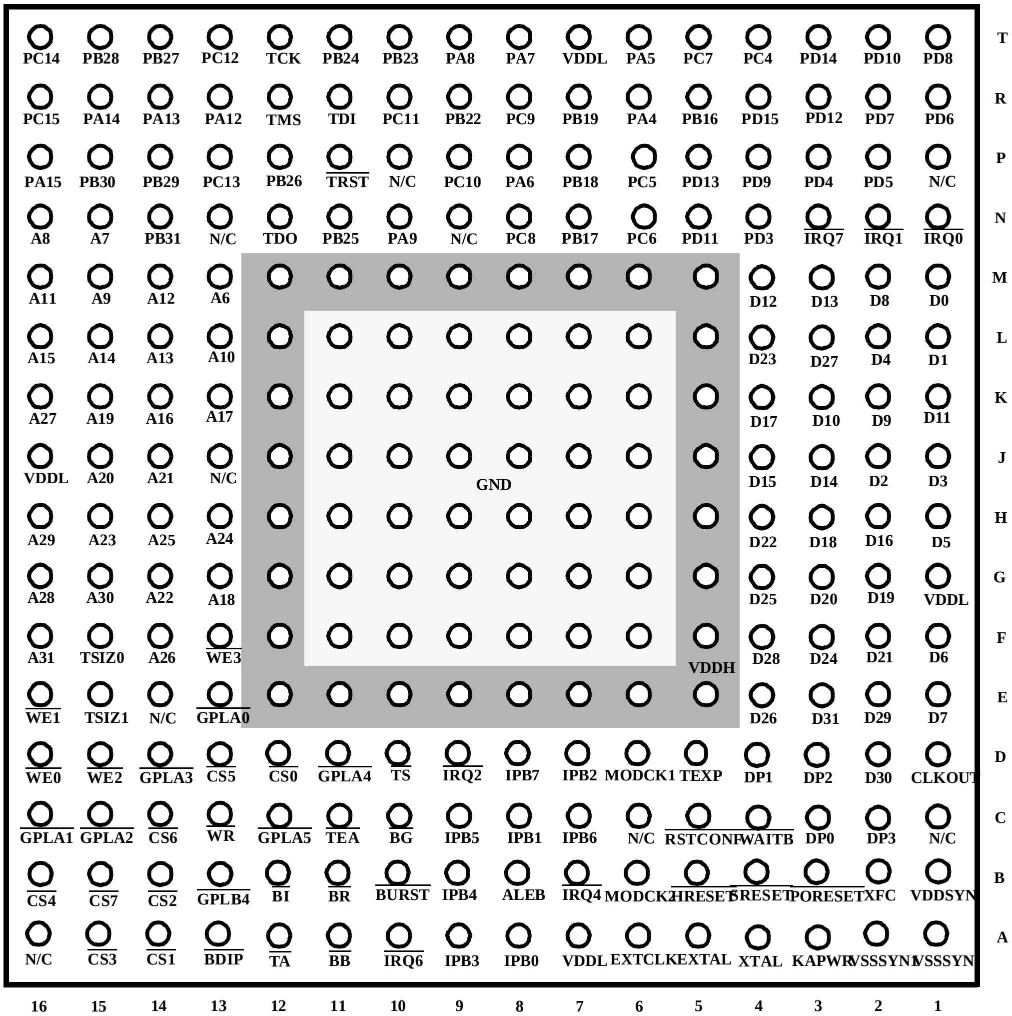


Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface.

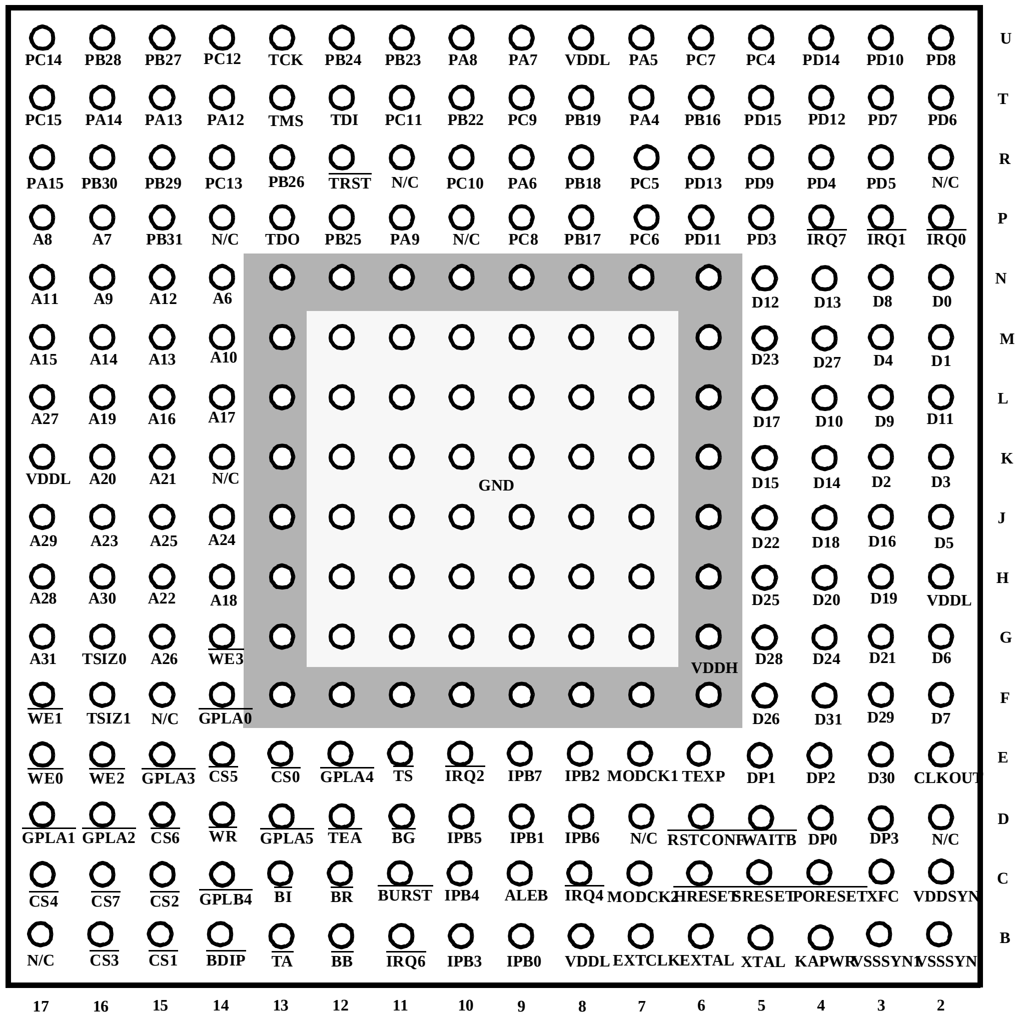
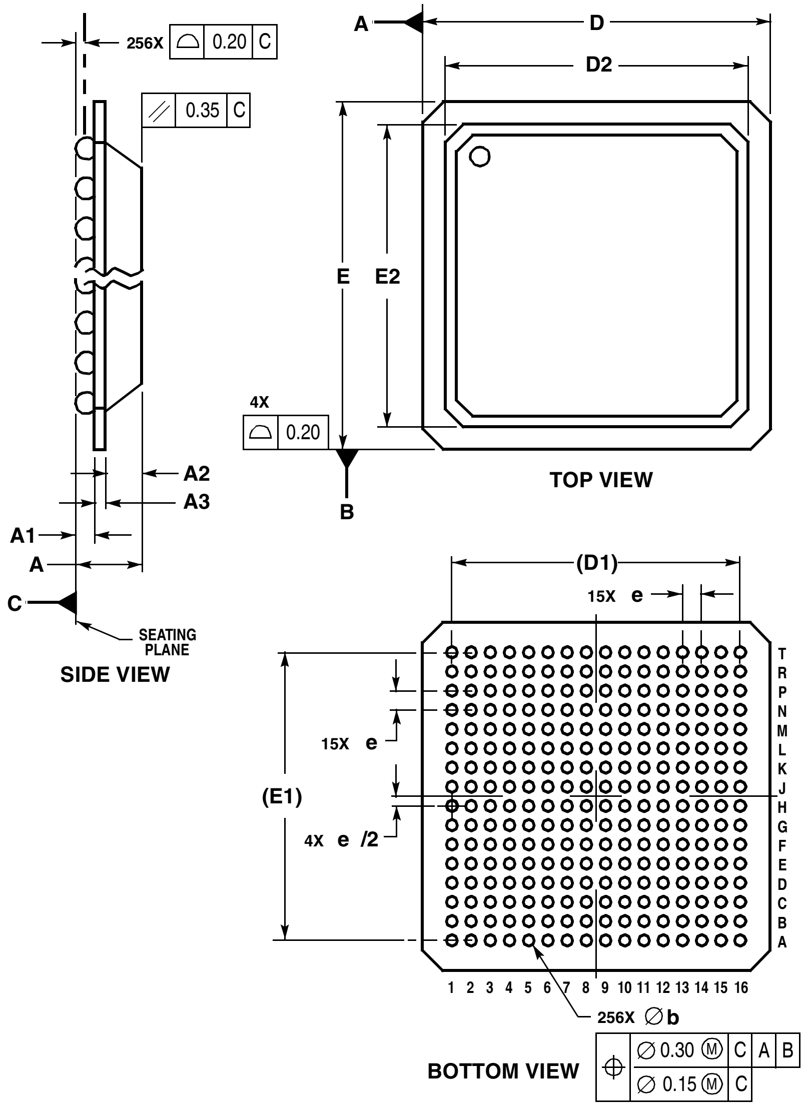


Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

Figure 64 shows the non-JEDEC package dimensions of the PBGA.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND THE SEATING PLANE ARE

	MILLIMETERS	
DIM	MIN	MAX
A	1.91	2.35
A1	0.50	0.70
A2	1.12	1.22
A3	0.29	0.43
b	0.60	0.90
D	23.00 BSC	
D1	19.05 REF	
D2	19.00	20.00
E	23.00 BSC	
E1	19.05 REF	
E2	19.00	20.00
e	1.27 BSC	

Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard

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