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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850srczq50bu

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Overview

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I²C port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Table 1. MPC850 Functionality Matrix

Additional documentation may be provided for parts listed in Table 1.





- Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
- Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface

(GND = 0V)

- Eight comparators: four operate on instruction address, two operate on data address, and two
 operate on data
- The MPC850 can compare using the =, \neq , <, and > conditions to generate watchpoints
- Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility on all general purpose I/O pins.

3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC850. Table 2 provides the maximum ratings.

Rating	Symbol	Value	Unit
Supply voltage	VDDH	-0.3 to 4.0	V
	VDDL	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	VDDSYN	-0.3 to 4.0	V
Input voltage ¹	V _{in}	GND-0.3 to VDDH + 2.5 V	V
Junction temperature ²	Тј	0 to 95 (standard) -40 to 95 (extended)	°C
Storage temperature range	T _{stg}	-55 to +150	°C

¹ Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. CAUTION: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction

applies to power-up and normal operation (that is, if the MPC850 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

² The MPC850, a high-frequency device in a BGA package, does not provide a guaranteed maximum ambient temperature. Only maximum junction temperature is guaranteed. It is the responsibility of the user to consider power dissipation and thermal management. Junction temperature ratings are the same regardless of frequency rating of the device.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}). Table 3 provides the package thermal characteristics for the MPC850.



Figure 4 provides the timing for the synchronous output signals.



Figure 4. Synchronous Output Signals Timing

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.



Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing





Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)



Table 8 shows the PCMCIA timing for the MPC850.

Table 8. PCMCIA Timing

Num	n Characteristic -		/IHz	66N	/IHz	80 I	MHz	FEACTOR	Unit
Num			Max	Min	Max	Min	Max	FREIGH	Unit
P44	A[6–31], REG valid to PCMCIA strobe asserted. ¹	13.00		21.00	—	17.00		0.750	ns
P45	A[6–31], REG valid to ALE negation. ¹	18.00	_	28.00	—	23.00	_	1.000	ns
P46	CLKOUT to REG valid	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P47	CLKOUT to REG Invalid.	6.00	_	9.00	—	7.00	_	0.250	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P50	CLKOUT to PCOE, IORD, PCWE, IOWR assert time.	_	11.00	_	11.00	_	11.00	—	ns
P51	CLKOUT to PCOE, IORD, PCWE, IOWR negate time.	2.00	11.00	2.00	11.00	2.00	11.00	—	ns
P52	CLKOUT to ALE assert time	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P53	CLKOUT to ALE negate time	_	13.00		16.00	_	14.00	0.250	ns
P54	PCWE, IOWR negated to D[0–31] invalid. ¹	3.00	_	6.00	_	4.00	_	0.250	ns
P55	WAIT_B valid to CLKOUT rising edge.1	8.00	_	8.00	_	8.00	_	—	ns
P56	CLKOUT rising edge to WAIT_B invalid. ¹	2.00	—	2.00	—	2.00	—	_	ns

¹ PSST = 1. Otherwise add PSST times cycle time.

PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAIT_B signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The WAIT_B assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC850 PowerQUICC User's Manual.





Figure 24 provides the PCMCIA access cycle timing for the external bus read.

Figure 24. PCMCIA Access Cycles Timing External Bus Read



Figure 31 shows the reset timing for the data bus configuration.



Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.



Figure 32. Reset Timing—Data Bus Weak Drive during Configuration







Figure 37. Boundary Scan (JTAG) Timing Diagram

8 **CPM Electrical Characteristics**

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC850.

8.1 PIO AC Electrical Specifications

Table 13 provides the parallel I/O timings for the MPC850 as shown in Figure 38.

Table 13. Parallel I/O Timing

Num	Characteristic	All Frequencies		Unit
Num	Unardetensite	Min Max	onit	
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	_	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns





Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock





Figure 49. IDL Timing





CPM Electrical Characteristics

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

	Table 18.	NMSI	External	Clock	Timing
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Num	Characteristic	All Frequencie	Unit	
Num	india characteristic		Max	Onit
100	RCLKx and TCLKx frequency 1 (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	_	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	RTSx active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	CTSx setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge ²	5.00	—	ns
108	CDx setup time to RCLKx rising edge	5.00	—	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Charactoristic	All Fr	equencies	Unit
Nulli	Characteristic	Min	Мах	onn
100	RCLKx and TCLKx frequency 1 (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time		—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	RTSx active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	CTSx setup time to TCLKx rising edge		—	ns
106	RXDx setup time to RCLKx rising edge		—	ns
107	RXDx hold time from RCLKx rising edge ²	0.00	—	ns
108	CDx setup time to RCLKx rising edge	40.00		ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.



CPM Electrical Characteristics

Figure 50 through Figure 52 show the NMSI timings.







1. This delay is equal to an integer number of character-length clocks.

Figure 56. SMC Transparent Timing Diagram

8.9 SPI Master AC Electrical Specifications

Table 22 provides the SPI master timings as shown in Figure 57 and Figure 58.

Num	Num Characteristic		iencies	Unit
Num	Characteristic	Min	Max	Unit
160	MASTER cycle time	4	1024	t _{cyc}
161	MASTER clock (SCK) high or low time	2	512	t _{cyc}
162	MASTER data setup time (inputs)	50.00	_	ns
163	Master data hold time (inputs)	0.00	_	ns
164	Master data valid (after SCK edge)	—	20.00	ns
165	65 Master data hold time (outputs)		_	ns
166	Rise time output	—	15.00	ns
167	Fall time output	—	15.00	ns

Table 22. SPI Master Timing



CPM Electrical Characteristics









8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

Table 23. SPI Slave Timing

Num	Num Characteristic		All Frequencies	
Nulli	Characteristic	Min	Max	Onit
170	Slave cycle time	2	—	t _{cyc}
171	Slave enable lead time	15.00	_	ns
172	Slave enable lag time	15.00	_	ns
173	Slave clock (SPICLK) high or low time		_	t _{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	_	t _{cyc}
175	Slave data setup time (inputs)	20.00	—	ns
176	Slave data hold time (inputs)	20.00	—	ns
177	Slave access time		50.00	ns
178	Slave SPI MISO disable time	_	50.00	ns
179	Slave data valid (after SPICLK edge)		50.00	ns
180	Slave data hold time (outputs)		_	ns
181	Rise time (input)	_	15.00	ns
182	Fall time (input)	_	15.00	ns



CPM Electrical Characteristics



Figure 60. SPI Slave (CP = 1) Timing Diagram

8.11 I²C AC Electrical Specifications

Table 24 provides the I^2C (SCL < 100 KHz) timings.

Table 24.	I ² C Timing	(SCL < 100 KHz)
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Num	Charactoristia	All Frequencies		Unit
		Min	Max	onit
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) ¹	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	—	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	_	ns
209	SDL/SCL rise time	—	1.00	μs



9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivativ

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

 Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support



Document Revision History

10 Document Revision History

Table 28 lists significant changes between revisions of this document.

Table 28. Document Revision History

Revision	Date	Change
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.
0.2	04/2002	Updated power numbers and added Rev. C
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.



Document Revision History

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