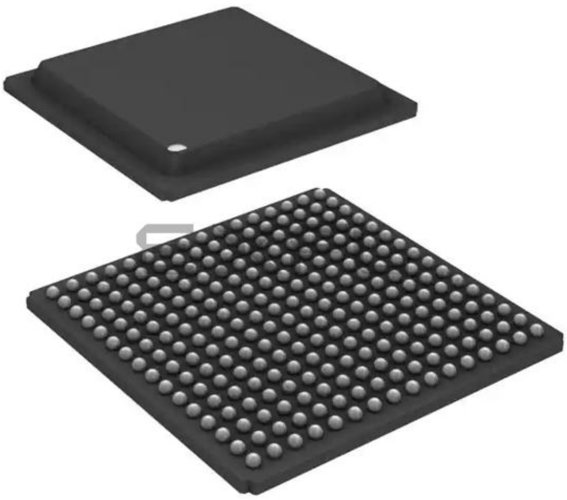

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850srczq66bu

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I^2C port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

Table 1. MPC850 Functionality Matrix

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Additional documentation may be provided for parts listed in Table 1.

- QUICC multichannel controller (QMC) microcode features
  - Up to 64 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
  - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One $I^2C^{®}$ (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and CPM in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation

Table 6. Bus Operation Timing [1]

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B1	CLKOUT period	20	—	30.30	—	25	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	—	50.00	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	—	50.00	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) [2]	-0.60	0.60	-0.60	0.60	-0.60	0.60	—	50.00	ns
B1d	CLKOUT phase jitter [2]	-2.00	2.00	-2.00	2.00	-2.00	2.00	—	50.00	ns
B1e	CLKOUT frequency jitter (MF < 10) [2]	—	0.50	—	0.50	—	0.50	—	50.00	%
B1f	CLKOUT frequency jitter (10 < MF < 500) [2]	—	2.00	—	2.00	—	2.00	—	50.00	%
B1g	CLKOUT frequency jitter (MF > 500) [2]	—	3.00	—	3.00	—	3.00	—	50.00	%
B1h	Frequency jitter on EXTCLK [3]	—	0.50	—	0.50	—	0.50	—	50.00	%
B2	CLKOUT pulse width low	8.00	—	12.12	—	10.00	—	—	50.00	ns
B3	CLKOUT width high	8.00	—	12.12	—	10.00	—	—	50.00	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B7	CLKOUT to A[6–31], RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3] invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7a	CLKOUT to TSIZ[0–1], $\overline{REG}$, $\overline{RSV}$, AT[0–3], $\overline{BDIP}$, PTR invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS[0–1], VF[0–2] IWP[0–2], LWP[0–1], $\overline{STS}$ invalid [4]	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B8	CLKOUT to A[6–31], RD/$\overline{WR}$, $\overline{BURST}$, D[0–31], DP[0–3] valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8a	CLKOUT to TSIZ[0–1], $\overline{REG}$, $\overline{RSV}$, AT[0–3] $\overline{BDIP}$, PTR valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS[0–1], VF[0–2], IWP[0–2], FRZ, LWP[0–1], $\overline{STS}$ valid [4]	5.00	11.74	7.58	14.33	6.25	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	TBD	—	—	50.00	ns

1 The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR)$$

For maxima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR) + 1ns(CAP\ LOAD - 50) / 10$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

D_{50} is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

2 Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.

3 If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

4 The timing for $\overline{BR}$ output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC850 is selected to work with internal bus arbiter.

5 The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).

6 The timing required for $\overline{BR}$ input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC850 is selected to work with the external bus arbiter.

7 The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

8 The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

9 The timing B30 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE[0:3]}$ when CSNT = '0'.

10 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.

11 The $\overline{AS}$ signal is considered asynchronous to CLKOUT.

Figure 2 is the control timing diagram.

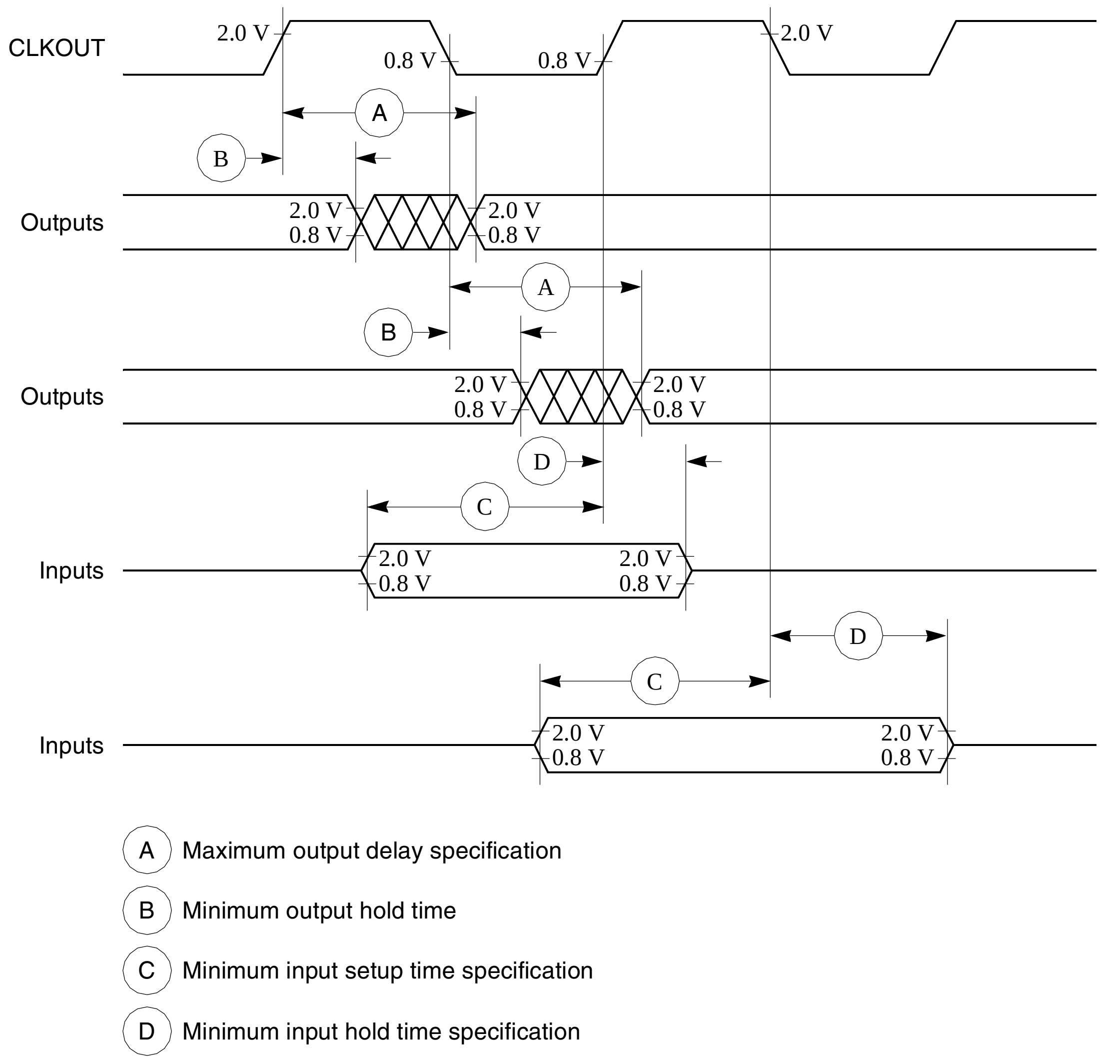

Figure 2. Control Timing

Figure 3 provides the timing for the external clock.

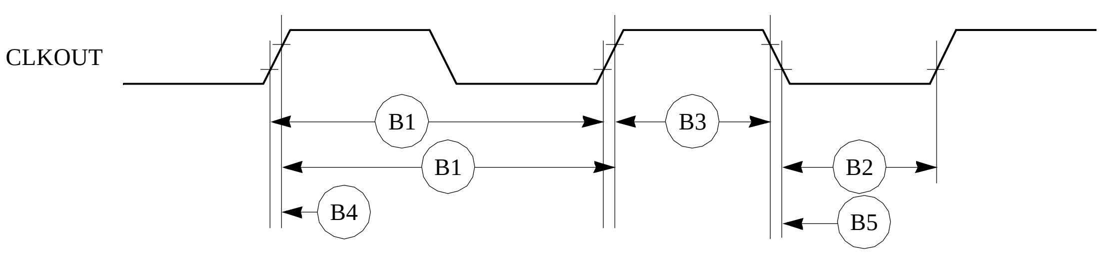

Figure 3. External Clock Timing

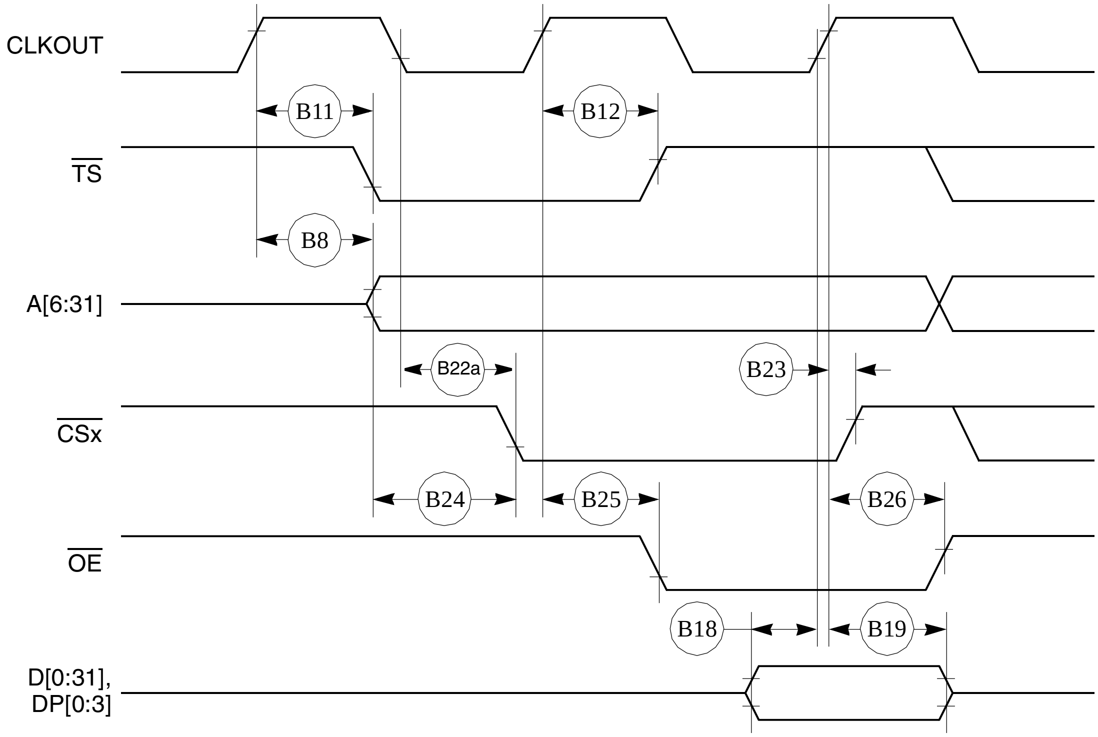

Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

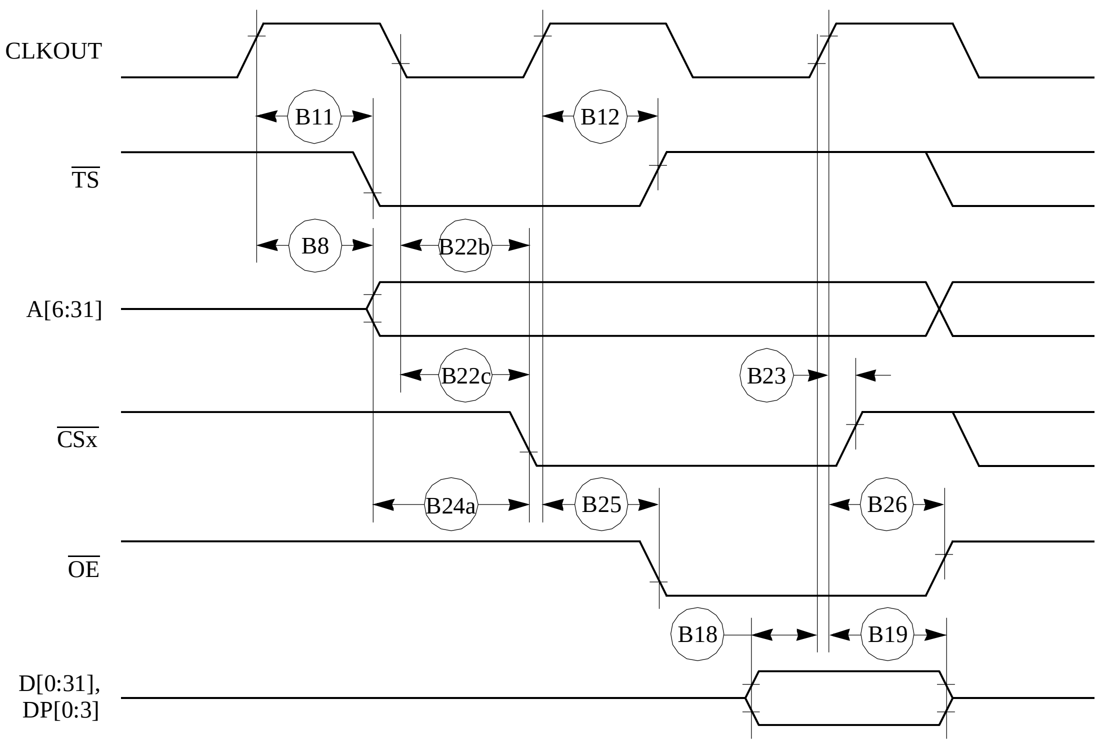

Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

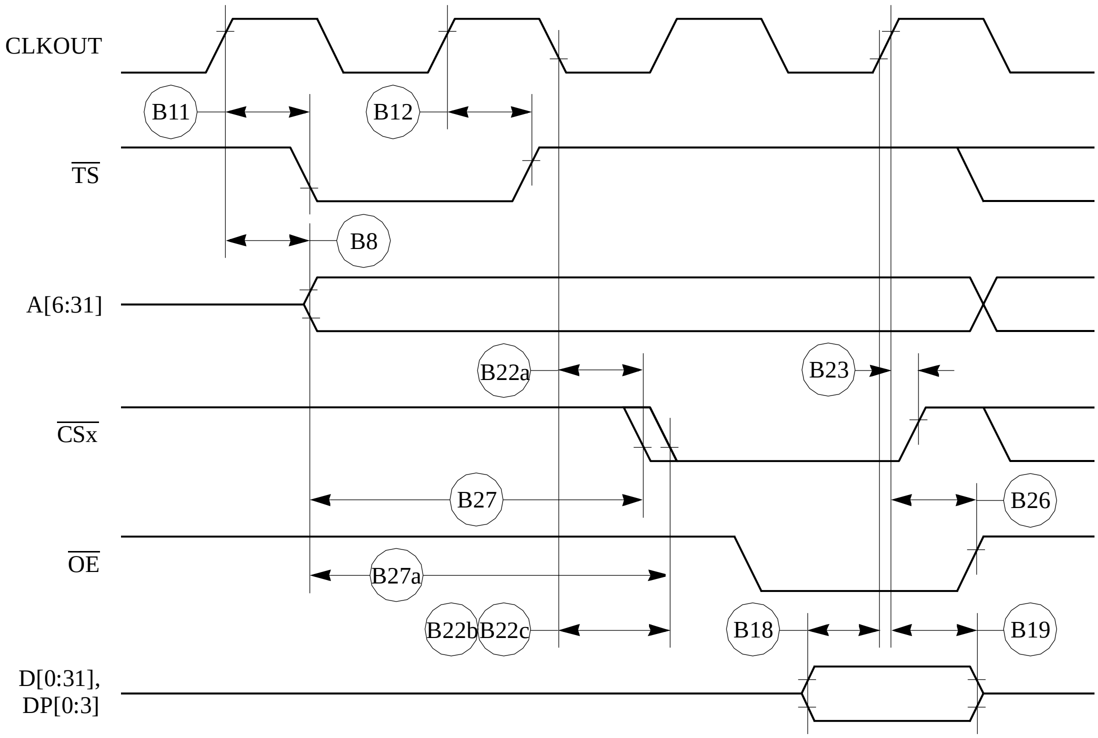

Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

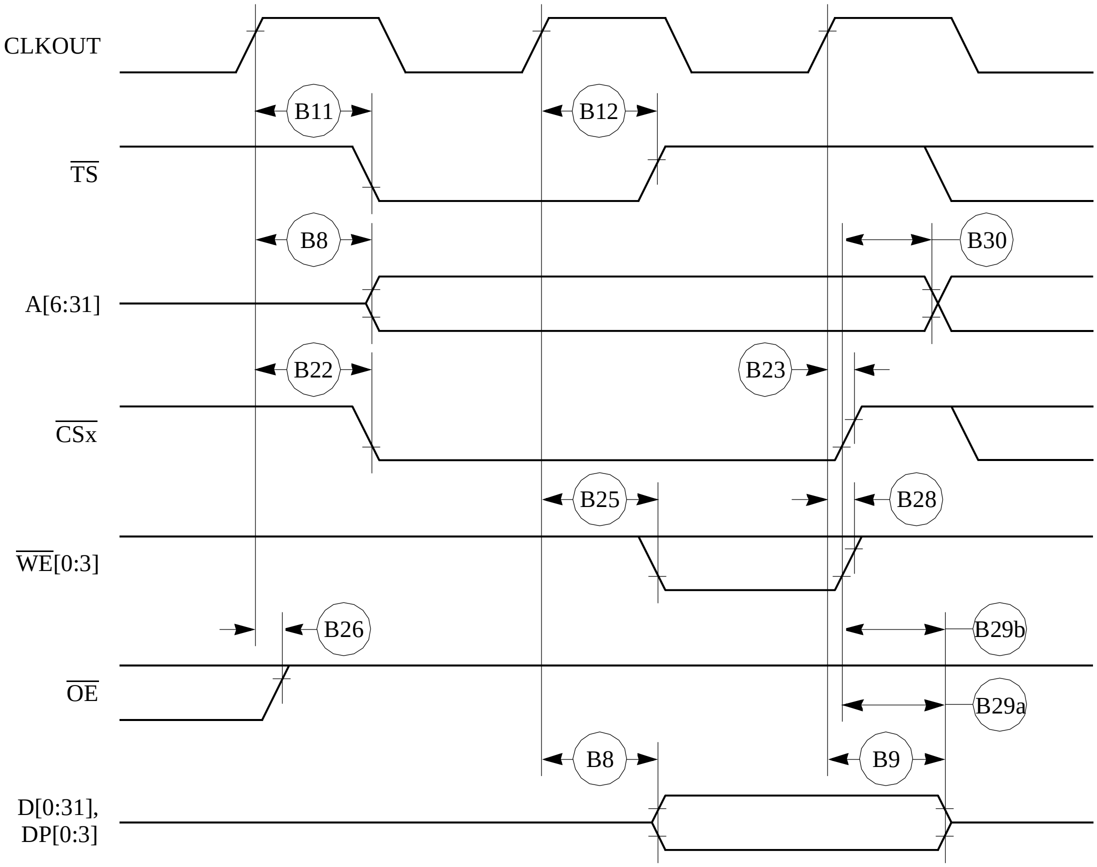

Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

Table 7 provides interrupt timing for the MPC850.

Table 7. Interrupt Timing

Num	Characteristic [1]	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
I39	$\overline{IRQx}$ valid to CLKOUT rising edge (set up time)	6.00	—	6.00	—	6.00	—	ns
I40	$\overline{IRQx}$ hold time after CLKOUT.	2.00	—	2.00	—	2.00	—	ns
I41	$\overline{IRQx}$ pulse width low	3.00	—	3.00	—	3.00	—	ns
I42	$\overline{IRQx}$ pulse width high	3.00	—	3.00	—	3.00	—	ns
I43	$\overline{IRQx}$ edge-to-edge time	80.00	—	121.0	—	100.0	—	ns

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.

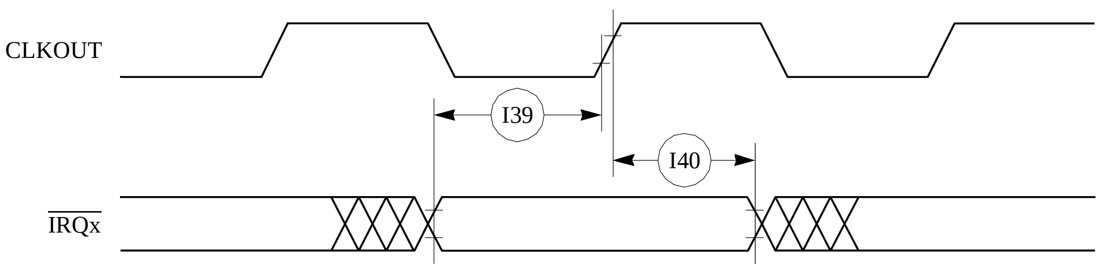

Figure 22. Interrupt Detection Timing for External Level Sensitive Lines

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.

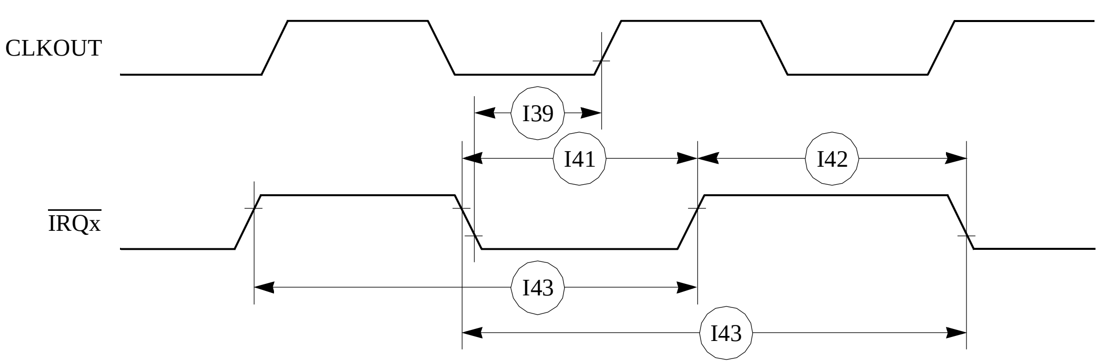

Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

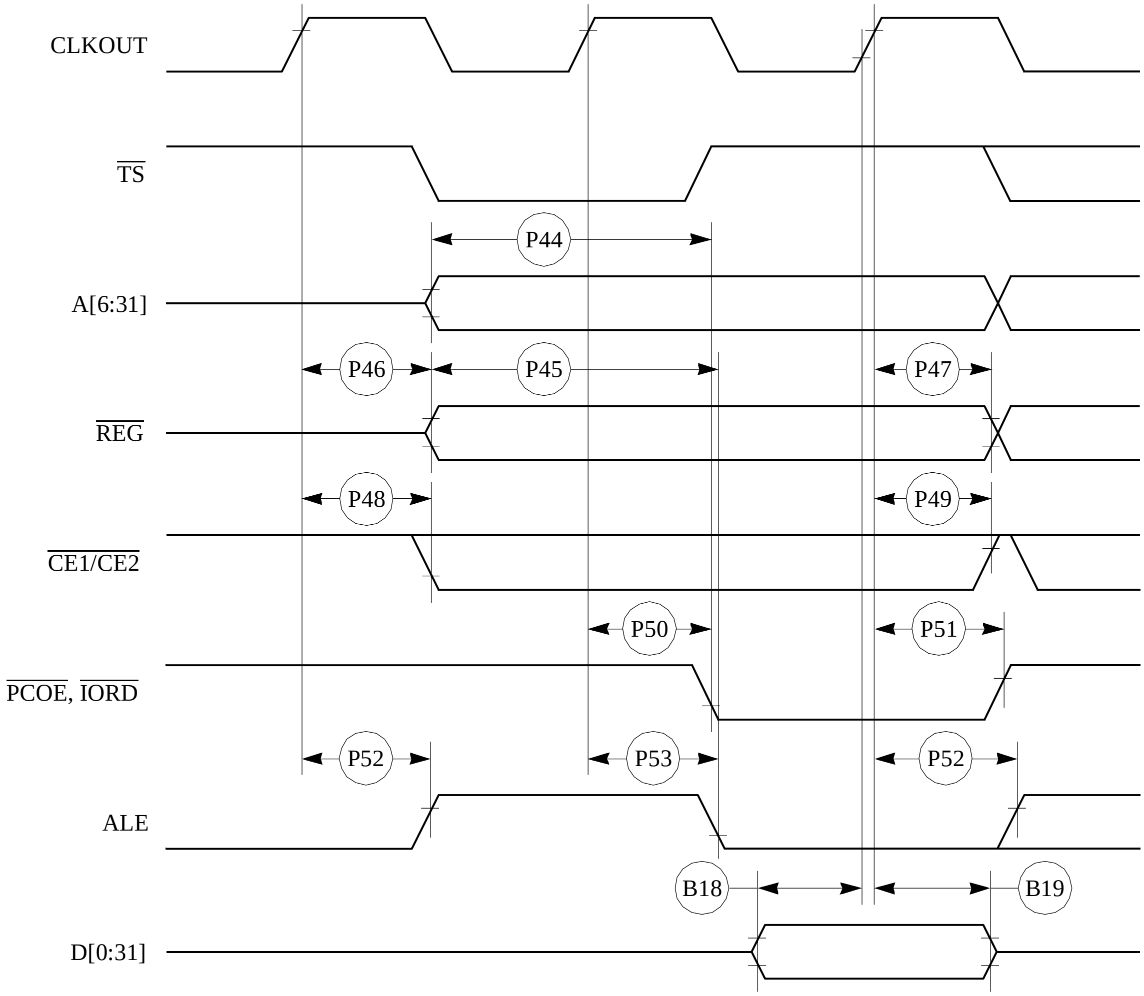

Figure 24. PCMCIA Access Cycles Timing External Bus Read

Table 9 shows the PCMCIA port timing for the MPC850.

Table 9. PCMCIA Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive [1]	18.00	—	26.00	—	22.00	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

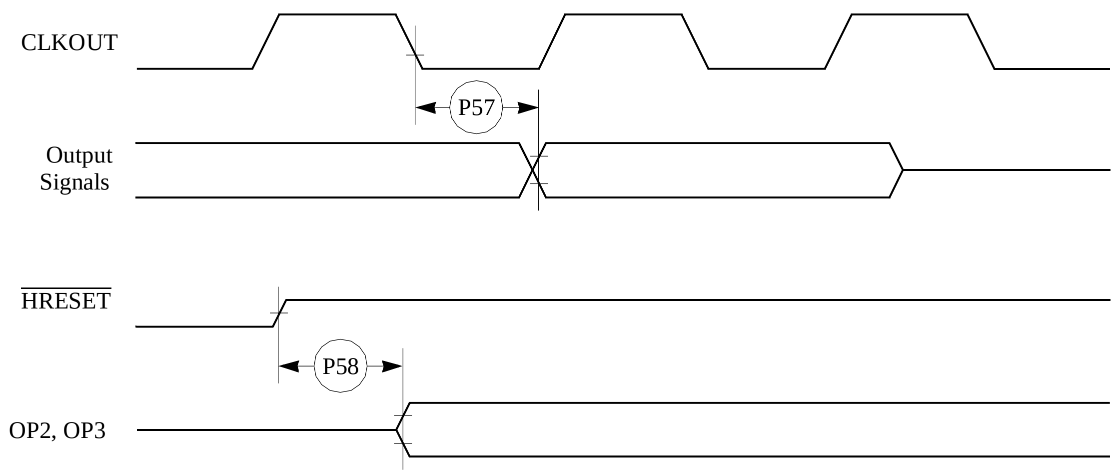

Figure 27. PCMCIA Output Port Timing

Figure 28 provides the PCMCIA output port timing for the MPC850.

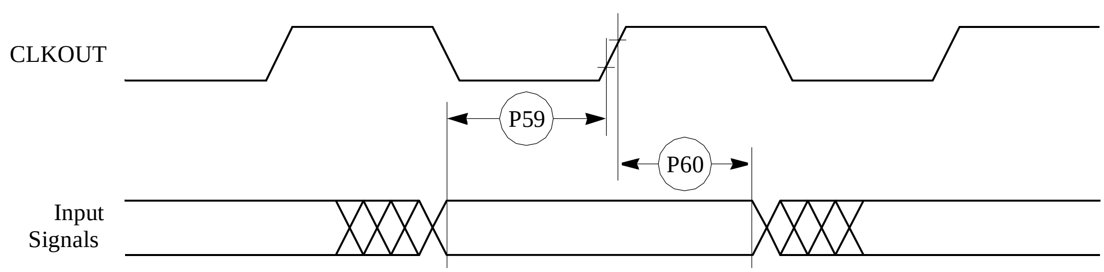

Figure 28. PCMCIA Input Port Timing

Table 10 shows the debug port timing for the MPC850.

Table 10. Debug Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
D61	DSCK cycle time	60.00	—	91.00	—	75.00	—	ns
D62	DSCK clock pulse width	25.00	—	38.00	—	31.00	—	ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	8.00	—	8.00	—	ns
D65	DSDI data hold time	5.00	—	5.00	—	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	0.00	2.00	ns

Figure 29 provides the input timing for the debug port clock.

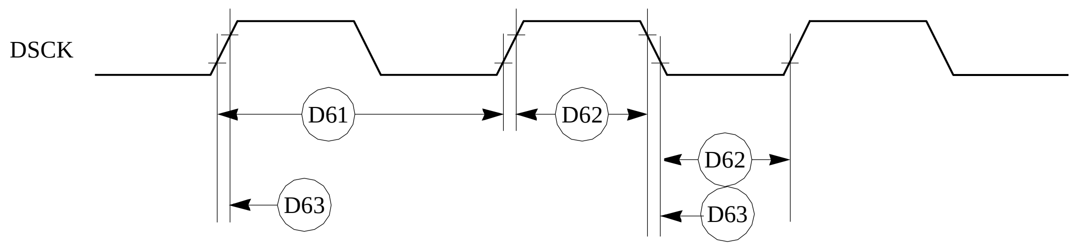

Figure 29. Debug Port Clock Input Timing

Figure 30 provides the timing for the debug port.

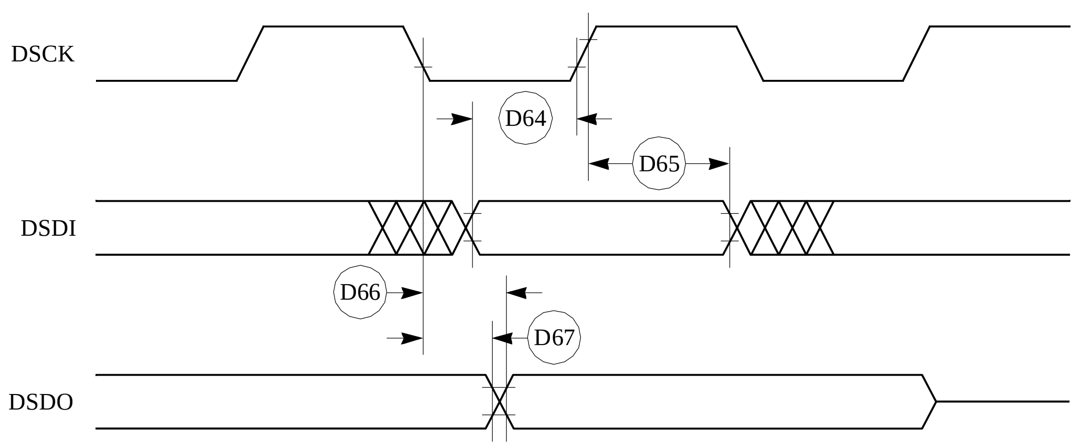

Figure 30. Debug Port Timings

Figure 33 provides the reset timing for the debug port configuration.

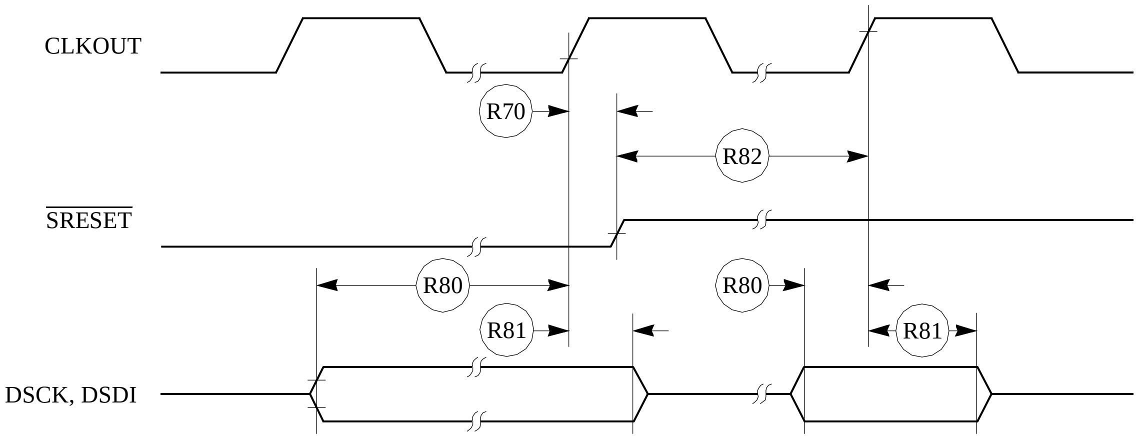

Figure 33. Reset Timing—Debug Port Configuration

7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

Table 12. JTAG Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
J82	TCK cycle time	100.00	—	100.00	—	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	40.00	—	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	5.00	—	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	25.00	—	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	—	27.00	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	0.00	—	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	—	20.00	—	20.00	ns
J90	TRST assert time	100.00	—	100.00	—	100.00	—	ns
J91	TRST setup time to TCK low	40.00	—	40.00	—	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	—	50.00	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	—	50.00	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	—	50.00	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	50.00	—	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	50.00	—	50.00	—	ns

8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns

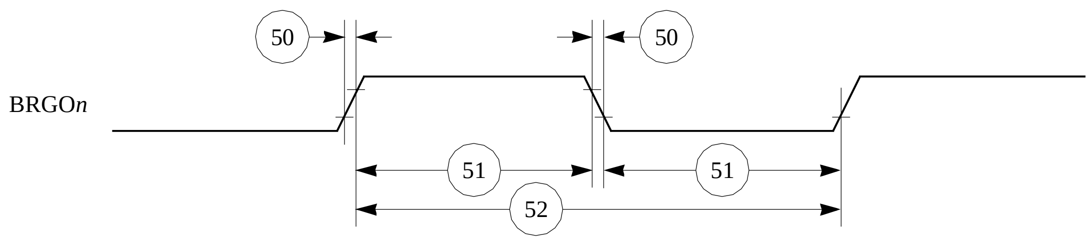

Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Table 16. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10.00	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1.00	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2.00	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3.00	—	clk
65	CLKO high to $\overline{\text{TOUT}}$ valid	3.00	25.00	ns

Table 17. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83A	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

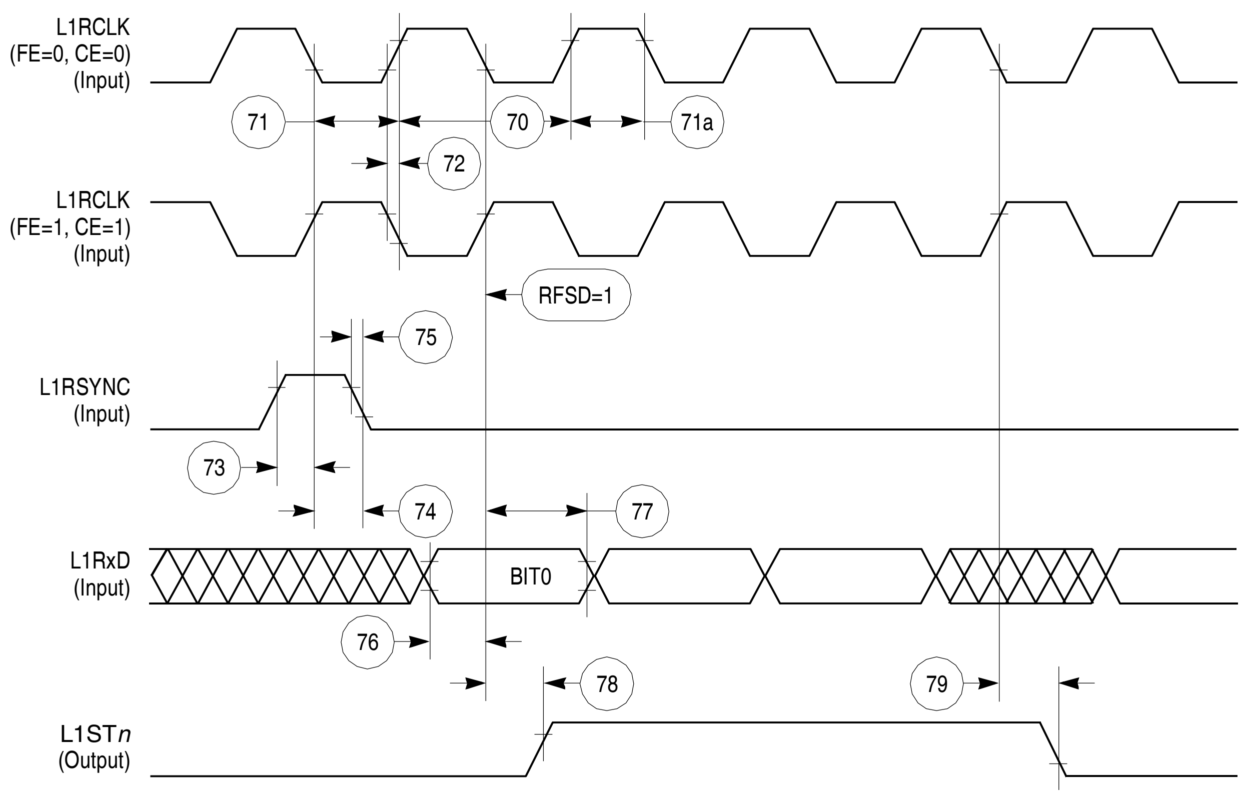

Figure 45. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

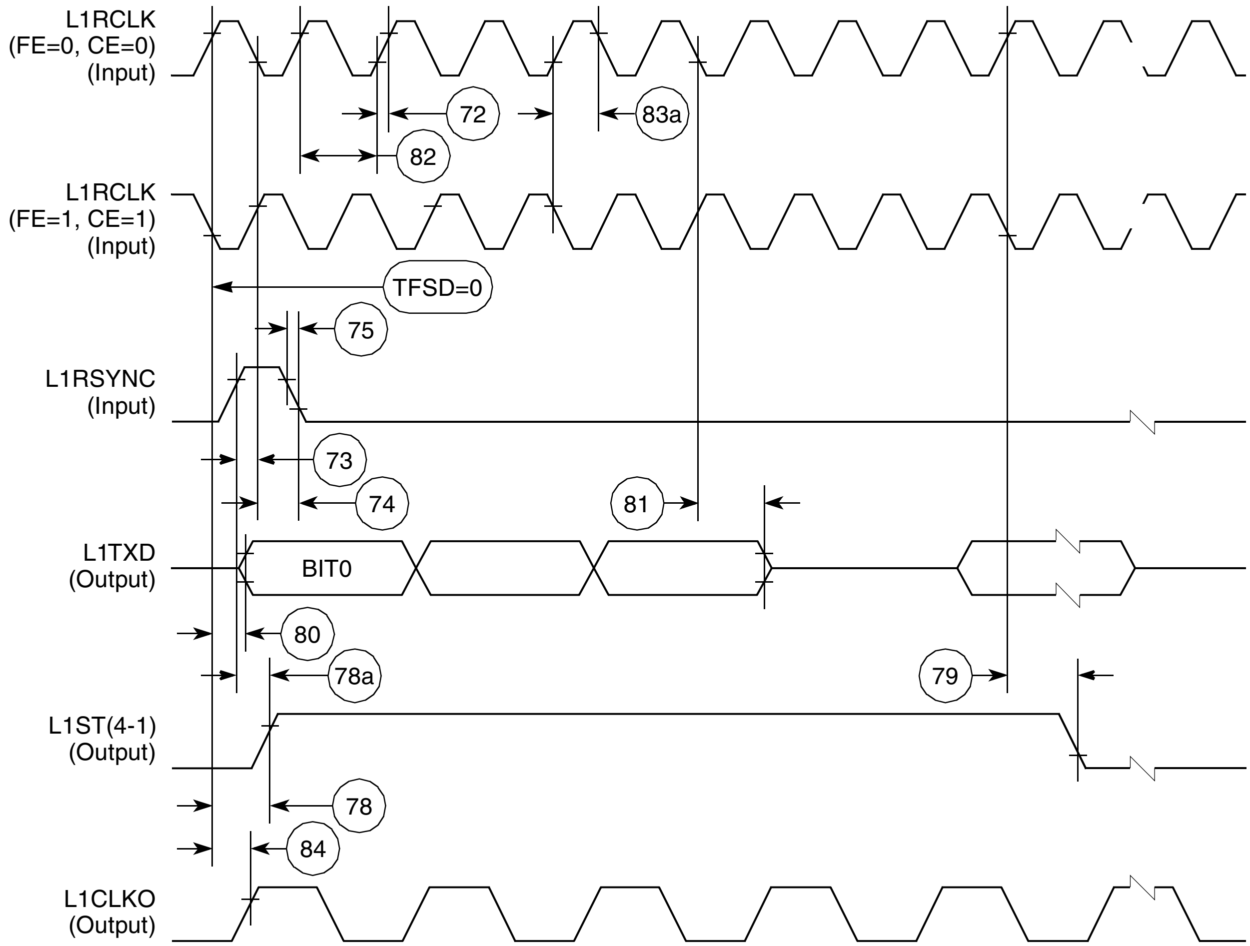

Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

Table 18. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	—	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge [2]	5.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	5.00	—	ns

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time	—	—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	40.00	—	ns
106	RXDx setup time to RCLKx rising edge	40.00	—	ns
107	RXDx hold time from RCLKx rising edge [2]	0.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	40.00	—	ns

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Figure 50 through Figure 52 show the NMSI timings.

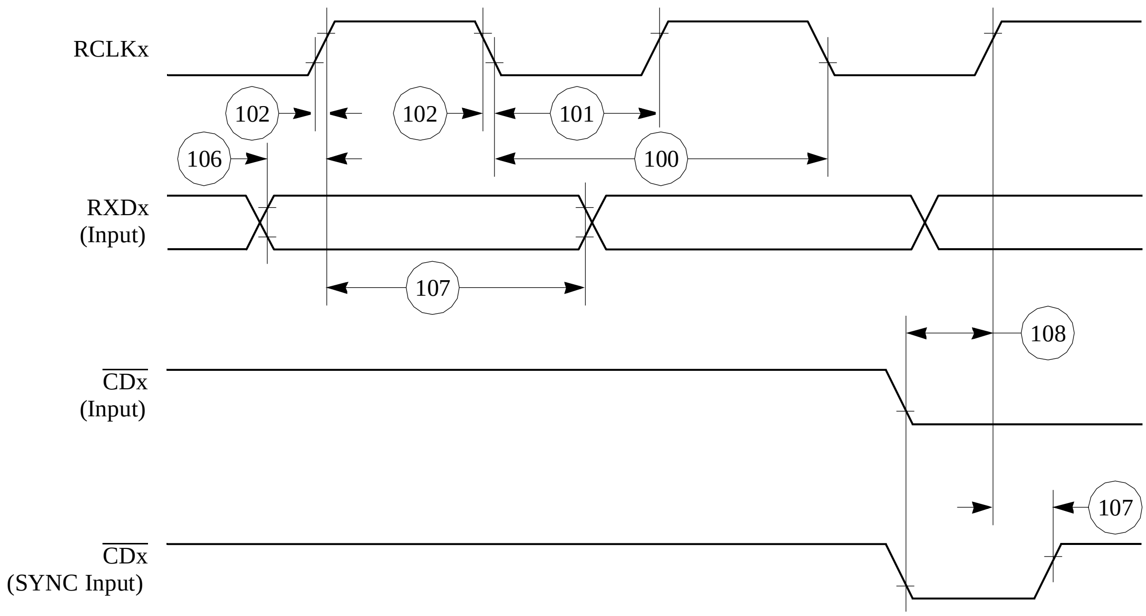

Figure 50. SCC NMSI Receive Timing Diagram

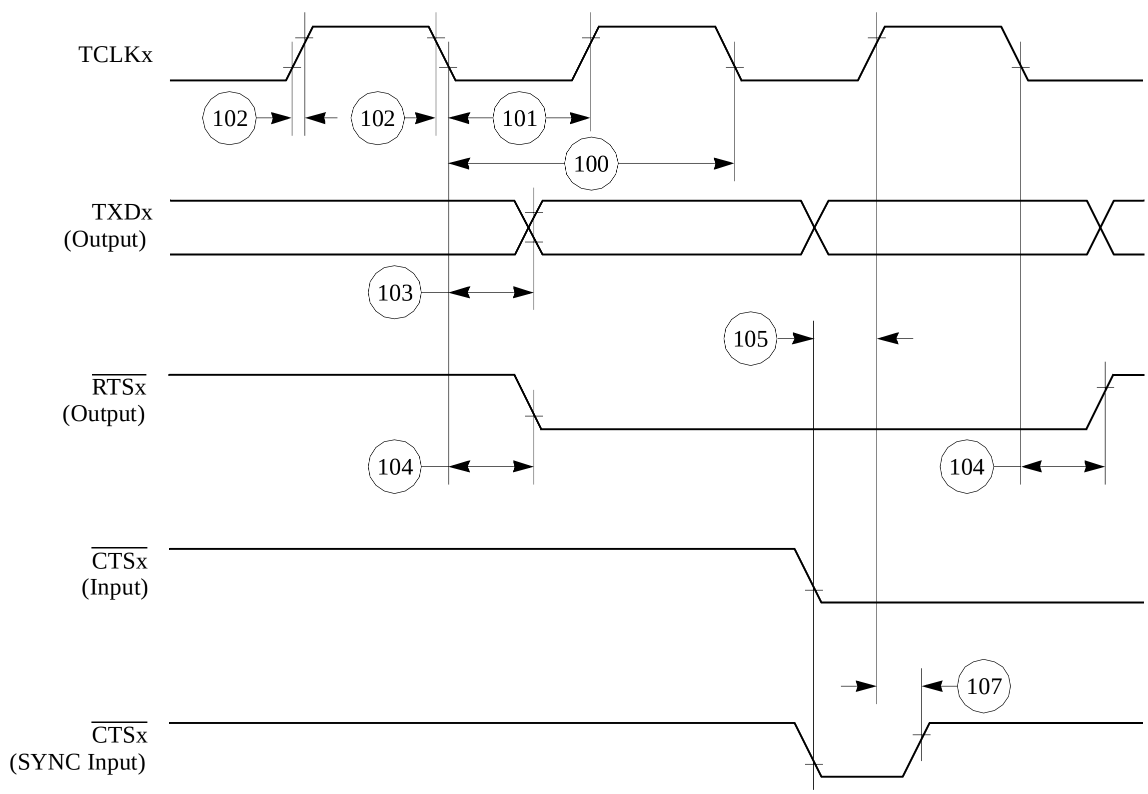

Figure 51. SCC NMSI Transmit Timing Diagram

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Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
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