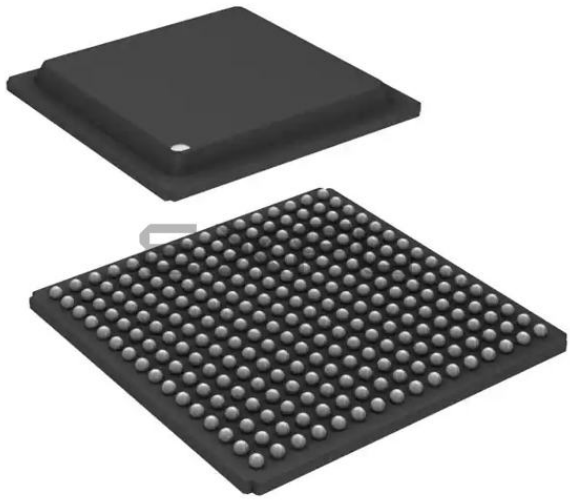

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 66MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 256-BBGA |
| Supplier Device Package | 256-PBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850srvr66bu |

  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

$\theta_{JA}$ = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between $P_D$ and $T_J$ is:

$P_D = K \div (T_J + 273°C)$(2)

Solving equations (1) and (2) for K gives:

$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$(3)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 5.1 Layout Practices

Each $V_{CC}$ pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{CC}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$ and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B22 | CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B22a | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0,1 | — | 8.00 | — | 8.00 | — | 8.00 | — | 50.00 | ns |
| B22b | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 | 5.00 | 11.75 | 7.58 | 14.33 | 6.25 | 13.00 | 0.250 | 50.00 | ns |
| B22c | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 | 7.00 | 14.00 | 11.00 | 18.00 | 9.00 | 16.00 | 0.375 | 50.00 | ns |
| B23 | CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | — | 50.00 | ns |
| B24 | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0. | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B24a | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B25 | CLKOUT rising edge to $\overline{OE}$, $\overline{WE[0–3]}$ asserted | — | 9.00 | — | 9.00 | — | 9.00 | — | 50.00 | ns |
| B26 | CLKOUT rising edge to $\overline{OE}$ negated | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | — | 50.00 | ns |
| B27 | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 | 23.00 | — | 36.00 | — | 29.00 | — | 1.250 | 50.00 | ns |
| B27a | A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B28 | CLKOUT rising edge to $\overline{WE[0–3]}$ negated GPCM write access CSNT = 0 | — | 9.00 | — | 9.00 | — | 9.00 | — | 50.00 | ns |
| B28a | CLKOUT falling edge to $\overline{WE[0–3]}$ negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B28b | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | — | 12.00 | — | 14.00 | — | 13.00 | 0.250 | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B31 | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |
| B31a | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B31b | CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | — | 50.00 | ns |
| B31c | CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B31d | CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 | 9.00 | 14.00 | 13.00 | 18.00 | 11.00 | 16.00 | 0.375 | 50.00 | ns |
| B32 | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |
| B32a | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B32b | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | — | 50.00 | ns |
| B32c | CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B32d | CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 | 9.00 | 14.00 | 13.00 | 18.00 | 11.00 | 16.00 | 0.375 | 50.00 | ns |
| B33 | CLKOUT falling edge to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |

Figure 4 provides the timing for the synchronous output signals.

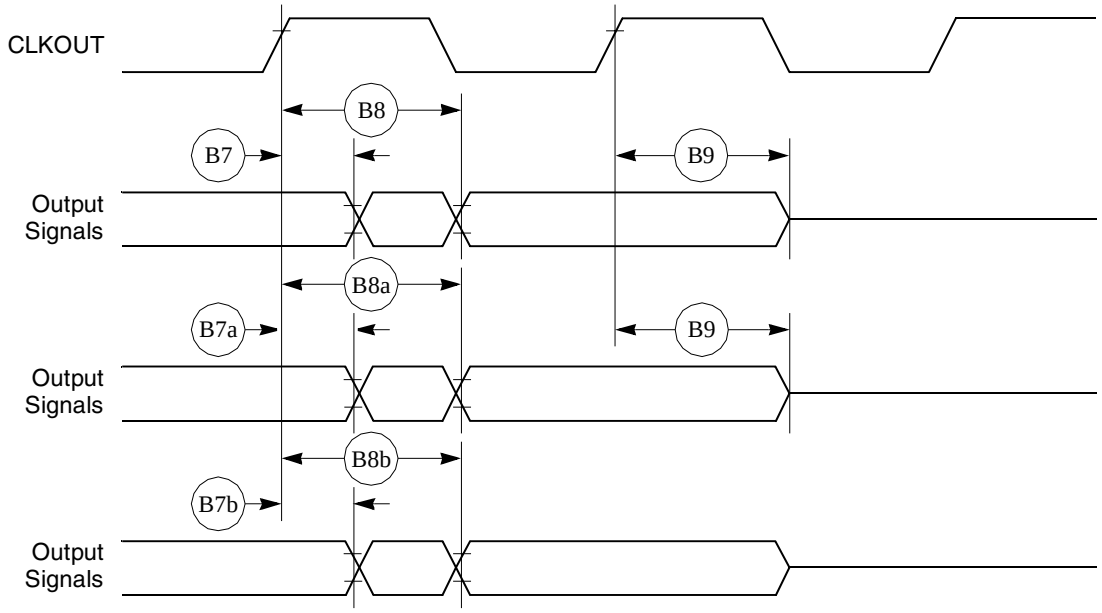


**Figure 4. Synchronous Output Signals Timing**

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.

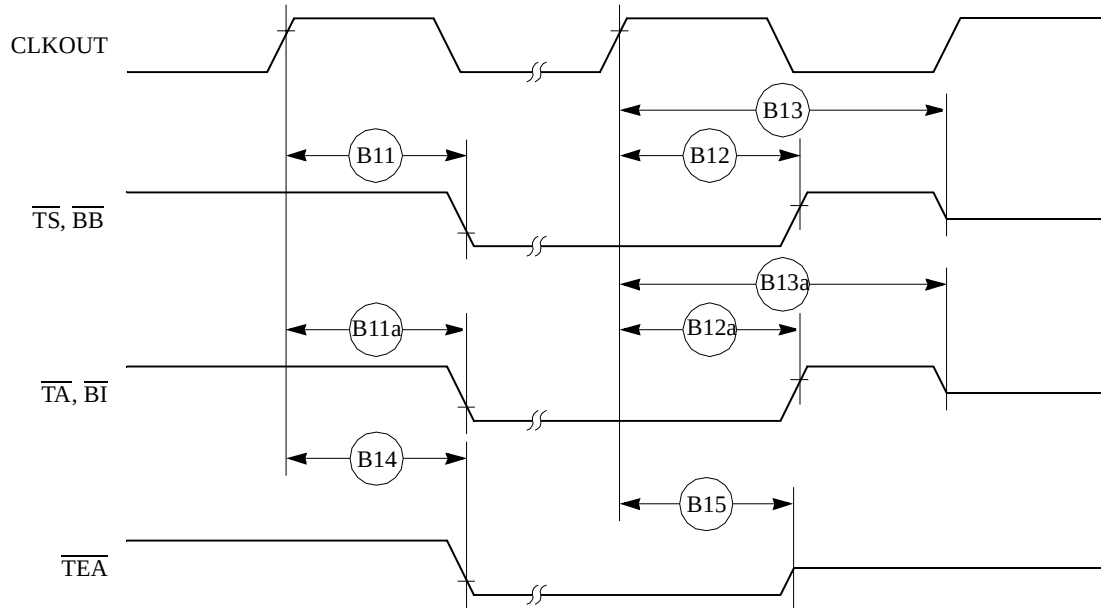


**Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing**

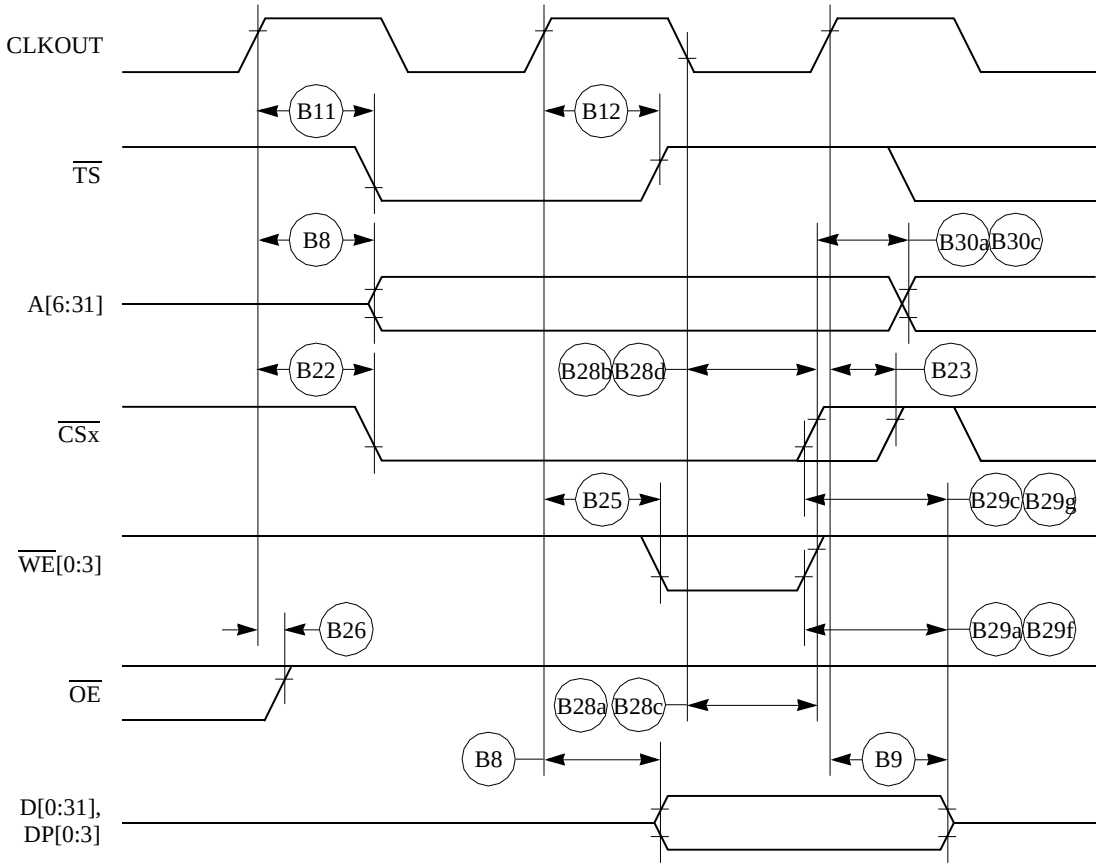


**Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)**

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

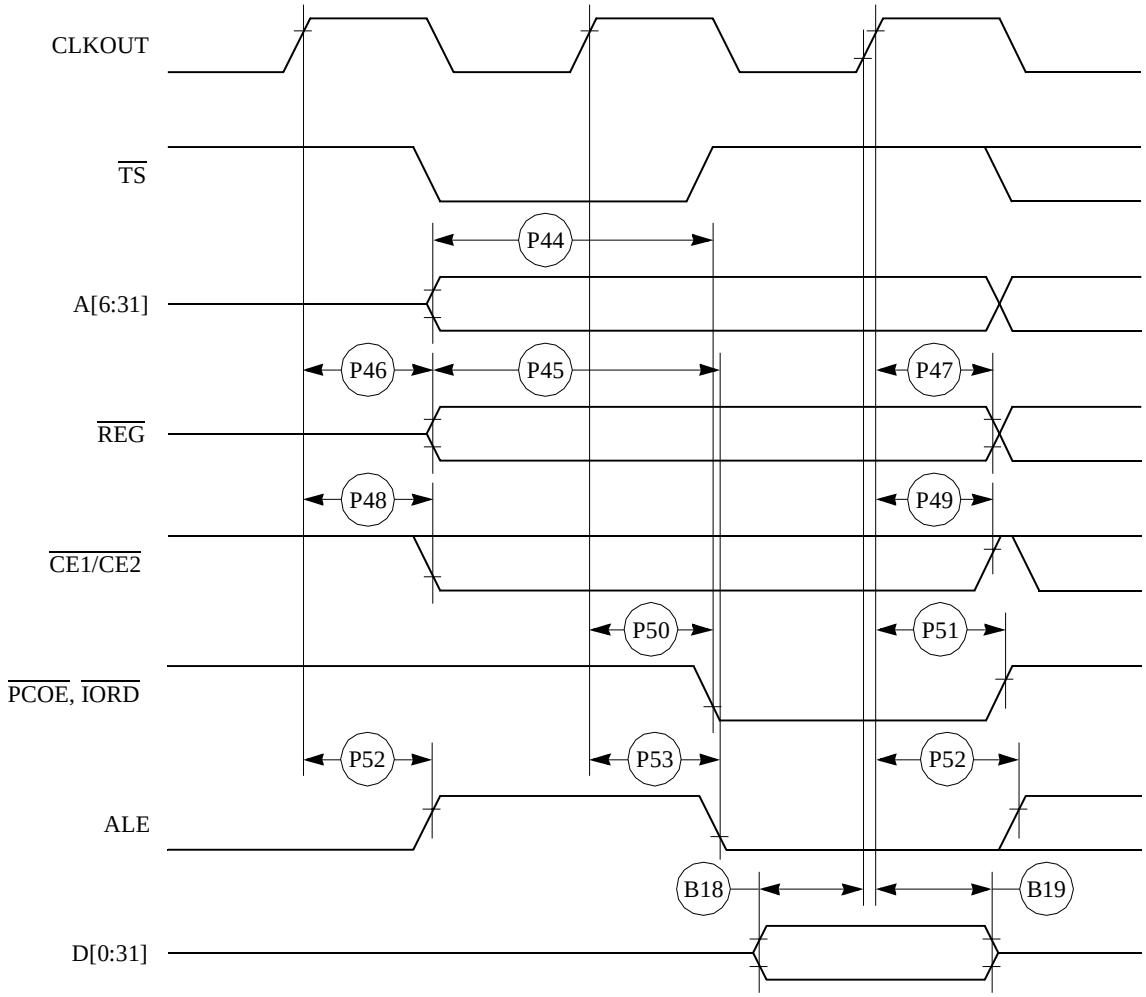


**Figure 24. PCMCIA Access Cycles Timing External Bus Read**

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

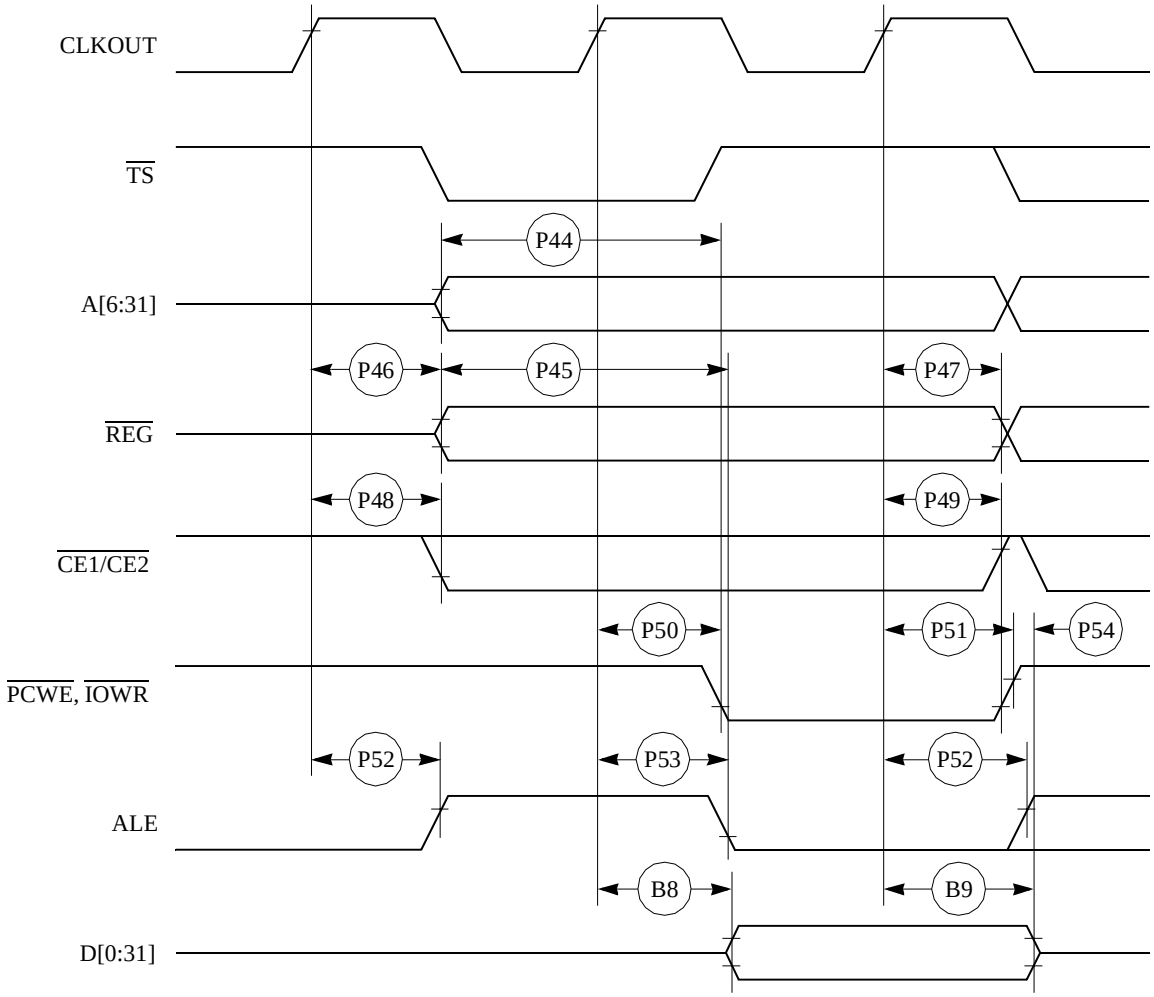


**Figure 25. PCMCIA Access Cycles Timing External Bus Write**

Figure 26 provides the PCMCIA WAIT signals detection timing.

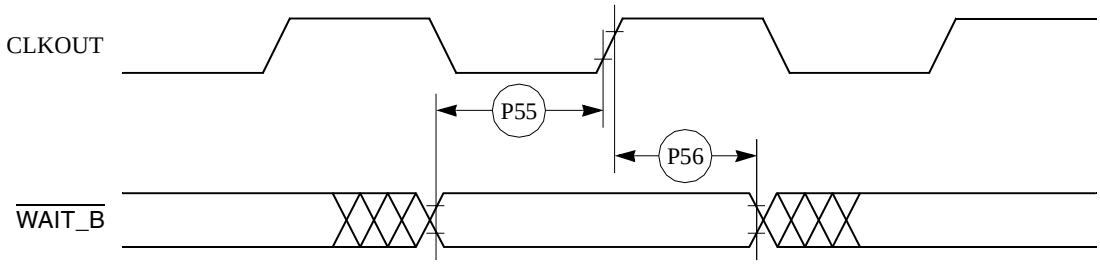


**Figure 26. PCMCIA WAIT Signal Detection Timing**

Table 9 shows the PCMCIA port timing for the MPC850.

**Table 9. PCMCIA Port Timing**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| P57 | CLKOUT to OPx valid | — | 19.00 | — | 19.00 | — | 19.00 | ns |
| P58 | $\overline{\text{HRESET}}$ negated to OPx drive [1] | 18.00 | — | 26.00 | — | 22.00 | — | ns |
| P59 | IP_Xx valid to CLKOUT rising edge | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| P60 | CLKOUT rising edge to IP_Xx invalid | 1.00 | — | 1.00 | — | 1.00 | — | ns |

[1] OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

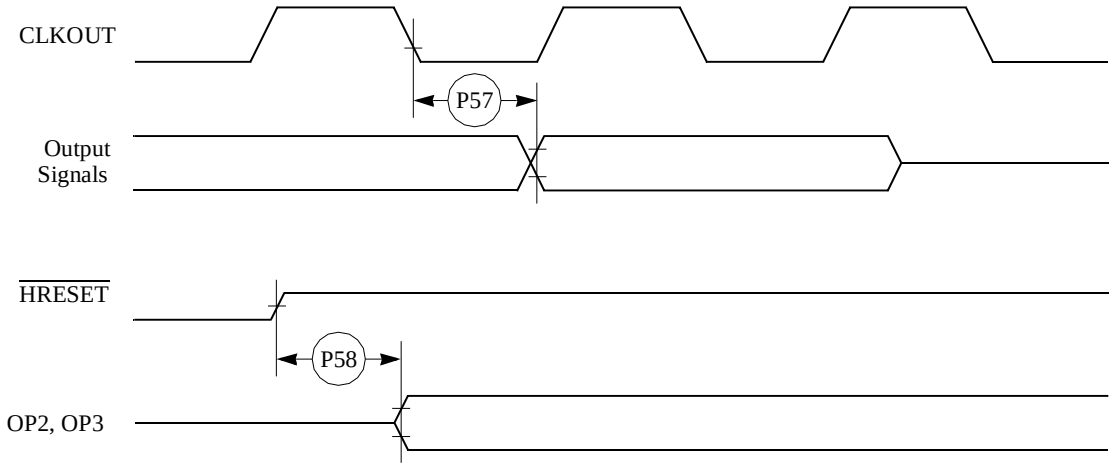


**Figure 27. PCMCIA Output Port Timing**

Figure 28 provides the PCMCIA output port timing for the MPC850.

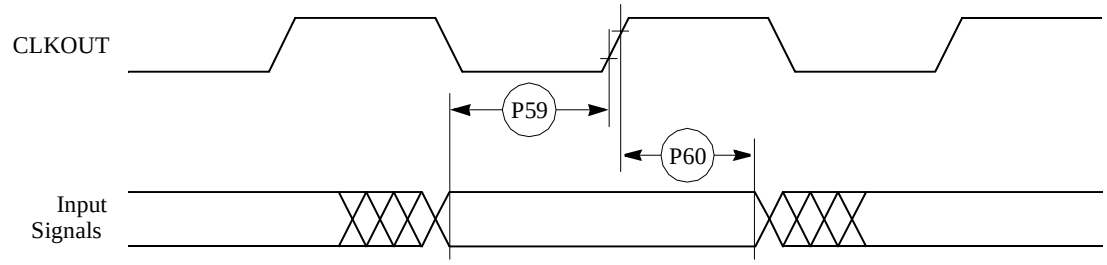


**Figure 28. PCMCIA Input Port Timing**

Table 10 shows the debug port timing for the MPC850.

**Table 10. Debug Port Timing**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| D61 | DSCK cycle time | 60.00 | — | 91.00 | — | 75.00 | — | ns |
| D62 | DSCK clock pulse width | 25.00 | — | 38.00 | — | 31.00 | — | ns |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | 0.00 | 3.00 | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| D65 | DSDI data hold time | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | 0.00 | 15.00 | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | 0.00 | 2.00 | 0.00 | 2.00 | ns |

Figure 29 provides the input timing for the debug port clock.

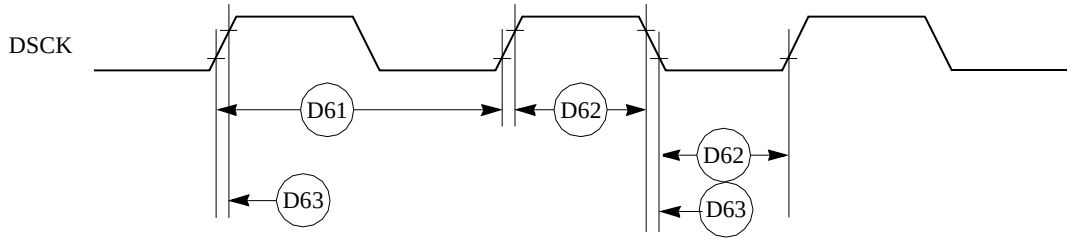


**Figure 29. Debug Port Clock Input Timing**

Figure 30 provides the timing for the debug port.

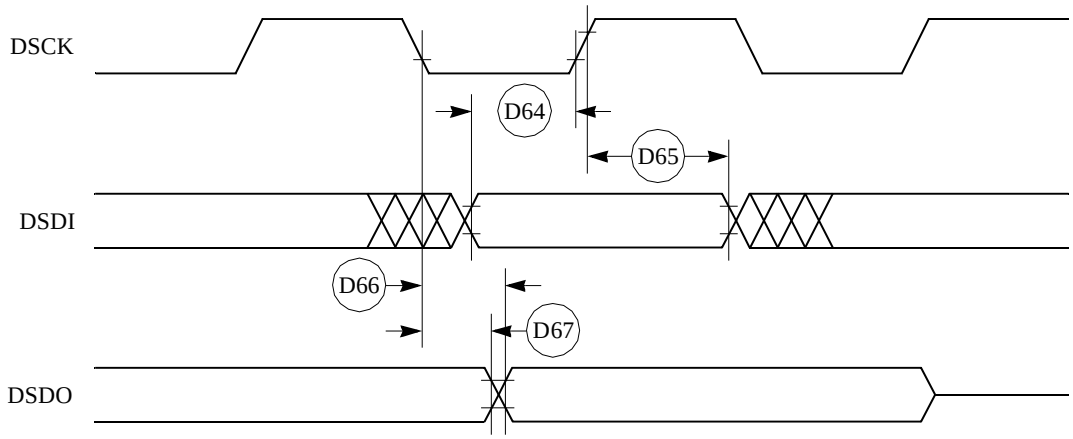


**Figure 30. Debug Port Timings**

Figure 33 provides the reset timing for the debug port configuration.

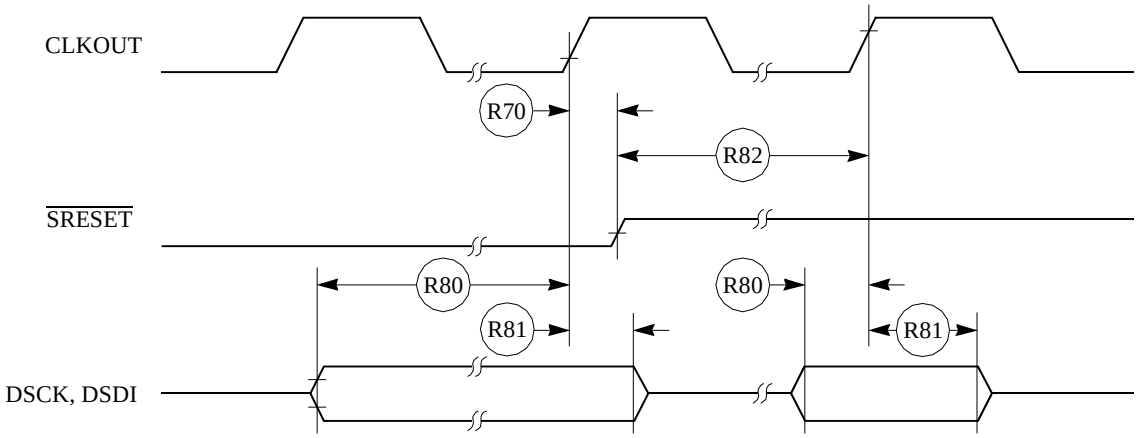


**Figure 33. Reset Timing—Debug Port Configuration**

# 7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

**Table 12. JTAG Timing**

| Num | Characteristic | 50 MHz | | 66MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | 100.00 | — | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | 40.00 | — | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | 0.00 | 10.00 | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | — | 27.00 | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | 100.00 | — | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | 40.00 | — | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | — | 50.00 | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | 50.00 | — | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | 50.00 | — | 50.00 | — | ns |

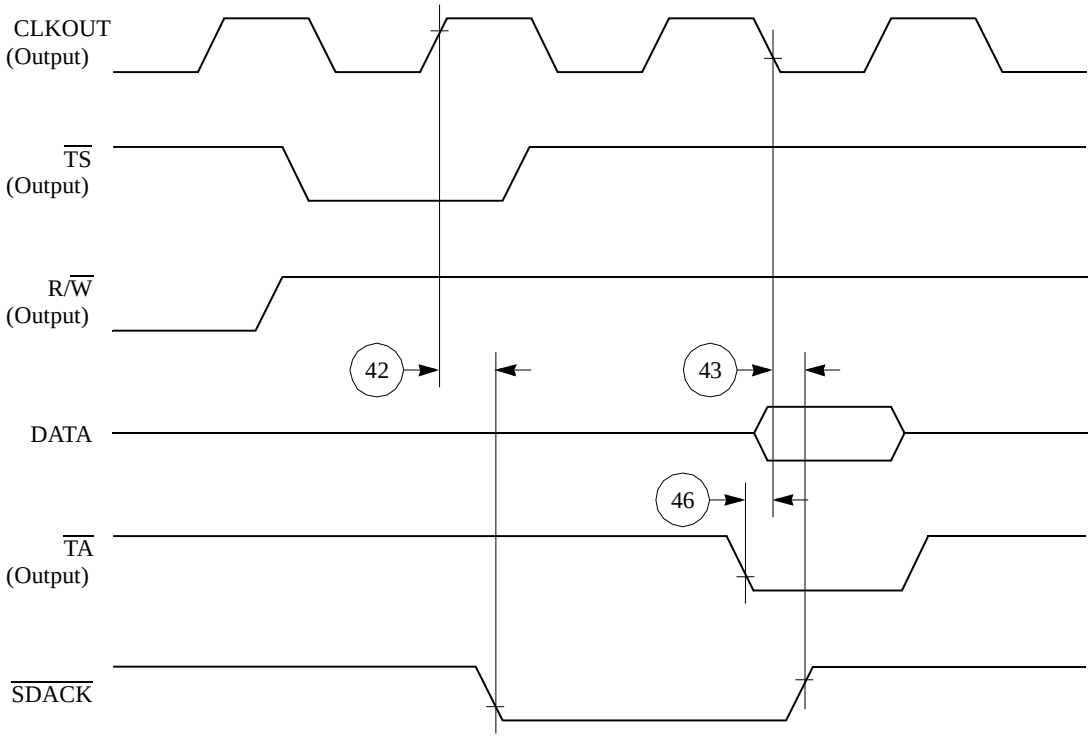


**Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock**

## 8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

**Table 15. Baud Rate Generator Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 50 | BRGO rise and fall time | — | 10.00 | ns |
| 51 | BRGO duty cycle | 40.00 | 60.00 | % |
| 52 | BRGO cycle | 40.00 | — | ns |

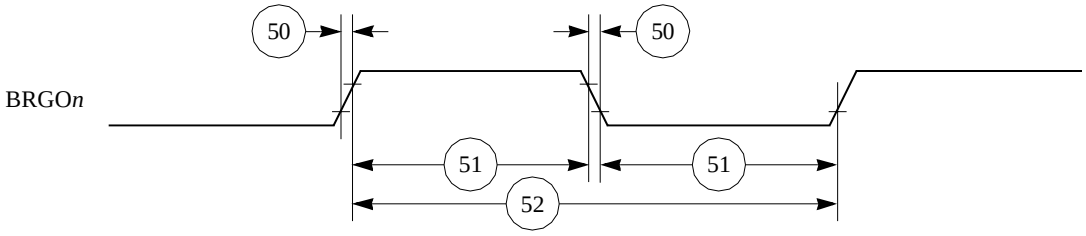


**Figure 43. Baud Rate Generator Timing Diagram**

## 8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

**Table 16. Timer Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 61 | TIN/$\overline{\text{TGATE}}$ rise and fall time | 10.00 | — | ns |
| 62 | TIN/$\overline{\text{TGATE}}$ low time | 1.00 | — | clk |
| 63 | TIN/$\overline{\text{TGATE}}$ high time | 2.00 | — | clk |
| 64 | TIN/$\overline{\text{TGATE}}$ cycle time | 3.00 | — | clk |
| 65 | CLKO high to $\overline{\text{TOUT}}$ valid | 3.00 | 25.00 | ns |

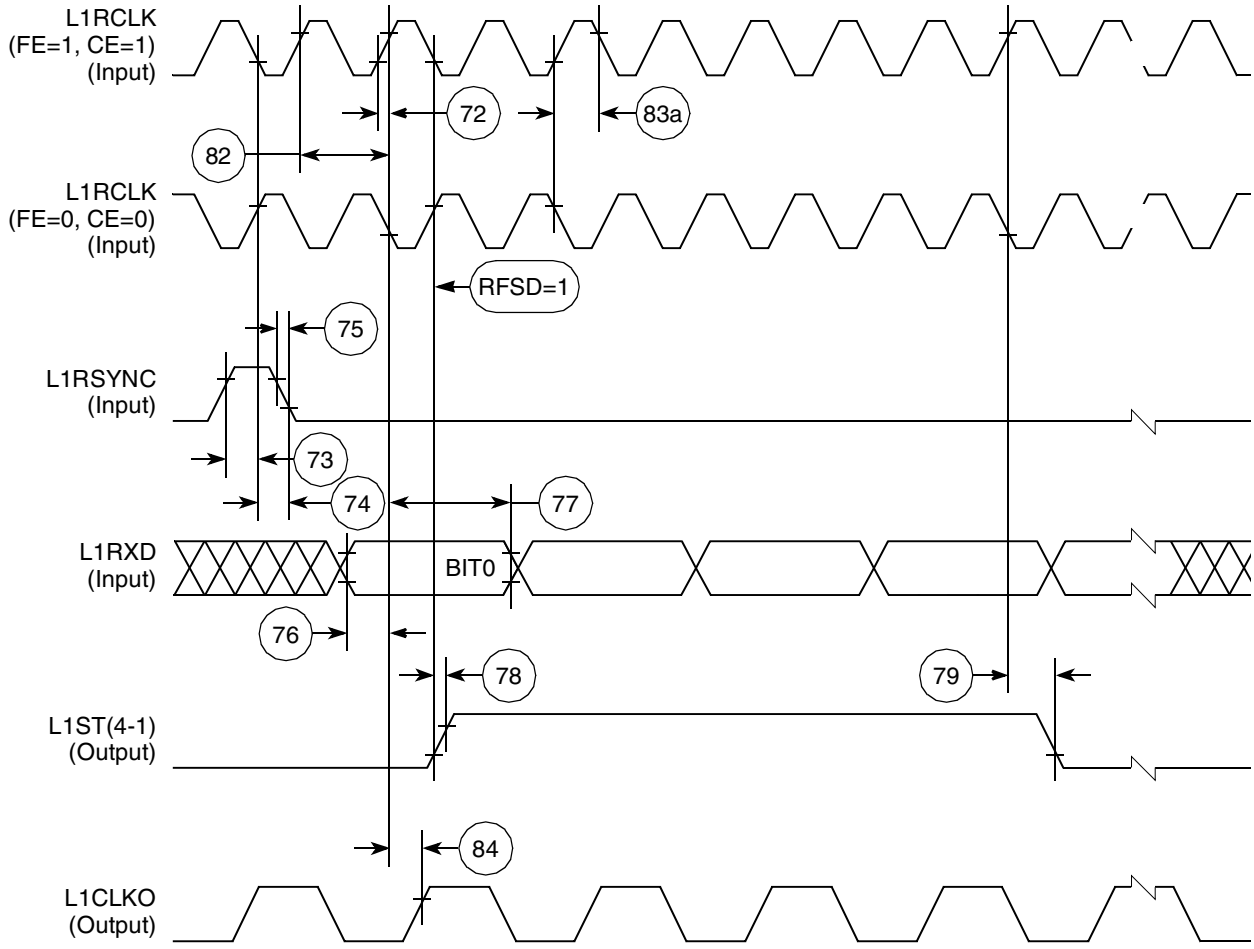


**Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)**

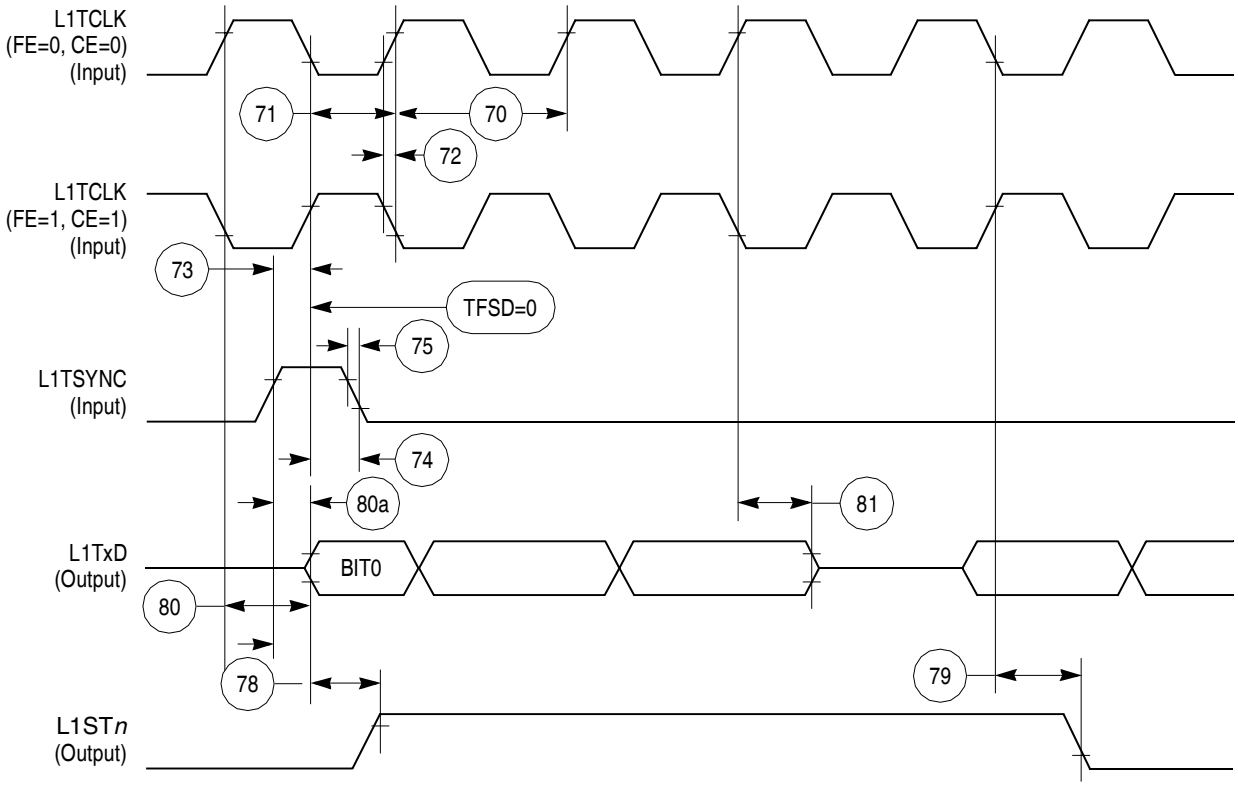


**Figure 47. SI Transmit Timing Diagram**

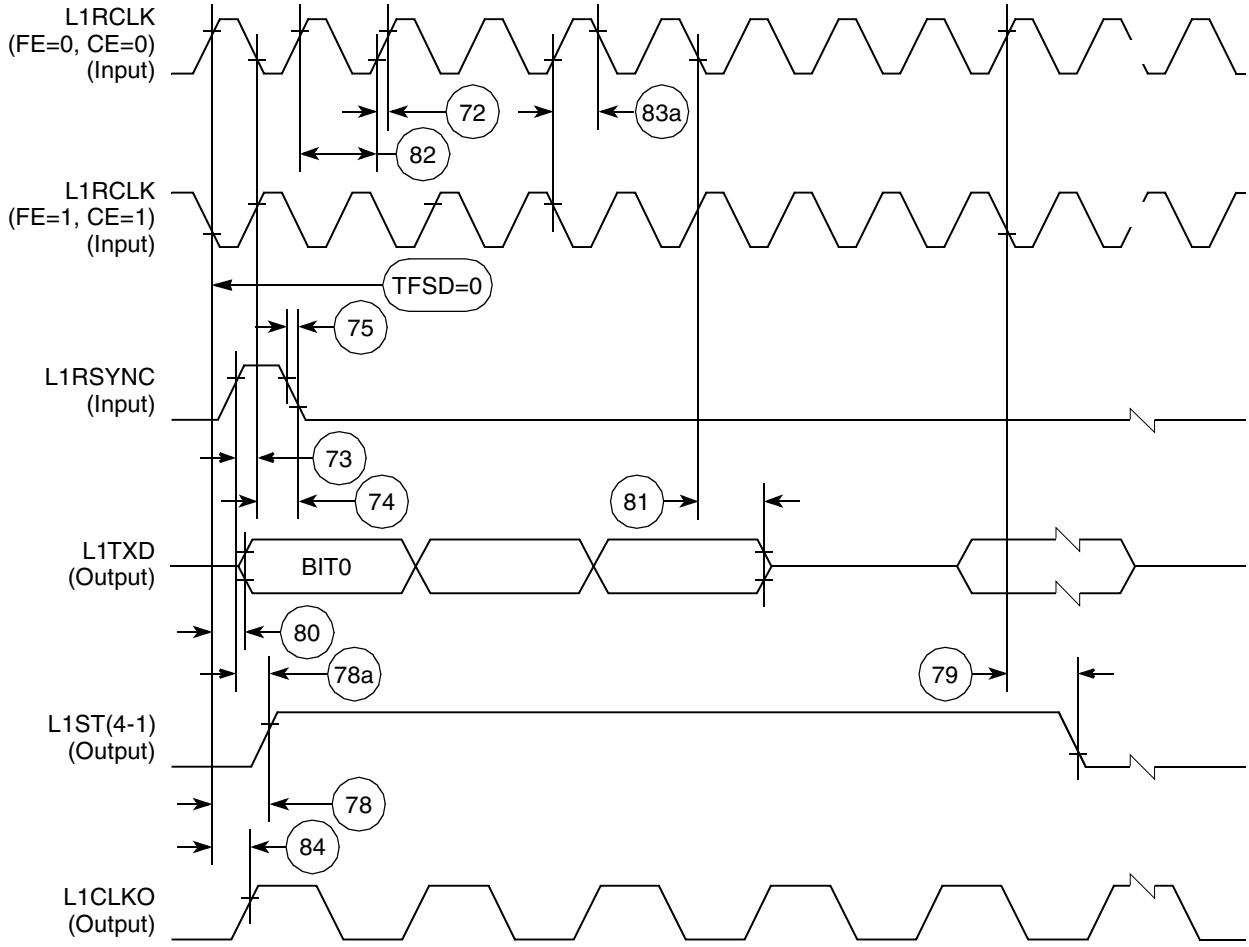


**Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)**

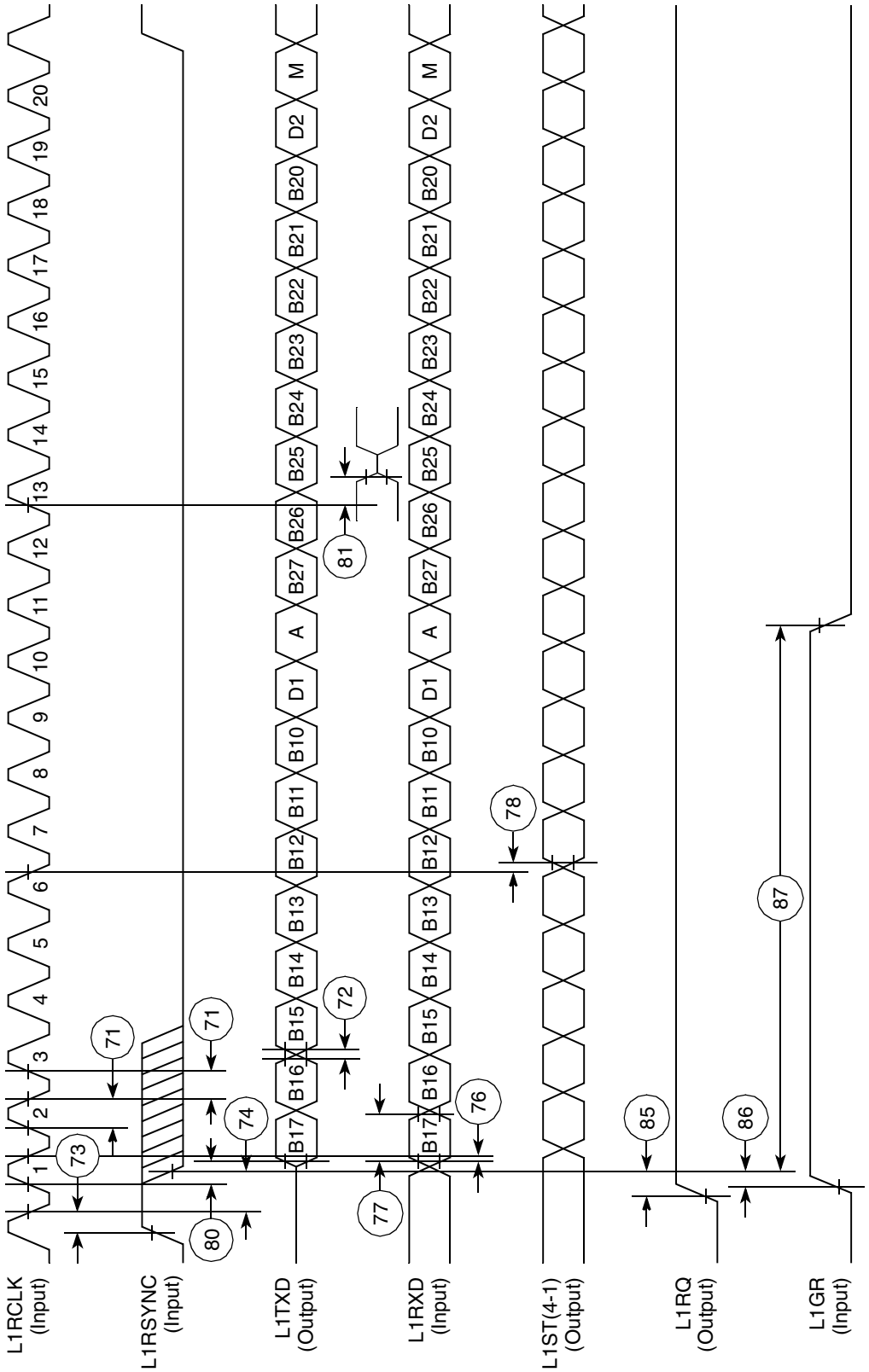


**Figure 49. IDL Timing**

# 9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

**Table 26. MPC850 Family Derivatives**

| Device | Ethernet Support | Number of SCCs [1] | 32-Channel HDLC Support | 64-Channel HDLC Support [2] |
|---|---|---|---|---|
| MPC850 | N/A | One | N/A | N/A |
| MPC850DE | Yes | Two | N/A | N/A |
| MPC850SR | Yes | Two | N/A | Yes |
| MPC850DSL | Yes | Two | No | No |

1 Serial Communication Controller (SCC)

2 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

**Table 27. MPC850 Package/Frequency/Availability**

| Package Type | Frequency (MHz) | Temperature (Tj) | Order Number |
|---|---|---|---|
| 256-Lead Plastic Ball Grid Array (ZT suffix) | 50 | 0°C to 95°C | XPC850ZT50BU<br>XPC850DEZT50BU<br>XPC850SRZT50BU<br>XPC850DSLZT50BU |
| | 66 | 0°C to 95°C | XPC850ZT66BU<br>XPC850DEZT66BU<br>XPC850SRZT66BU |
| | 80 | 0°C to 95°C | XPC850ZT80BU<br>XPC850DEZT80BU<br>XPC850SRZT80BU |
| 256-Lead Plastic Ball Grid Array (CZT suffix) | 50 | -40°C to 95°C | XPC850CZT50BU<br>XPC850DECZT50BU<br>XPC850SRCZT50BU<br>XPC850DSLCZT50BU |
| | 66 | | XPC850CZT66BU<br>XPC850DECZT66BU<br>XPC850SRCZT66BU |
| | 80 | | XPC850CZT80B<br>XPC850DECZT80B<br>XPC850SRCZT80B |

## 9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

# 10 Document Revision History

Table 28 lists significant changes between revisions of this document.

**Table 28. Document Revision History**

| Revision | Date | Change |
|---|---|---|
| 2 | 7/2005 | Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit. |
| 1 | 10/2002 | Added MPC850DSL. Corrected Figure 25 on page 34. |
| 0.2 | 04/2002 | Updated power numbers and added Rev. C |
| 0.1 | 11/2001 | Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table. |

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