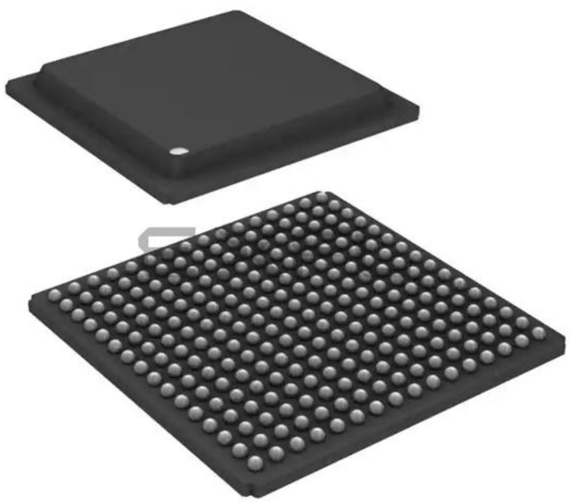
# NXP USA Inc. - MPC850SRZQ50BU Datasheet



**Welcome to** E-XFL.COM

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 50MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 256-BBGA |
| Supplier Device Package | 256-PBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850srzq50bu |

# 2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:

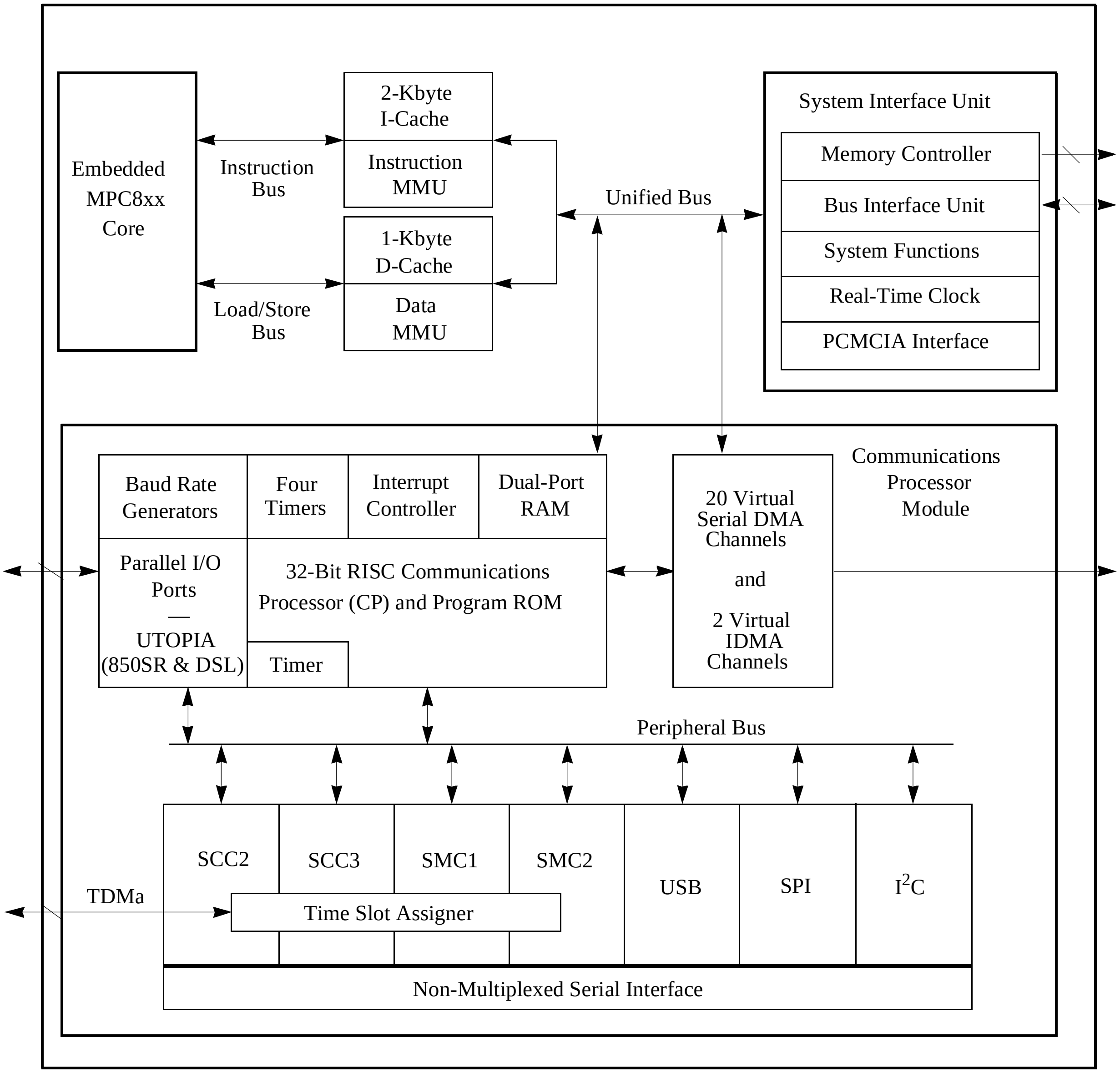


Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

  - Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
  - Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - The MPC850 can compare using the =, ≠, <, and > conditions to generate watchpoints
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility on all general purpose I/O pins.

# 3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC850. Table 2 provides the maximum ratings.

**Table 2. Maximum Ratings**

(GND = 0V)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | VDDH | -0.3 to 4.0 | V |
| | VDDL | -0.3 to 4.0 | V |
| | KAPWR | -0.3 to 4.0 | V |
| | VDDSYN | -0.3 to 4.0 | V |
| Input voltage [1] | $V_{in}$ | GND-0.3 to VDDH + 2.5 V | V |
| Junction temperature [2] | $T_j$ | 0 to 95 (standard)<br>-40 to 95 (extended) | °C |
| Storage temperature range | $T_{stg}$ | -55 to +150 | °C |

[1] Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
CAUTION: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC850 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

[2] The MPC850, a high-frequency device in a BGA package, does not provide a guaranteed maximum ambient temperature. Only maximum junction temperature is guaranteed. It is the responsibility of the user to consider power dissipation and thermal management. Junction temperature ratings are the same regardless of frequency rating of the device.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{CC}$). Table 3 provides the package thermal characteristics for the MPC850.

$\theta_{JA}$ = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between $P_D$ and $T_J$ is:

$P_D = K \div (T_J + 273°C)$(2)

Solving equations (1) and (2) for K gives:

$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$(3)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 5.1 Layout Practices

Each $V_{CC}$ pin on the MPC850 should be provided with a low-impedance path to the board’s supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{CC}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$ and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

### Table 6. Bus Operation Timing [1] (continued)

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B28c | CLKOUT falling edge to $\overline{\text{WE[0–3]}}$ negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 | 7.00 | 14.00 | 11.00 | 18.00 | 9.00 | 16.00 | 0.375 | 50.00 | ns |
| B28d | CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | — | 14.00 | — | 18.00 | — | 16.00 | 0.375 | 50.00 | ns |
| B29 | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, CSNT = 0 | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B29a | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B29b | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B29c | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B29d | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B29e | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B29f | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1 | 5.00 | — | 9.00 | — | 7.00 | — | 0.375 | 50.00 | ns |
| B29g | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 5.00 | — | 9.00 | — | 7.00 | — | 0.375 | 50.00 | ns |

### Table 6. Bus Operation Timing [1] (continued)

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B31 | CLKOUT falling edge to $\overline{\text{CS}}$ valid - as requested by control bit CST4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |
| B31a | CLKOUT falling edge to $\overline{\text{CS}}$ valid - as requested by control bit CST1 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B31b | CLKOUT rising edge to $\overline{\text{CS}}$ valid - as requested by control bit CST2 in the corresponding word in the UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | — | 50.00 | ns |
| B31c | CLKOUT rising edge to $\overline{\text{CS}}$ valid - as requested by control bit CST3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B31d | CLKOUT falling edge to $\overline{\text{CS}}$ valid - as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 | 9.00 | 14.00 | 13.00 | 18.00 | 11.00 | 16.00 | 0.375 | 50.00 | ns |
| B32 | CLKOUT falling edge to $\overline{\text{BS}}$ valid - as requested by control bit BST4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |
| B32a | CLKOUT falling edge to $\overline{\text{BS}}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B32b | CLKOUT rising edge to $\overline{\text{BS}}$ valid - as requested by control bit BST2 in the corresponding word in the UPM | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | — | 50.00 | ns |
| B32c | CLKOUT rising edge to $\overline{\text{BS}}$ valid - as requested by control bit BST3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B32d | CLKOUT falling edge to $\overline{\text{BS}}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 | 9.00 | 14.00 | 13.00 | 18.00 | 11.00 | 16.00 | 0.375 | 50.00 | ns |
| B33 | CLKOUT falling edge to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | — | 50.00 | ns |

### Table 6. Bus Operation Timing [1] (continued)

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B33a | CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B34 | A[6–31] and D[0–31] to $\overline{\text{CS}}$ valid - as requested by control bit CST4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B34a | A[6–31] and D[0–31] to $\overline{\text{CS}}$ valid - as requested by control bit CST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B34b | A[6–31] and D[0–31] to $\overline{\text{CS}}$ valid - as requested by CST2 in the corresponding word in UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B35 | A[6–31] to $\overline{\text{CS}}$ valid - as requested by control bit BST4 in the corresponding word in UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B35a | A[6–31] and D[0–31] to $\overline{\text{BS}}$ valid - as requested by BST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B35b | A[6–31] and D[0–31] to $\overline{\text{BS}}$ valid - as requested by control bit BST2 in the corresponding word in the UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B36 | A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B37 | UPWAIT valid to CLKOUT falling edge [10] | 6.00 | — | 6.00 | — | 6.00 | — | — | 50.00 | ns |
| B38 | CLKOUT falling edge to UPWAIT valid [10] | 1.00 | — | 1.00 | — | 1.00 | — | — | 50.00 | ns |
| B39 | $\overline{\text{AS}}$ valid to CLKOUT rising edge [11] | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B40 | A[6–31], TSIZ[0–1], RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, valid to CLKOUT rising edge. | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B41 | $\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |

Figure 4 provides the timing for the synchronous output signals.

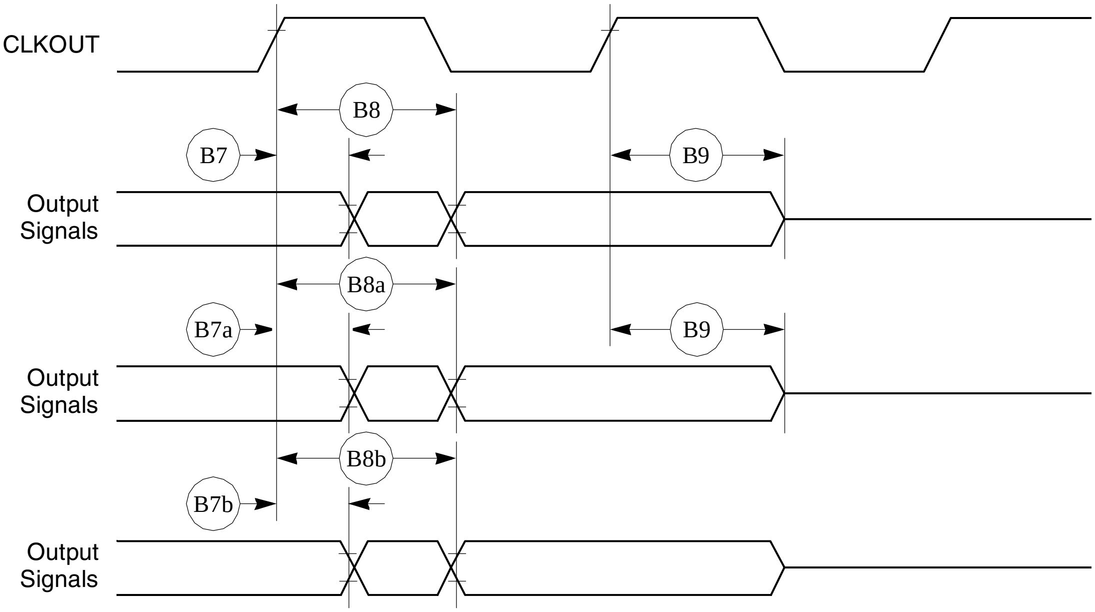


**Figure 4. Synchronous Output Signals Timing**

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.

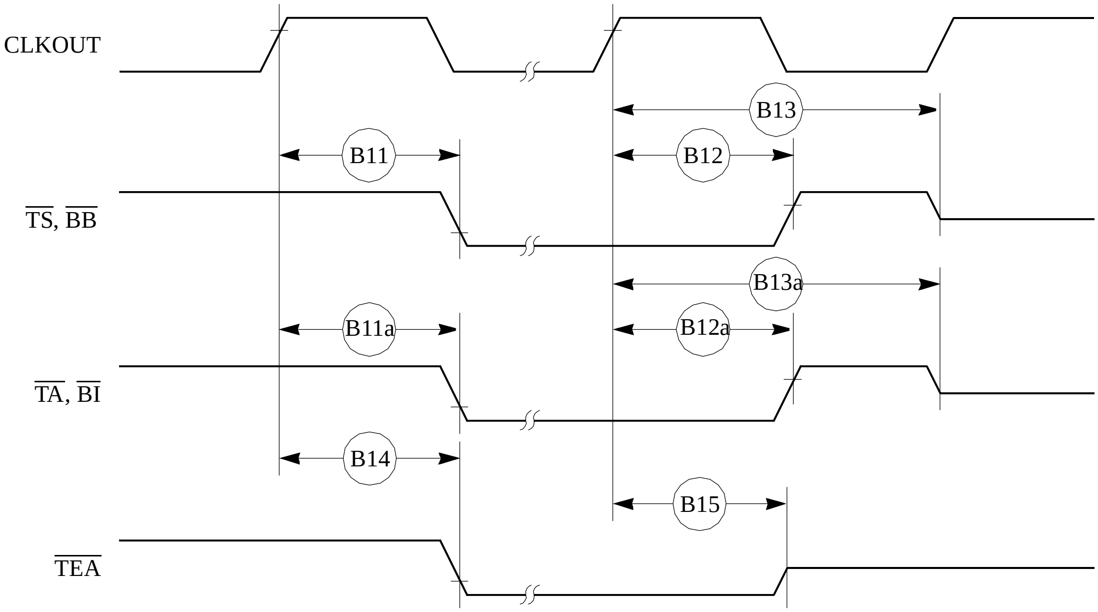


**Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing**

Figure 16 provides the timing for the external bus controlled by the UPM.

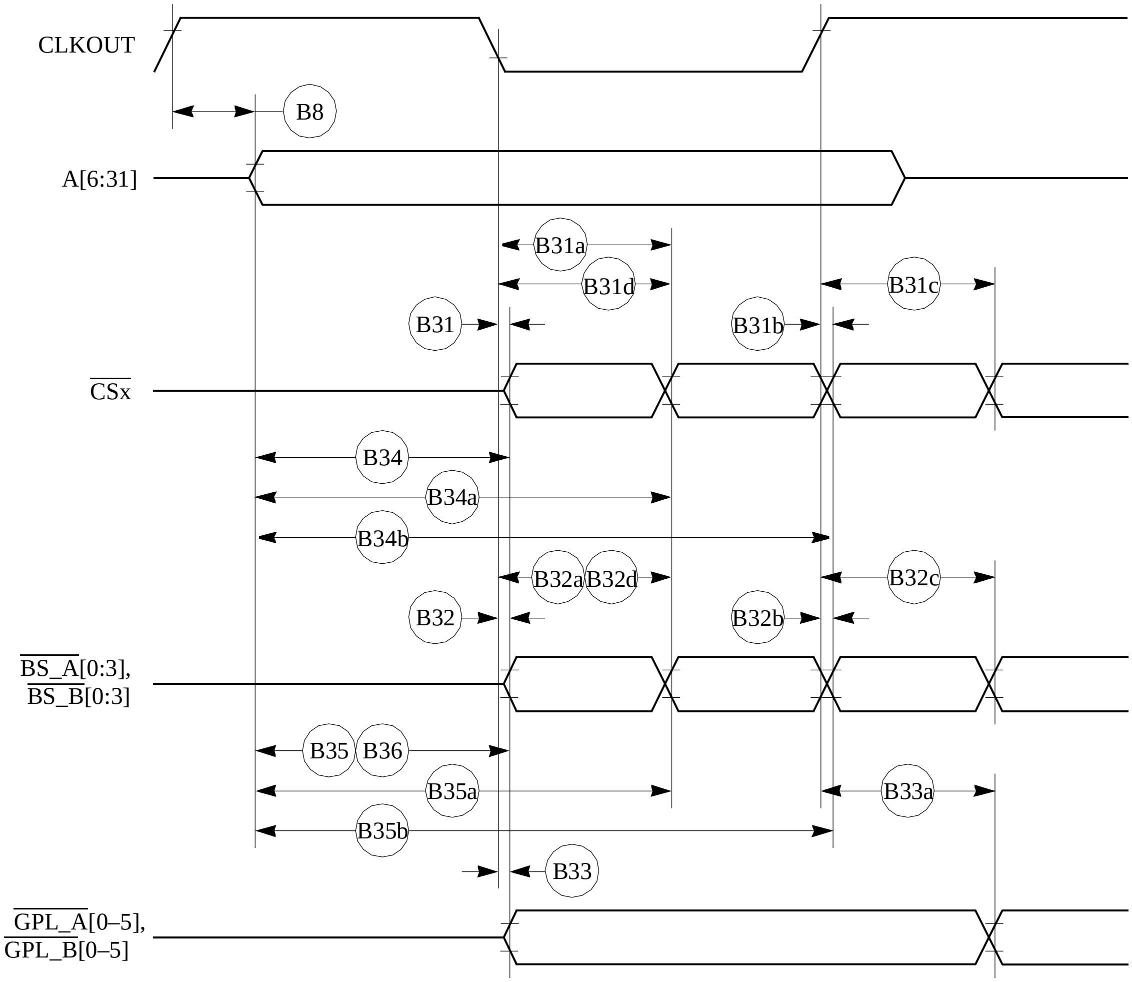


Figure 16. External Bus Timing (UPM Controlled Signals)

Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

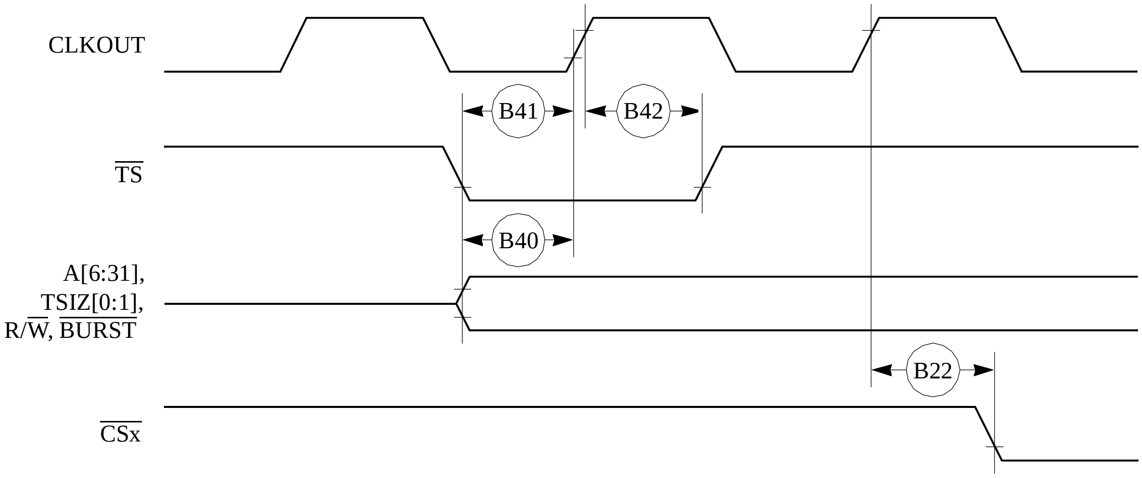


Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.

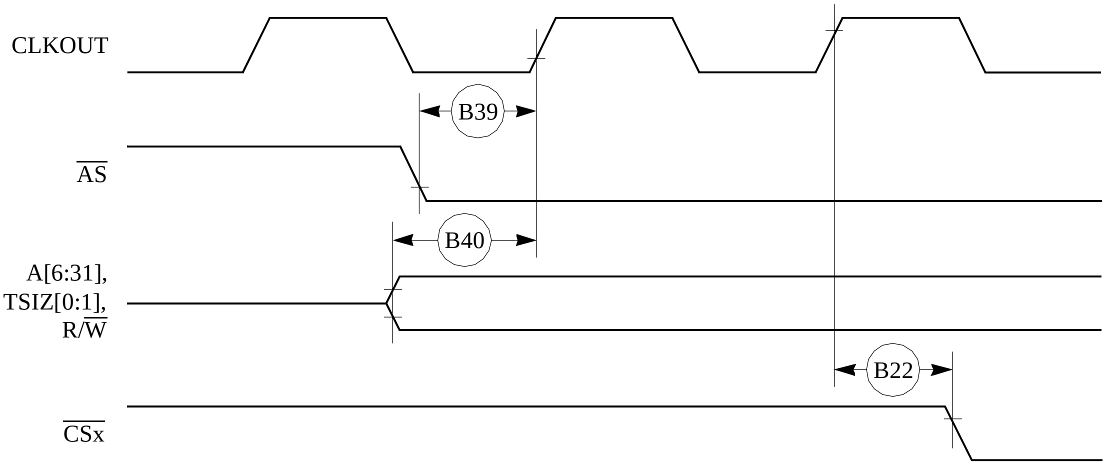


Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 21 provides the timing for the asynchronous external master control signals negation.

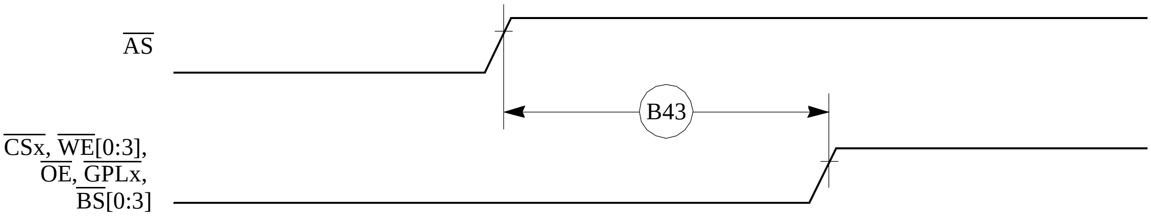


Figure 21. Asynchronous External Master—Control Signals Negation Timing

Table 7 provides interrupt timing for the MPC850.

Table 7. Interrupt Timing

| Num | Characteristic [1] | 50 MHz | | 66MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| I39 | $\overline{\text{IRQx}}$ valid to CLKOUT rising edge (set up time) | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| I40 | $\overline{\text{IRQx}}$ hold time after CLKOUT. | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| I41 | $\overline{\text{IRQx}}$ pulse width low | 3.00 | — | 3.00 | — | 3.00 | — | ns |
| I42 | $\overline{\text{IRQx}}$ pulse width high | 3.00 | — | 3.00 | — | 3.00 | — | ns |
| I43 | $\overline{\text{IRQx}}$ edge-to-edge time | 80.00 | — | 121.0 | — | 100.0 | — | ns |

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.

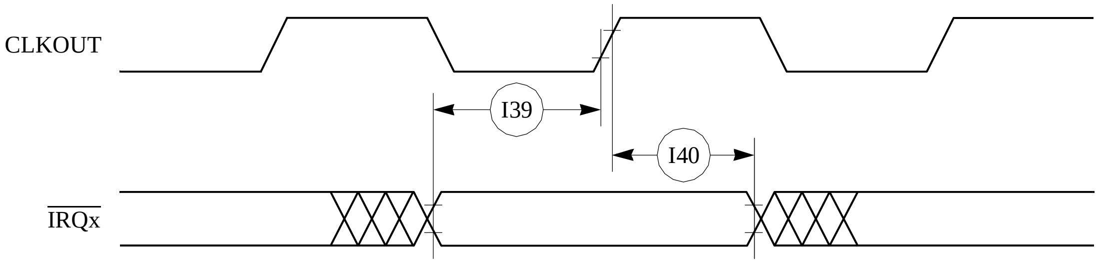


Figure 22. Interrupt Detection Timing for External Level Sensitive Lines

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.

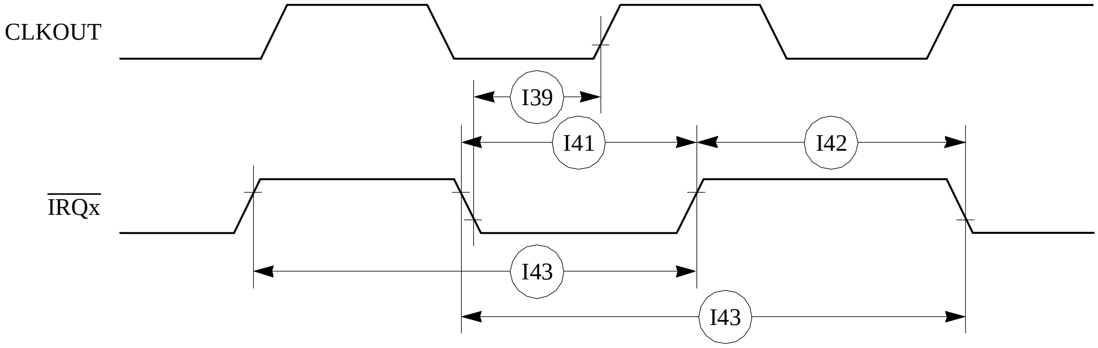


Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines

Table 10 shows the debug port timing for the MPC850.

**Table 10. Debug Port Timing**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| D61 | DSCK cycle time | 60.00 | — | 91.00 | — | 75.00 | — | ns |
| D62 | DSCK clock pulse width | 25.00 | — | 38.00 | — | 31.00 | — | ns |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | 0.00 | 3.00 | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| D65 | DSDI data hold time | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | 0.00 | 15.00 | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | 0.00 | 2.00 | 0.00 | 2.00 | ns |

Figure 29 provides the input timing for the debug port clock.

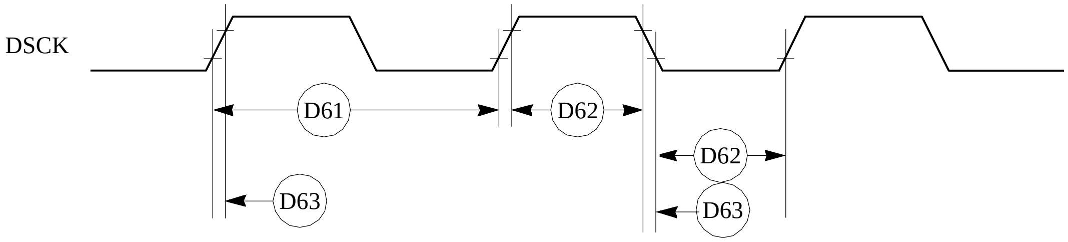


Figure 29. Debug Port Clock Input Timing

Figure 30 provides the timing for the debug port.

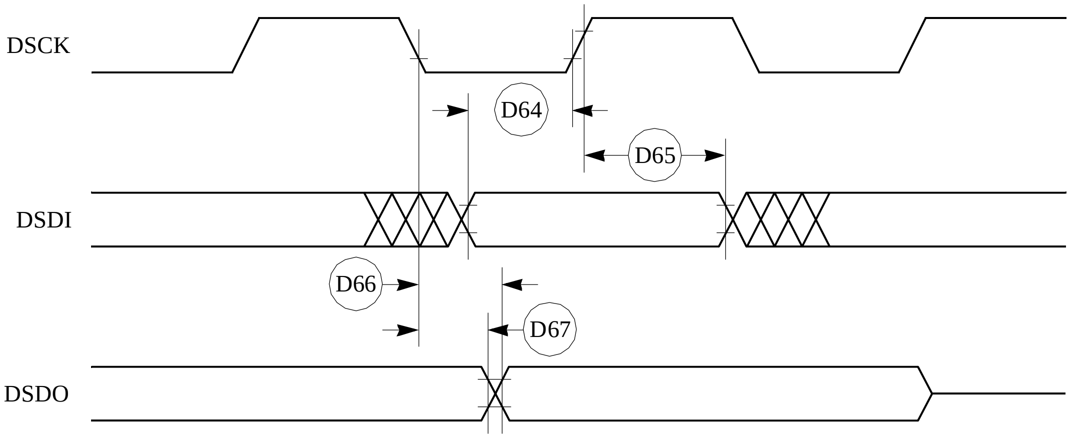


Figure 30. Debug Port Timings

Table 11 shows the reset timing for the MPC850.

**Table 11. Reset Timing**

| Num | Characteristic | 50 MHz | | 66MHz | | 80 MHz | | FFACTOR | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| R69 | CLKOUT to $\overline{\text{HRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | ns |
| R70 | CLKOUT to $\overline{\text{SRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | ns |
| R71 | $\overline{\text{RSTCONF}}$ pulse width | 340.00 | — | 515.00 | — | 425.00 | — | 17.000 | ns |
| R72 | | — | — | — | — | — | — | — | |
| R73 | Configuration data to $\overline{\text{HRESET}}$ rising edge set up time | 350.00 | — | 505.00 | — | 425.00 | — | 15.000 | ns |
| R74 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time | 350.00 | — | 350.00 | — | 350.00 | — | — | ns |
| R75 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R76 | Configuration data hold time after $\overline{\text{HRESET}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R77 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R78 | $\overline{\text{RSTCONF}}$ negated to data out high impedance. | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R79 | CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance. | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R80 | DSDI, DSCK set up | 60.00 | — | 90.00 | — | 75.00 | — | 3.000 | ns |
| R81 | DSDI, DSCK hold time | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R82 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample | 160.00 | — | 242.00 | — | 200.00 | — | 8.000 | ns |

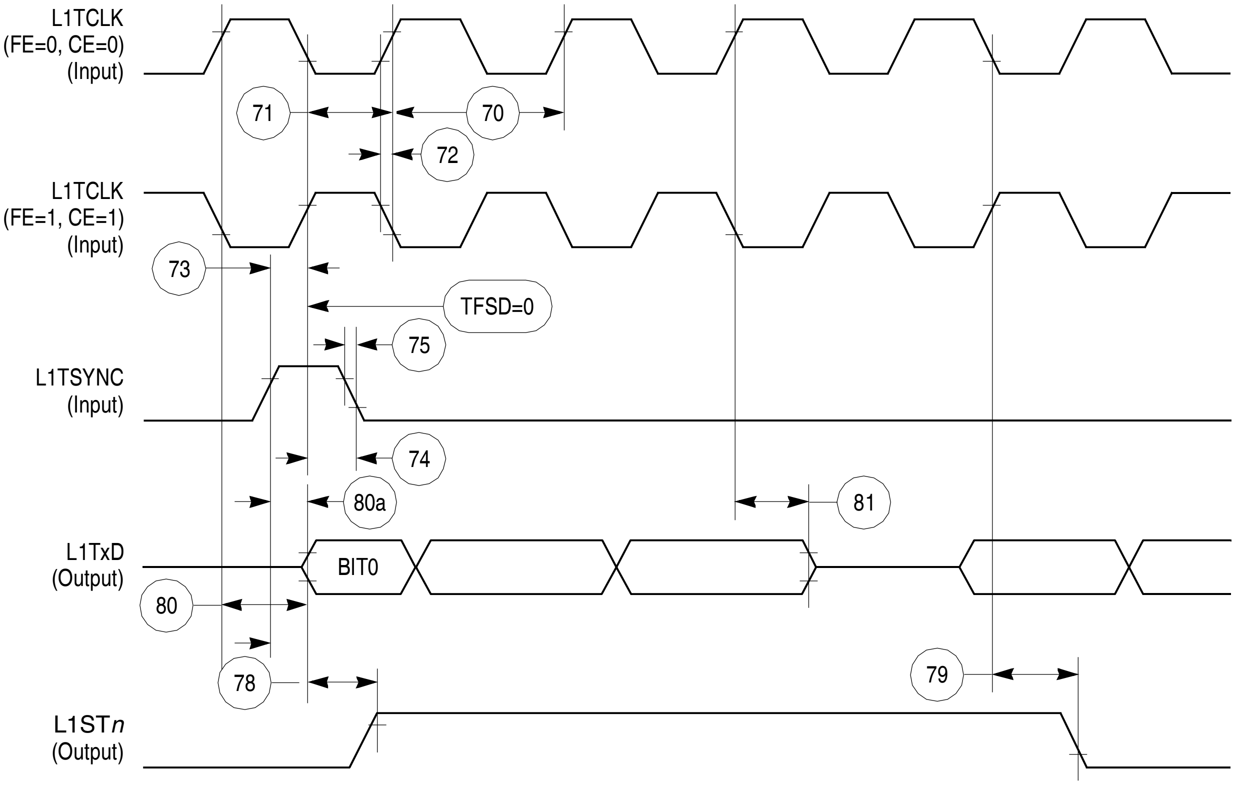


Figure 47. SI Transmit Timing Diagram

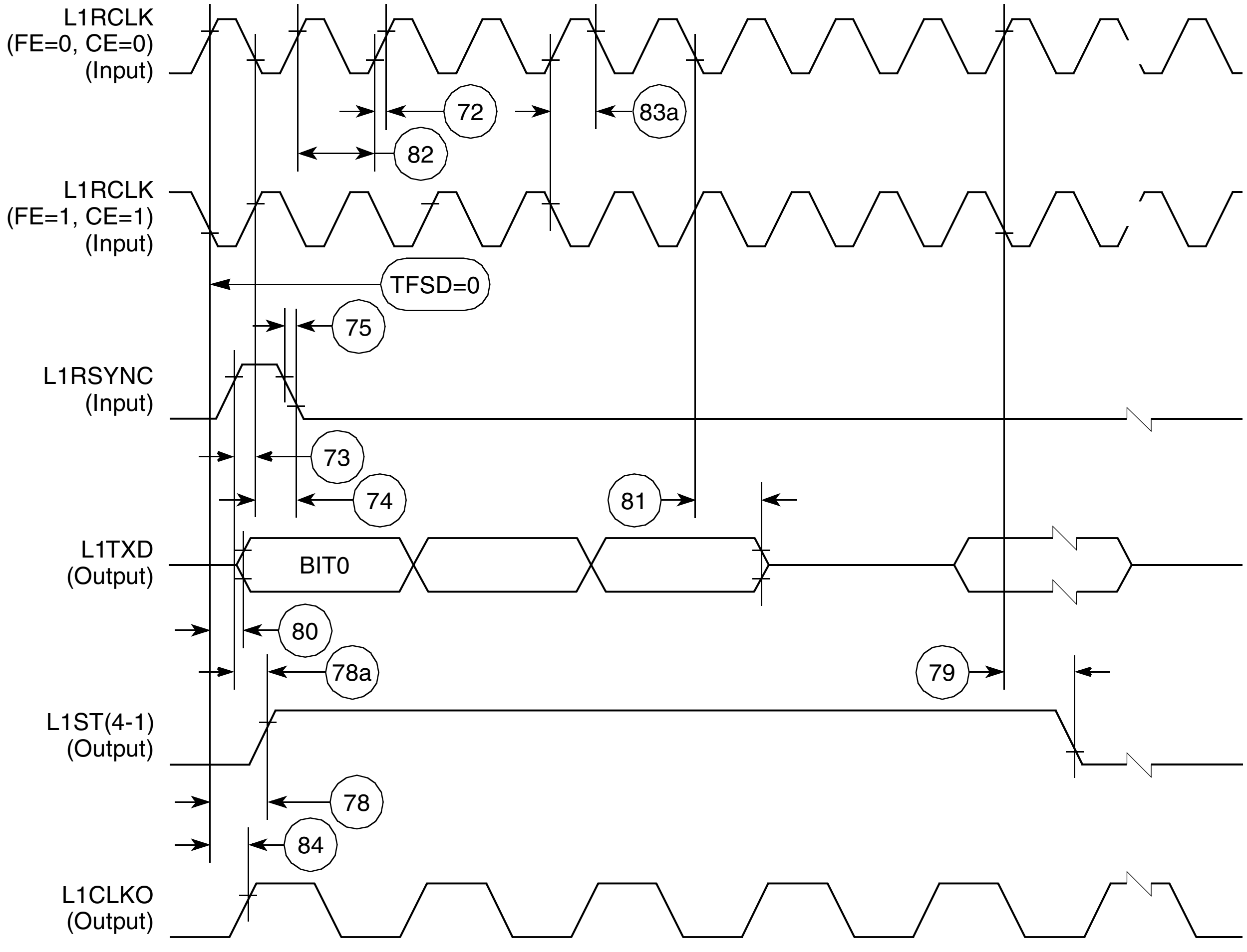


Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)

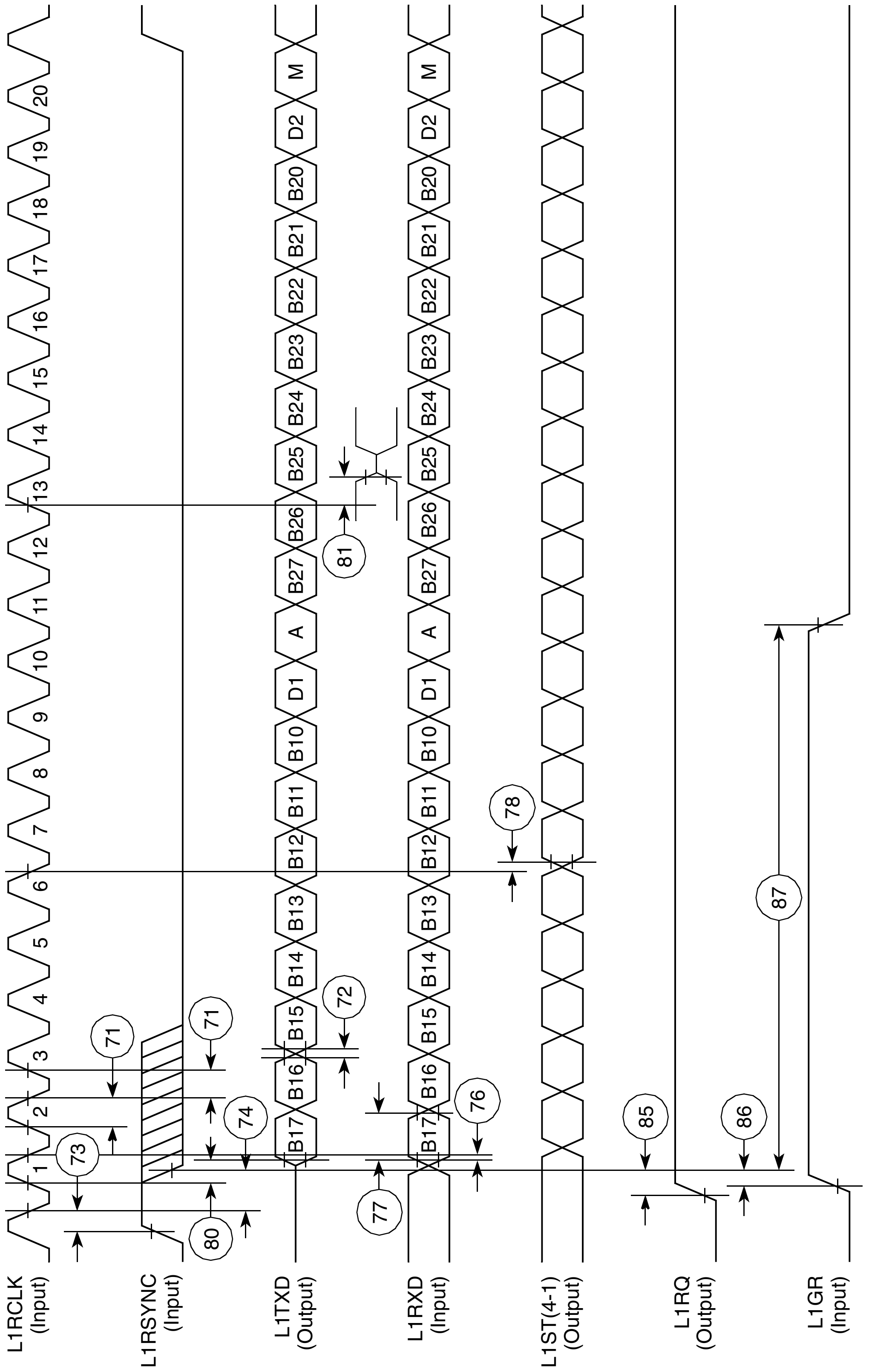


Figure 49. IDL Timing

## 8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

**Table 23. SPI Slave Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15.00 | — | ns |
| 172 | Slave enable lag time | 15.00 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20.00 | — | ns |
| 176 | Slave data hold time (inputs) | 20.00 | — | ns |
| 177 | Slave access time | — | 50.00 | ns |
| 178 | Slave SPI MISO disable time | — | 50.00 | ns |
| 179 | Slave data valid (after SPICLK edge) | — | 50.00 | ns |
| 180 | Slave data hold time (outputs) | 0.00 | — | ns |
| 181 | Rise time (input) | — | 15.00 | ns |
| 182 | Fall time (input) | — | 15.00 | ns |

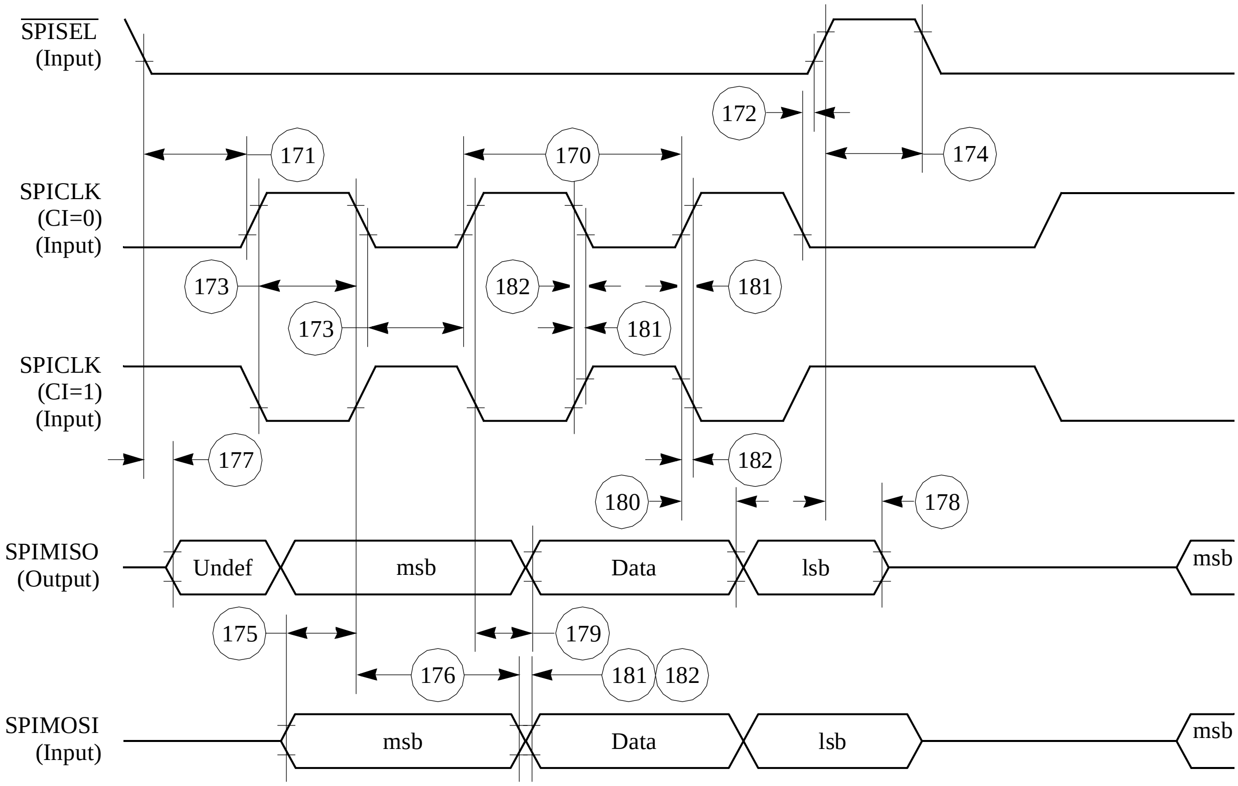


Figure 60. SPI Slave (CP = 1) Timing Diagram

## 8.11 I²C AC Electrical Specifications

Table 24 provides the I²C (SCL < 100 KHz) timings.

Table 24. I²C Timing (SCL < 100 KHz)

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 200 | SCL clock frequency (slave) | 0.00 | 100.00 | KHz |
| 200 | SCL clock frequency (master) [1] | 1.50 | 100.00 | KHz |
| 202 | Bus free time between transmissions | 4.70 | — | µs |
| 203 | Low period of SCL | 4.70 | — | µs |
| 204 | High period of SCL | 4.00 | — | µs |
| 205 | Start condition setup time | 4.70 | — | µs |
| 206 | Start condition hold time | 4.00 | — | µs |
| 207 | Data hold time | 0.00 | — | µs |
| 208 | Data setup time | 250.00 | — | ns |
| 209 | SDL/SCL rise time | — | 1.00 | µs |

Table 24. I²C Timing (SCL < 100 KHz) (CONTINUED)

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 210 | SDL/SCL fall time | — | 300.00 | ns |
| 211 | Stop condition setup time | 4.70 | — | µs |

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I²C (SCL > 100 KHz) timings.

Table 25. I²C Timing (SCL > 100 KHz)

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master) [1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | | 1/(2.2 * fSCL) | — | s |
| 203 | Low period of SCL | | 1/(2.2 * fSCL) | — | s |
| 204 | High period of SCL | | 1/(2.2 * fSCL) | — | s |
| 205 | Start condition setup time | | 1/(2.2 * fSCL) | — | s |
| 206 | Start condition hold time | | 1/(2.2 * fSCL) | — | s |
| 207 | Data hold time | | 0 | — | s |
| 208 | Data setup time | | 1/(40 * fSCL) | — | s |
| 209 | SDL/SCL rise time | | — | 1/(10 * fSCL) | s |
| 210 | SDL/SCL fall time | | — | 1/(33 * fSCL) | s |
| 211 | Stop condition setup time | | 1/2(2.2 * fSCL) | — | s |

[1] SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 61 shows the I²C bus timing.

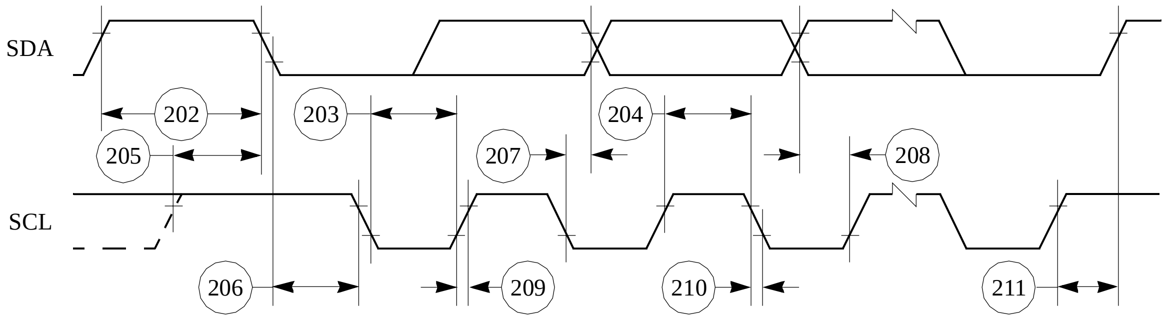


Figure 61. I²C Bus Timing Diagram

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

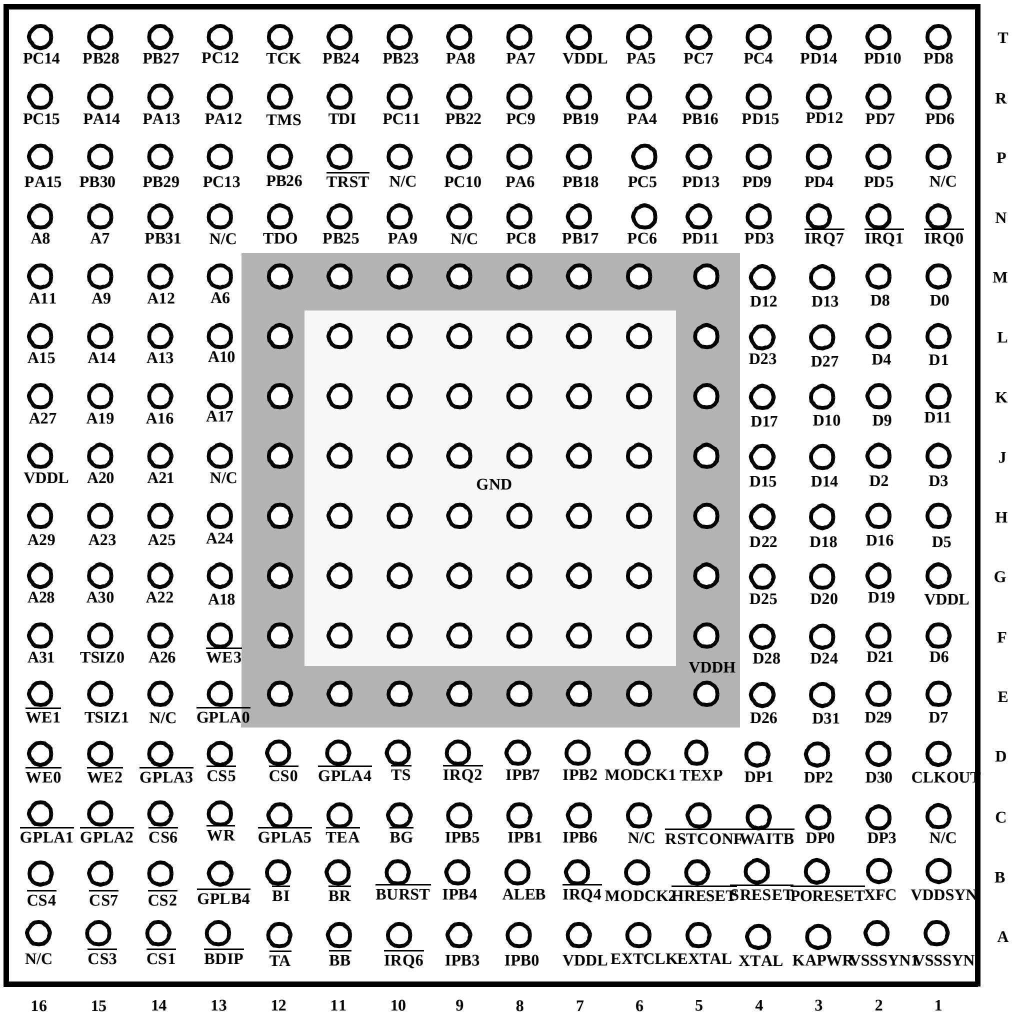


Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

## *How to Reach Us:*

**Home Page:**
www.freescale.com

**email:**
support@freescale.com

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

**For Literature Requests Only:**
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2005.