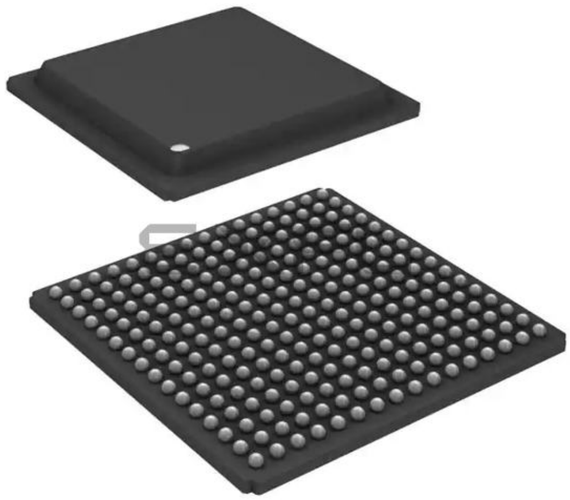


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc850zq80bu

- — Gate mode can enable/disable counting
- — Interrupt can be masked on reference match and event capture

- Interrupts
  - — Eight external interrupt request (IRQ) lines
  - — Twelve port pins with interrupt capability
  - — Fifteen internal interrupt sources
  - — Programmable priority among SCCs and USB
  - — Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - — Master (socket) interface, release 2.1 compliant
  - — Single PCMCIA socket
  - — Supports eight memory or I/O windows
- Communications processor module (CPM)
  - — 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - — Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - — Supports continuous mode transmission and reception on all serial channels
  - — Up to 8 Kbytes of dual-port RAM
  - — Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - — Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - — Can be connected to any SCC, SMC, or USB
  - — Allow changes during operation
  - — Autobaud support option
- Two SCCs (serial communications controllers)
  - — Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - — HDLC/SDLC™ (all channels supported at 2 Mbps)
  - — HDLC bus (implements an HDLC-based local area network (LAN))
  - — Asynchronous HDLC to support PPP (point-to-point protocol)
  - — AppleTalk®
  - — Universal asynchronous receiver transmitter (UART)
  - — Synchronous UART
  - — Serial infrared (IrDA)
  - — Totally transparent (bit streams)
  - — Totally transparent (frame based with optional cyclic redundancy check (CRC))

- QUICC multichannel controller (QMC) microcode features
  - Up to 64 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
  - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One $I^2C^®$ (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and CPM in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation

θ_{JA} = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$P_D = K \div (T_J + 273°C)$(2)

Solving equations (1) and (2) for K gives:

$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$(3)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

5.1 Layout Practices

Each V_{CC} pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0,1	—	8.00	—	8.00	—	8.00	—	50.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	—	50.00	ns
B24	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0.	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B24a	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE[0–3]}$ asserted	—	9.00	—	9.00	—	9.00	—	50.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	—	50.00	ns
B27	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	23.00	—	36.00	—	29.00	—	1.250	50.00	ns
B27a	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B28	CLKOUT rising edge to $\overline{WE[0–3]}$ negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	50.00	ns
B28a	CLKOUT falling edge to $\overline{WE[0–3]}$ negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	—	12.00	—	14.00	—	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B29h	$\overline{\text{WE}}$[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B29i	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B30	$\overline{\text{CS}}$, $\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access [9]	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B30a	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 0, CSNT =1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B30b	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B30c	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	8.00	—	6.00	—	0.375	50.00	ns
B30d	$\overline{\text{WE}}$[0–3] negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT =1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B42	CLKOUT rising edge to $\overline{\text{TS}}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B43	$\overline{\text{AS}}$ negation to memory controller signals negation	—	TBD	—	TBD	TBD	—	—	50.00	ns

[1] The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{\text{FFACTOR x 1000}}{F} + (D_{50} - 20 \text{ x FFACTOR})$$

For maxima:

$$D = \frac{\text{FFACTOR x 1000}}{F} + (D_{50} - 20 \text{ x FFACTOR}) + 1\text{ns(CAP LOAD - 50) / 10}$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

D_{50} is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

[2] Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.

[3] If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

[4] The timing for $\overline{\text{BR}}$ output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for $\overline{\text{BG}}$ output is relevant when the MPC850 is selected to work with internal bus arbiter.

[5] The setup times required for $\overline{\text{TA}}$, $\overline{\text{TEA}}$, and $\overline{\text{BI}}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).

[6] The timing required for $\overline{\text{BR}}$ input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the MPC850 is selected to work with the external bus arbiter.

[7] The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.

[8] The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

[9] The timing B30 refers to $\overline{\text{CS}}$ when ACS = '00' and to $\overline{\text{WE[0:3]}}$ when CSNT = '0'.

[10] The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.

[11] The $\overline{\text{AS}}$ signal is considered asynchronous to CLKOUT.

Figure 2 is the control timing diagram.

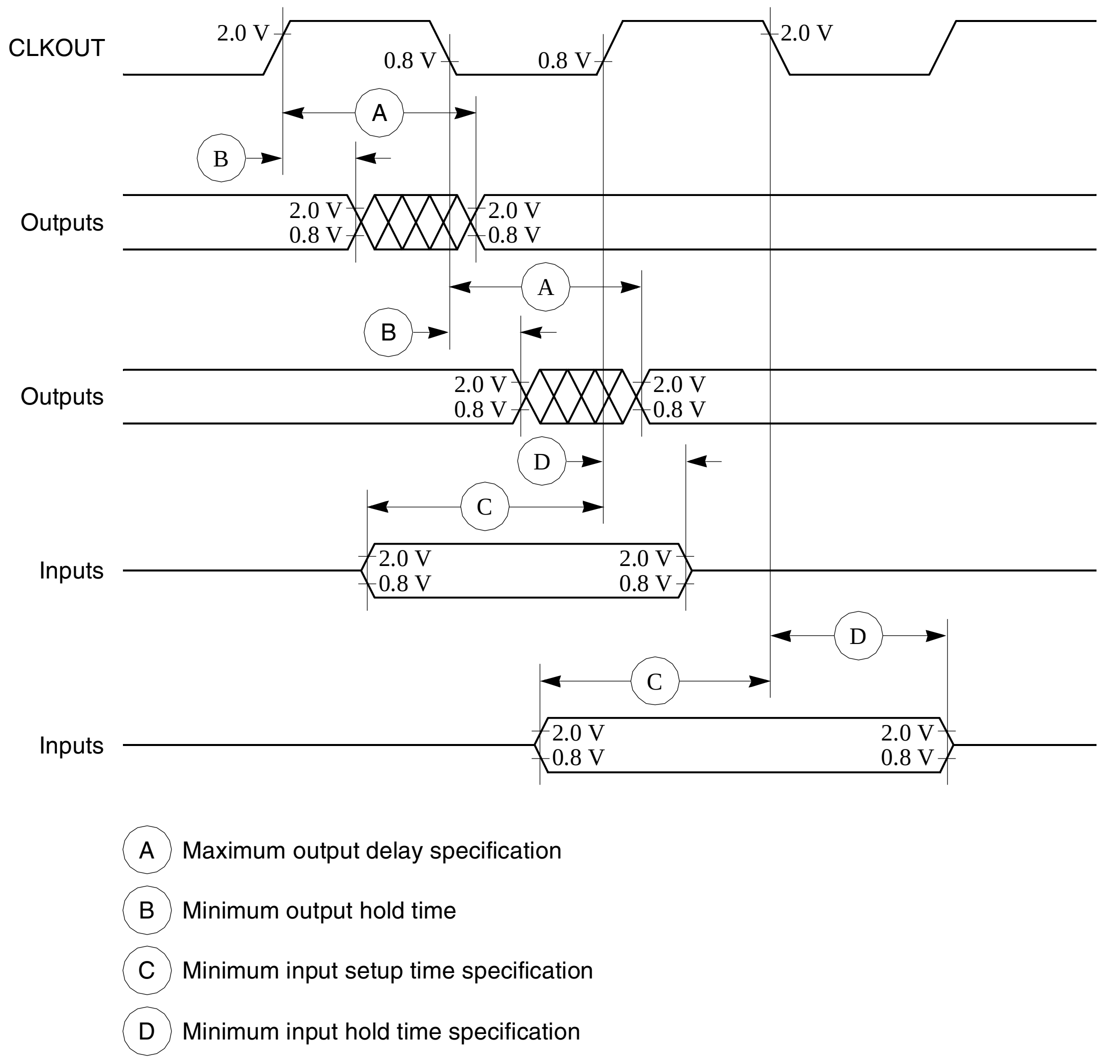


Figure 2. Control Timing

Figure 3 provides the timing for the external clock.

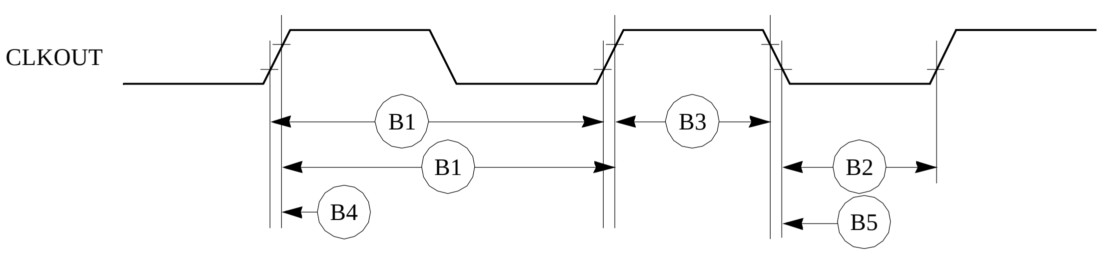


Figure 3. External Clock Timing

Figure 8 provides the timing for the input data controlled by the UPM in the memory controller.

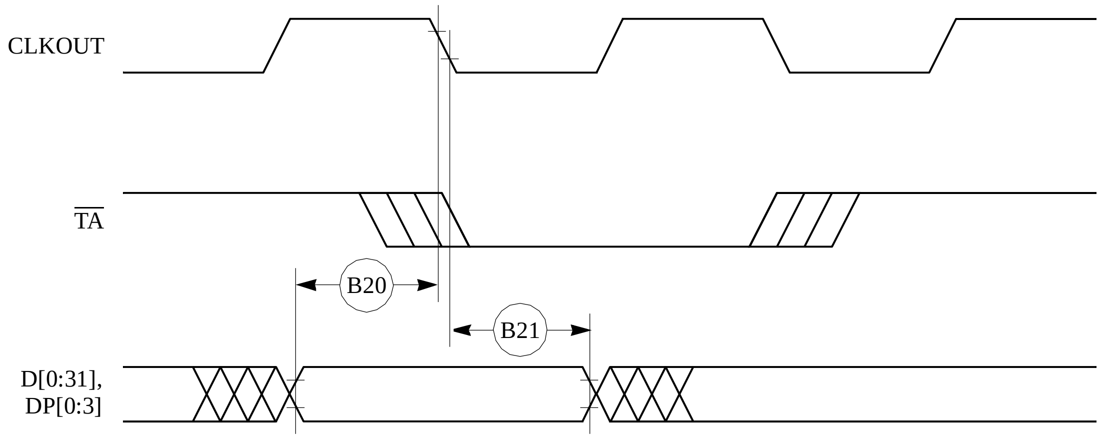


Figure 8. Input Data Timing when Controlled by UPM in the Memory Controller

Figure 9 through Figure 12 provide the timing for the external bus read controlled by various GPCM factors.

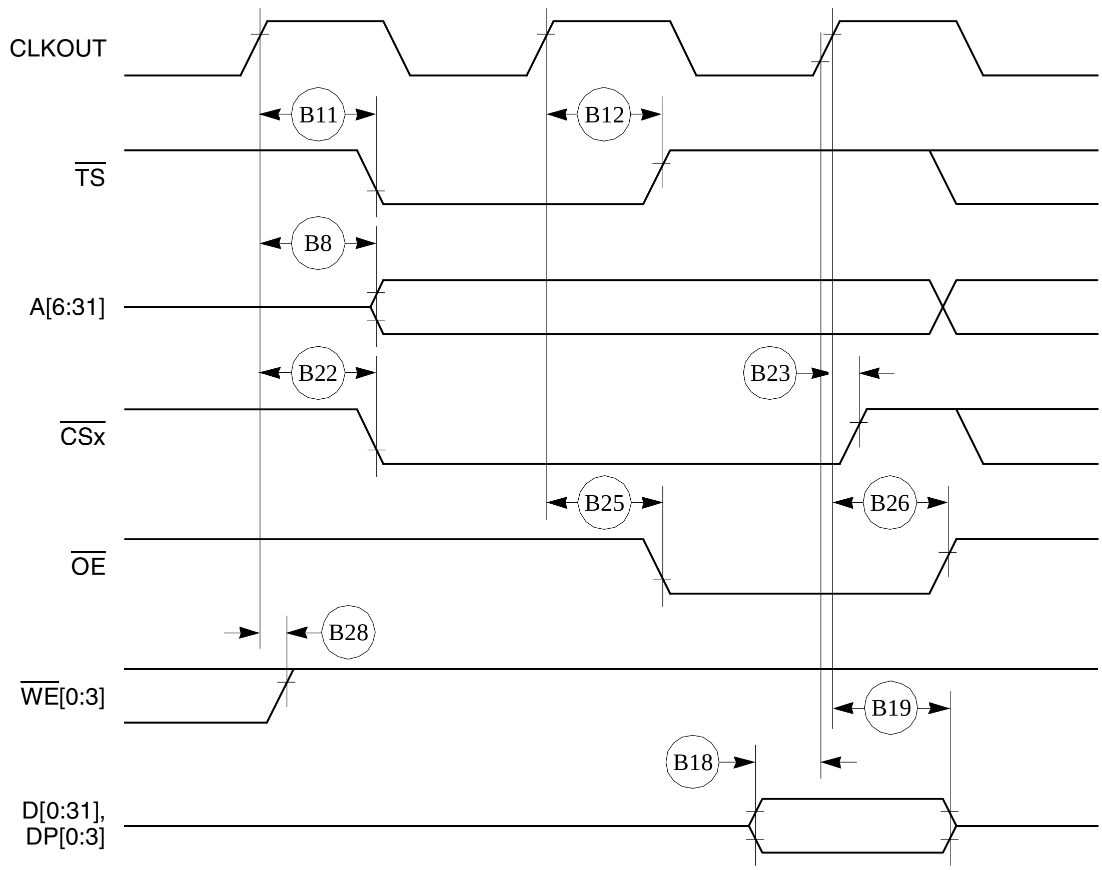


Figure 9. External Bus Read Timing (GPCM Controlled—ACS = 00)

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

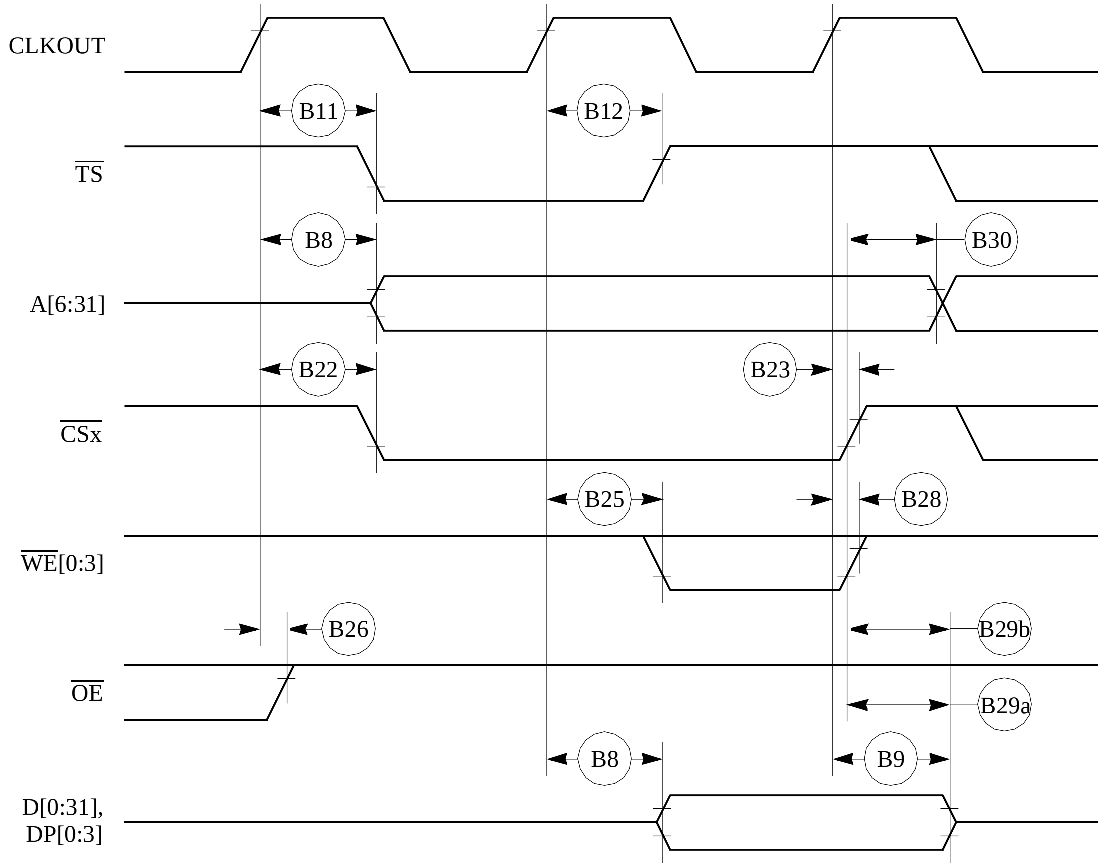


Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

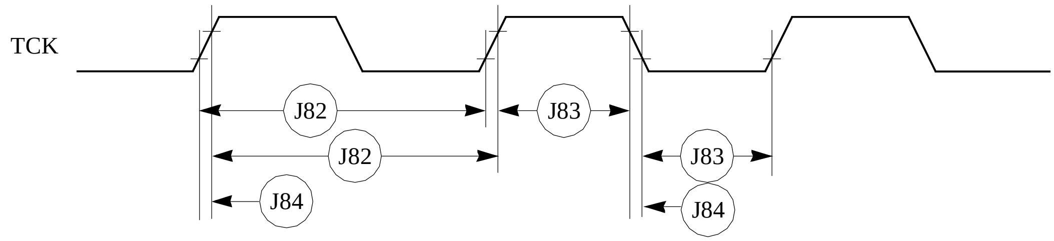


Figure 34. JTAG Test Clock Input Timing

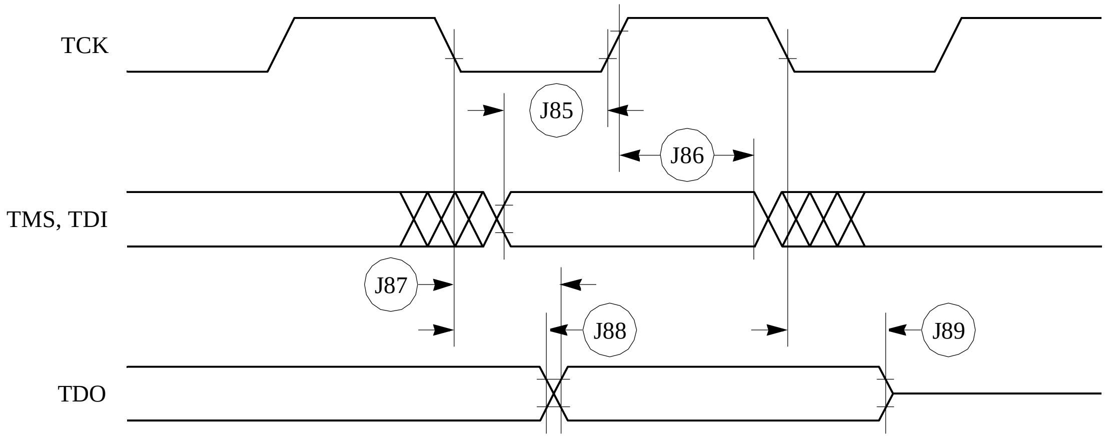


Figure 35. JTAG Test Access Port Timing Diagram

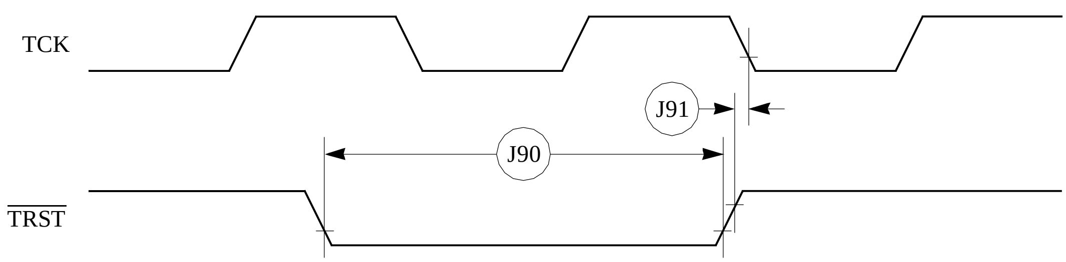


Figure 36. JTAG $\overline{\text{TRST}}$ Timing Diagram

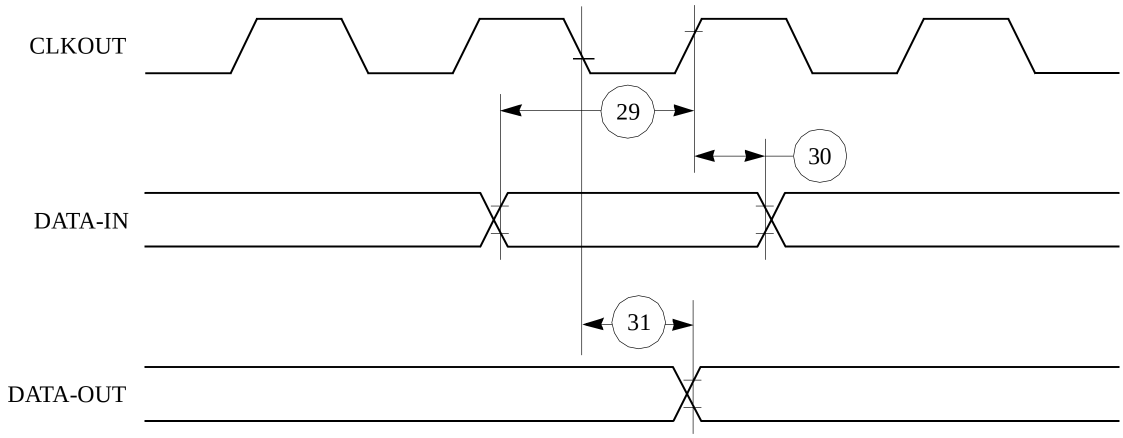


Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Table 14. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7.00	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3.00	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12.00	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12.00	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20.00	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15.00	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7.00	—	ns

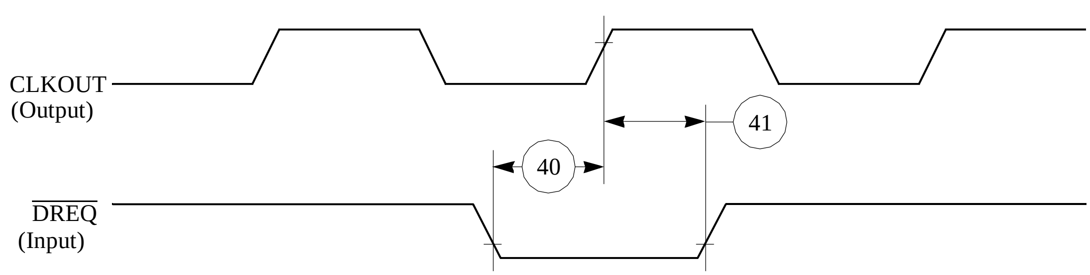


Figure 39. IDMA External Requests Timing Diagram

Table 17. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83A	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2 These specs are valid for IDL mode only.
3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.
4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

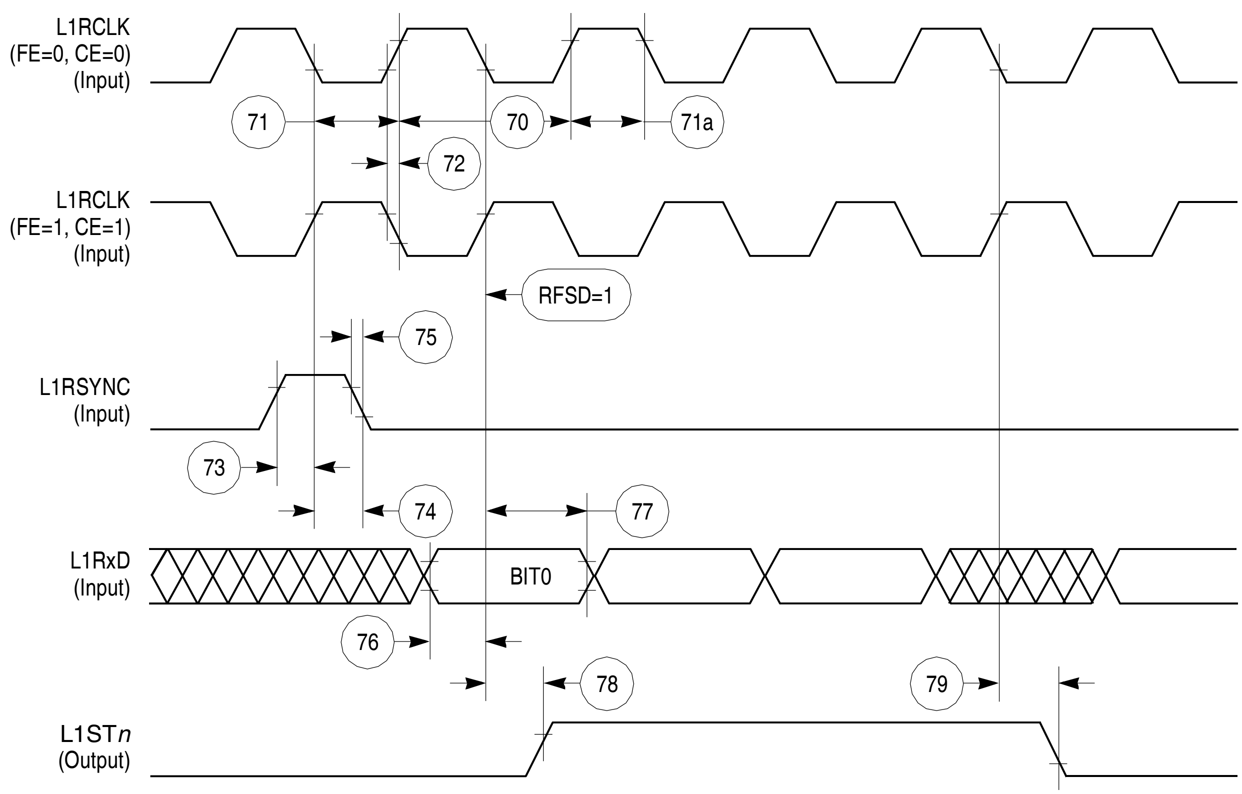


Figure 45. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

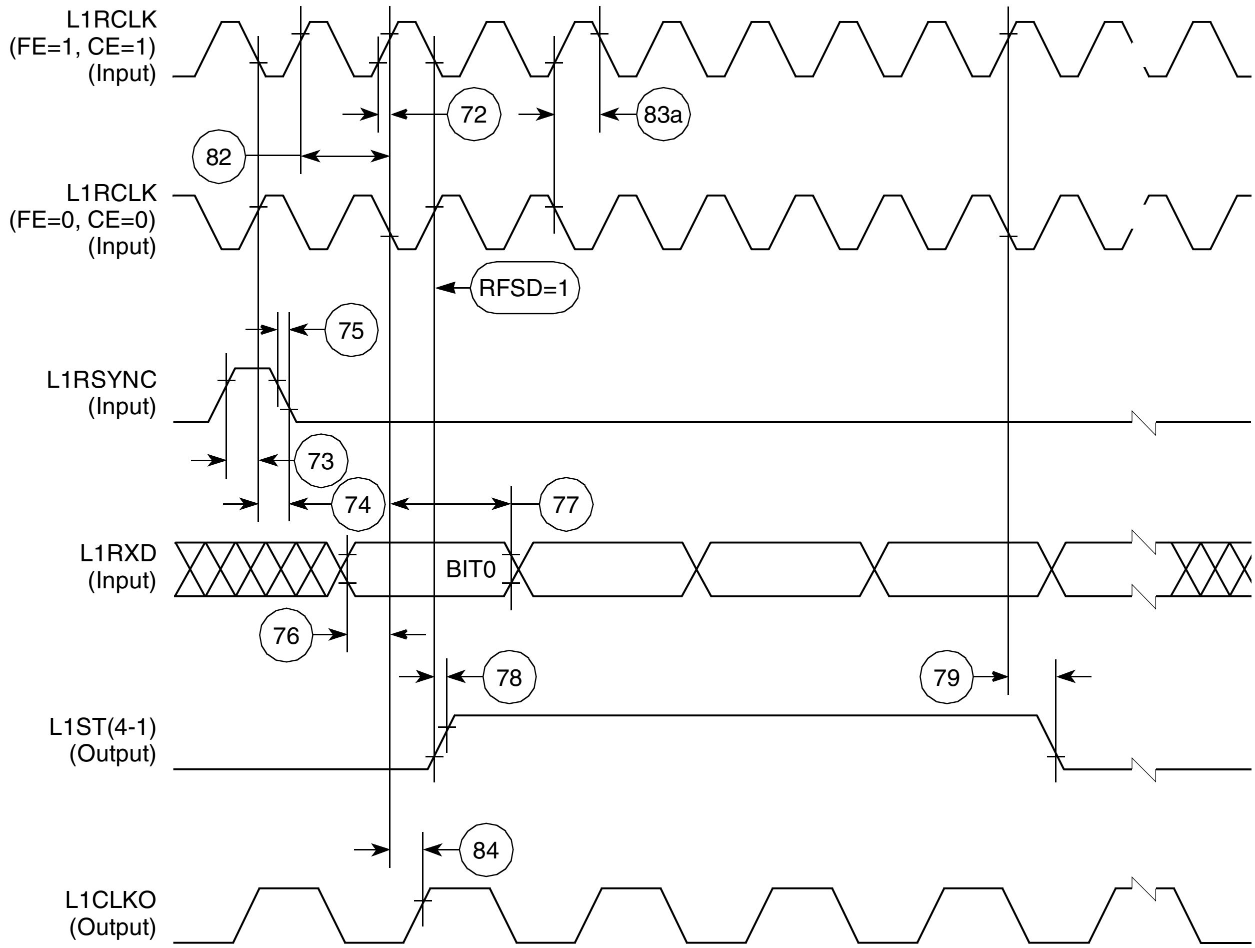


Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

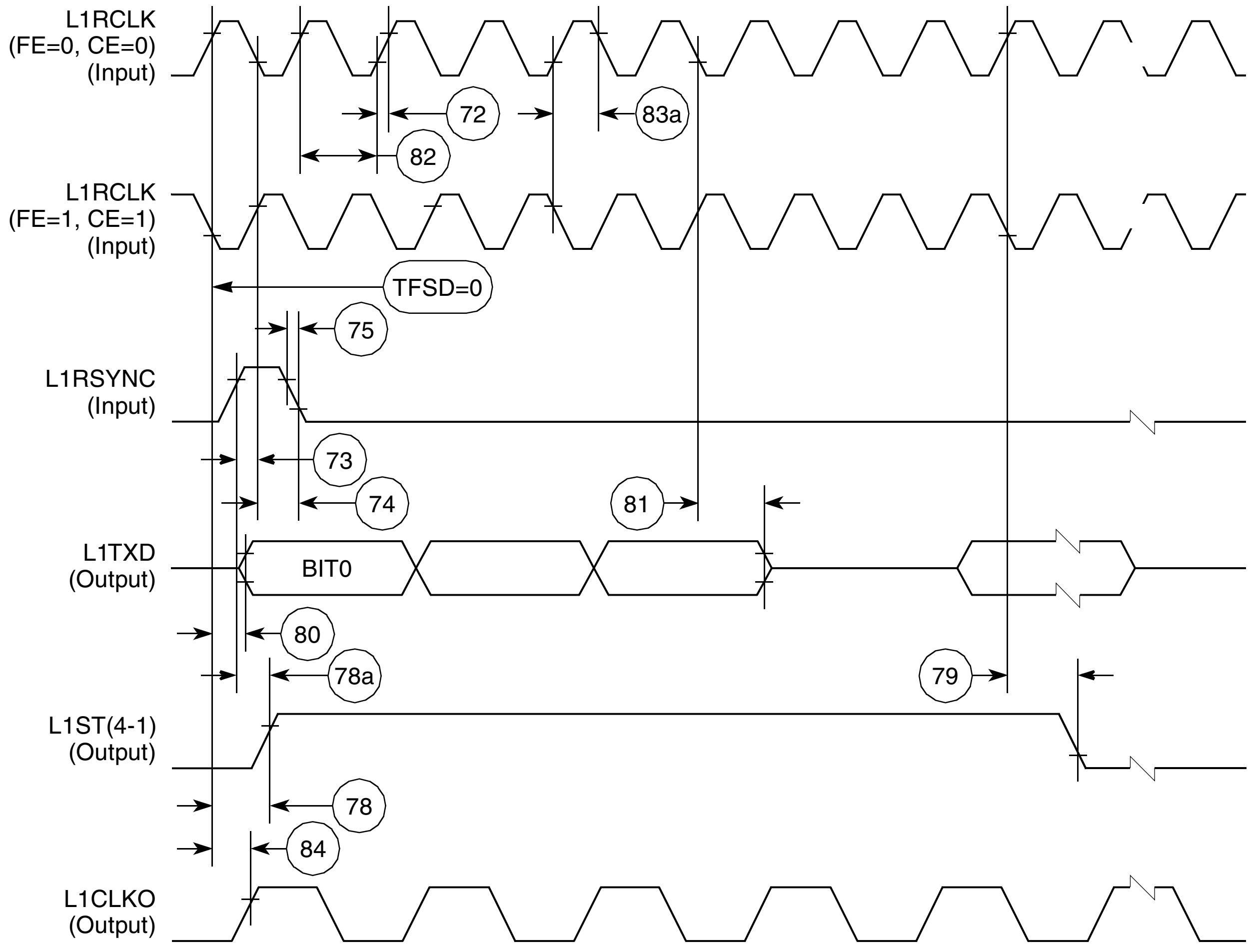


Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)

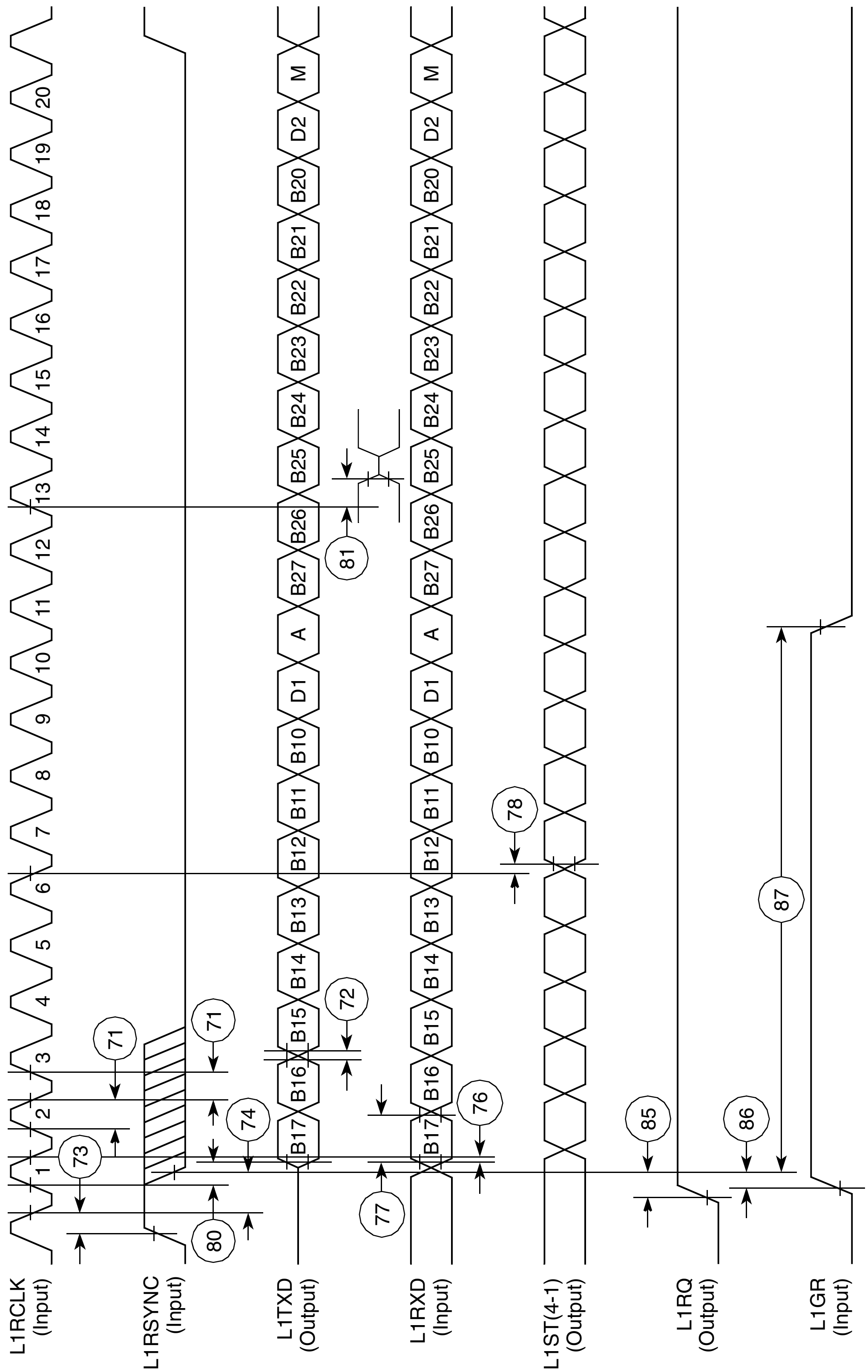
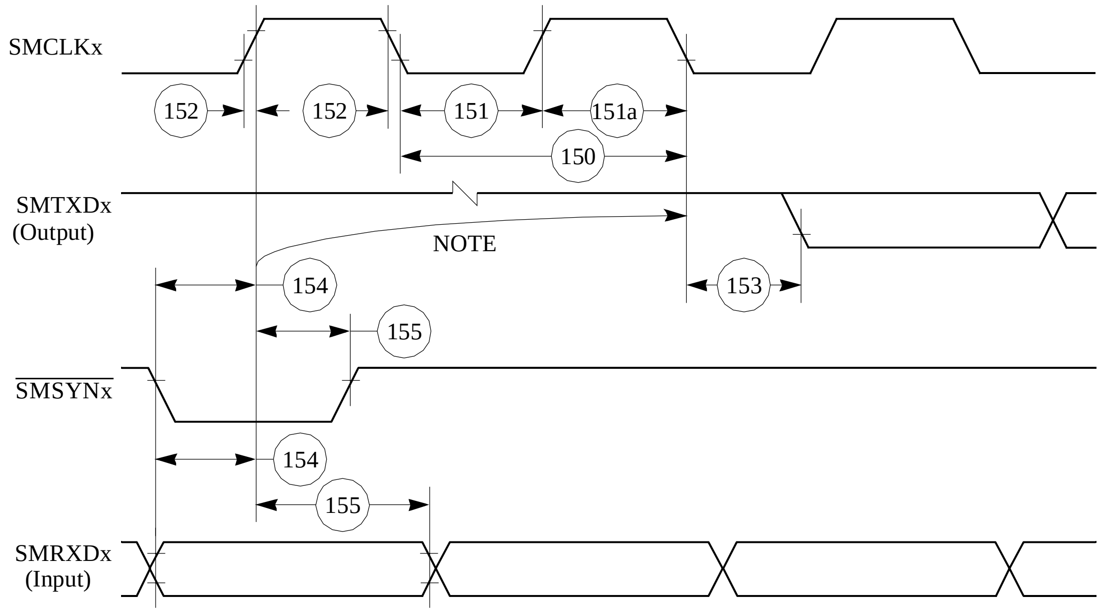


Figure 49. IDL Timing



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 56. SMC Transparent Timing Diagram

8.9 SPI Master AC Electrical Specifications

Table 22 provides the SPI master timings as shown in Figure 57 and Figure 58.

Table 22. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50.00	—	ns
163	Master data hold time (inputs)	0.00	—	ns
164	Master data valid (after SCK edge)	—	20.00	ns
165	Master data hold time (outputs)	0.00	—	ns
166	Rise time output	—	15.00	ns
167	Fall time output	—	15.00	ns

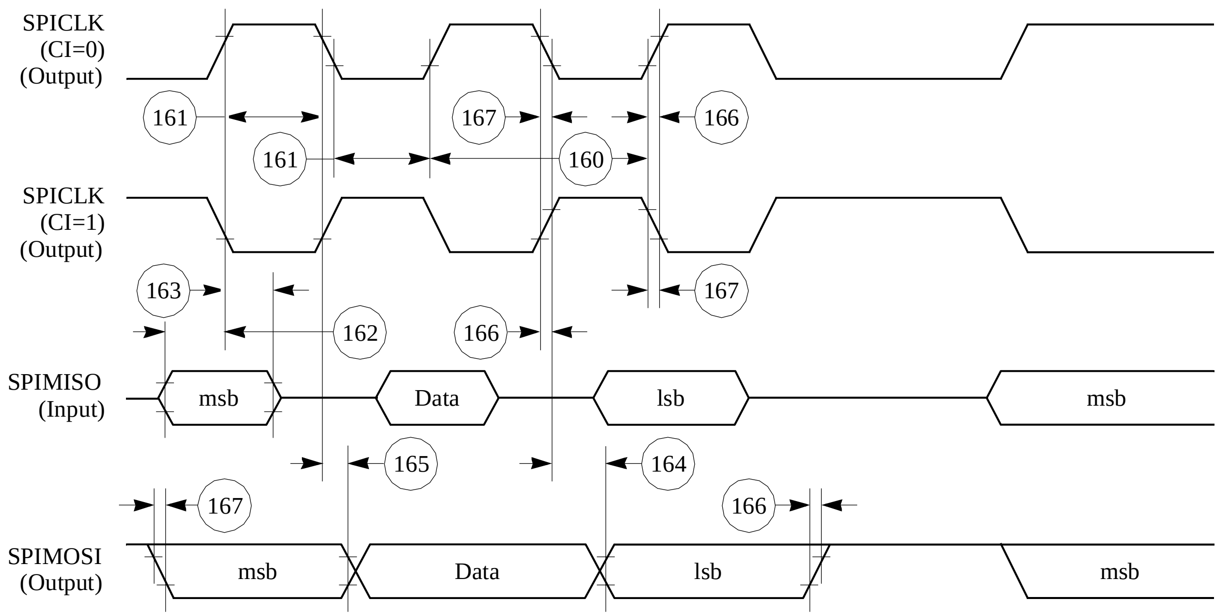


Figure 57. SPI Master (CP = 0) Timing Diagram

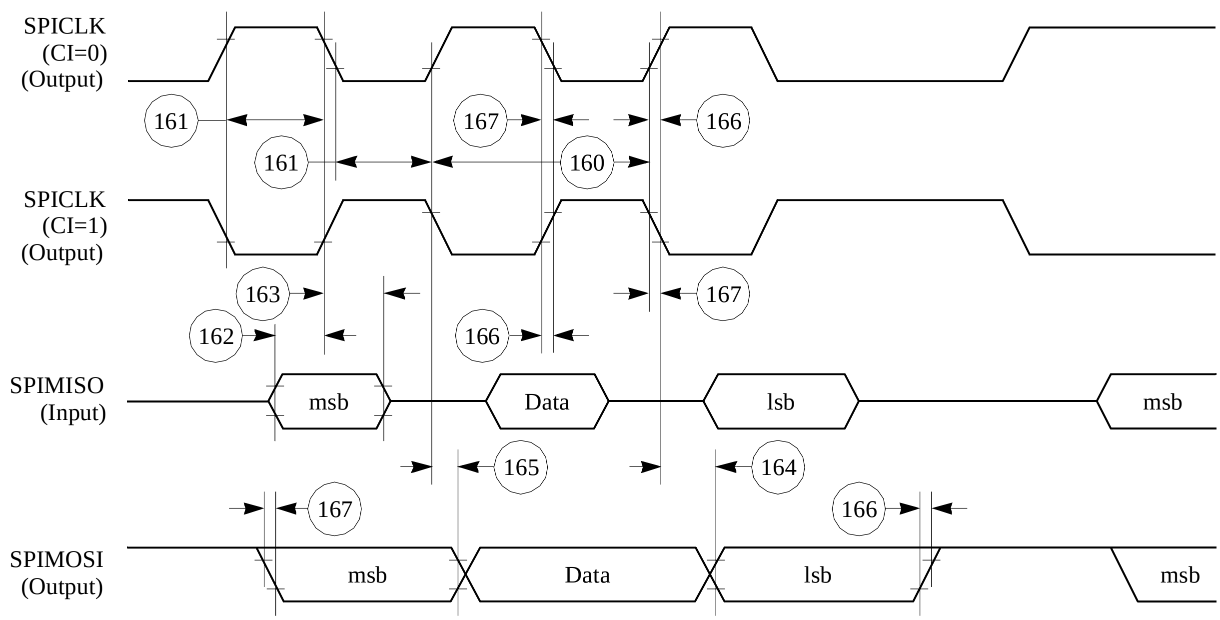


Figure 58. SPI Master (CP = 1) Timing Diagram

Table 24. I²C Timing (SCL < 100 KHz) (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
210	SDL/SCL fall time	—	300.00	ns
211	Stop condition setup time	4.70	—	µs

[1] SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I²C (SCL > 100 KHz) timings.

Table 25. I²C Timing (SCL > 100 KHz)

Num	Characteristic	Expression	All Frequencies		Unit
			Min	Max	
200	SCL clock frequency (slave)	fSCL	0	BRGCLK/48	Hz
200	SCL clock frequency (master) [1]	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus free time between transmissions		1/(2.2 * fSCL)	—	s
203	Low period of SCL		1/(2.2 * fSCL)	—	s
204	High period of SCL		1/(2.2 * fSCL)	—	s
205	Start condition setup time		1/(2.2 * fSCL)	—	s
206	Start condition hold time		1/(2.2 * fSCL)	—	s
207	Data hold time		0	—	s
208	Data setup time		1/(40 * fSCL)	—	s
209	SDL/SCL rise time		—	1/(10 * fSCL)	s
210	SDL/SCL fall time		—	1/(33 * fSCL)	s
211	Stop condition setup time		1/2(2.2 * fSCL)	—	s

[1] SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 61 shows the I²C bus timing.

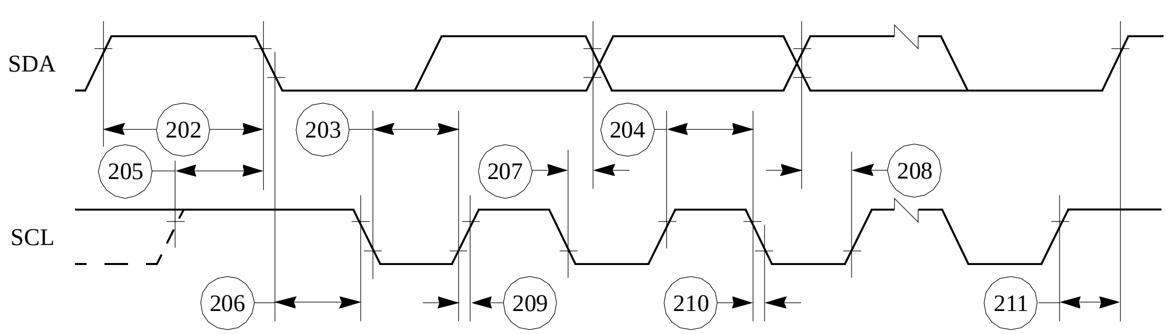


Figure 61. I²C Bus Timing Diagram

9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivatives

Device	Ethernet Support	Number of SCCs [1]	32-Channel HDLC Support	64-Channel HDLC Support [2]
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

1 Serial Communication Controller (SCC)

2 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

THIS PAGE INTENTIONALLY LEFT BLANK