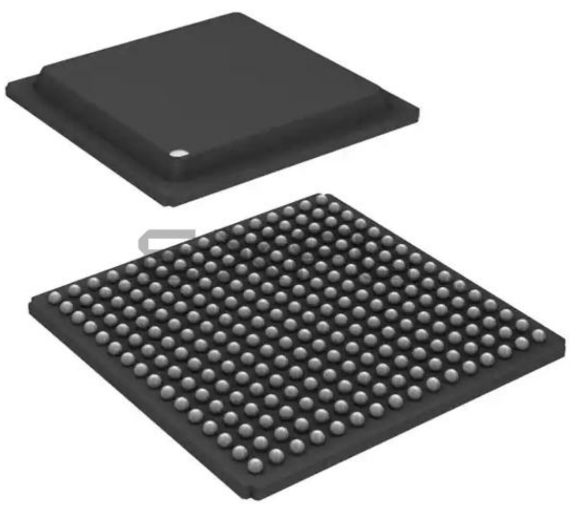
# NXP USA Inc. - XPC850CVR50BU Datasheet



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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 50MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 256-BBGA |
| Supplier Device Package | 256-PBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850cvr50bu |

  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

  - Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
  - Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - The MPC850 can compare using the =, ≠, <, and > conditions to generate watchpoints
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility on all general purpose I/O pins.

# 3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC850. Table 2 provides the maximum ratings.

**Table 2. Maximum Ratings**

(GND = 0V)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | VDDH | -0.3 to 4.0 | V |
| | VDDL | -0.3 to 4.0 | V |
| | KAPWR | -0.3 to 4.0 | V |
| | VDDSYN | -0.3 to 4.0 | V |
| Input voltage [1] | $V_{in}$ | GND-0.3 to VDDH + 2.5 V | V |
| Junction temperature [2] | $T_j$ | 0 to 95 (standard)<br>-40 to 95 (extended) | °C |
| Storage temperature range | $T_{stg}$ | -55 to +150 | °C |

[1] Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
CAUTION: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC850 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

[2] The MPC850, a high-frequency device in a BGA package, does not provide a guaranteed maximum ambient temperature. Only maximum junction temperature is guaranteed. It is the responsibility of the user to consider power dissipation and thermal management. Junction temperature ratings are the same regardless of frequency rating of the device.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{CC}$). Table 3 provides the package thermal characteristics for the MPC850.

**Table 5. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input low voltage | VIL | GND | 0.8 | V |
| EXTAL, EXTCLK input high voltage | VIHC | 0.7*(VCC) | VCC+0.3 | V |
| Input leakage current, Vin = 5.5 V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins) | $I_{in}$ | — | 100 | µA |
| Input leakage current, Vin = 3.6V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input leakage current, Vin = 0V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input capacitance | $C_{in}$ | — | 20 | pF |
| Output high voltage, IOH = -2.0 mA, VDDH = 3.0V<br>except XTAL, XFC, and open-drain pins | VOH | 2.4 | — | V |
| Output low voltage<br>CLKOUT [3]<br>IOL = 3.2 mA [1]<br>IOL = 5.3 mA [2]<br>IOL = 7.0 mA PA[14]/$\overline{\text{USBOE}}$, PA[12]/TXD2<br>IOL = 8.9 mA $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$ | VOL | — | 0.5 | V |

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[1] A[6:31], TSIZ0/REG, TSIZ1, D[0:31], DP[0:3]/IRQ[3:6], RD/WR, BURST, RSV/IRQ2, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, PA[15]/USBRXD, PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/TOUT1/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/TOUT2/TIN4, PB[31]/SPISEL, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/BRGO1, PB[26]/I2CSCL/BRGO2, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/SDACK1, PB[22]/SMSYN2/SDACK2, PB[19]/L1ST1, PB[18]/RTS2/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/DREQ0/L1ST5, PC[14]/DREQ1/RTS2/L1ST6, PC[13]/L1ST7/RTS3, PC[12]/L1RQa/L1ST8, PC[11]/USBRXP, PC[10]/TGATE1/USBRXN, PC[9]/CTS2, PC[8]/CD2/TGATE1, PC[7]/USBTXP, PC[6]/USBTXN, PC[5]/CTS3/L1TSYNCA/SDACK1, PC[4]/CD3/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

[2] BDIP/GPL_B5, BR, BG, FRZ/IRQ6, CS[0:5], CS6/CE1_B, CS7/CE2_B, WE0/BS_AB0/IORD, WE1/BS_AB1/IOWR, WE2/BS_AB2/PCOE, WE3/BS_AB3/PCWE, GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A[2:3]/GPL_B[2:3]/CS[2:3], UPWAITA/GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/DSCK/AT1, OP2/MODCK1/STS, OP3/MODCK2/DSDO

3 The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, IOH and IOL for Clkout should be extracted from the IBIS model at any output voltage level.

# 5 Power Considerations

The average chip-junction temperature, $T_J$, in °C can be obtained from the equation:

$T_J = T_A + (P_D \bullet \theta_{JA})$(1)

where

$T_A$ = Ambient temperature, °C

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B29h | $\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1 | 25.00 | — | 39.00 | — | 31.00 | — | 1.375 | 50.00 | ns |
| B29i | $\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 25.00 | — | 39.00 | — | 31.00 | — | 1.375 | 50.00 | ns |
| B30 | $\overline{\text{CS}}$, $\overline{\text{WE[0–3]}}$ negated to A[6–31] invalid<br>GPCM write access [9] | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B30a | $\overline{\text{WE[0–3]}}$ negated to A[6–31] invalid<br>GPCM write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 0, CSNT =1, ACS = 10 or ACS = 11, EBDF = 0 | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B30b | $\overline{\text{WE[0–3]}}$ negated to A[6–31] invalid<br>GPCM write access, TRLX = 1, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 | 28.00 | — | 43.00 | — | 36.00 | — | 1.500 | 50.00 | ns |
| B30c | $\overline{\text{WE[0–3]}}$ negated to A[6–31] invalid<br>GPCM write access, TRLX = 0, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 5.00 | — | 8.00 | — | 6.00 | — | 0.375 | 50.00 | ns |
| B30d | $\overline{\text{WE[0–3]}}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT =1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 | 25.00 | — | 39.00 | — | 31.00 | — | 1.375 | 50.00 | ns |

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B33a | CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B34 | A[6–31] and D[0–31] to $\overline{\text{CS}}$ valid - as requested by control bit CST4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B34a | A[6–31] and D[0–31] to $\overline{\text{CS}}$ valid - as requested by control bit CST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B34b | A[6–31] and D[0–31] to $\overline{\text{CS}}$ valid - as requested by CST2 in the corresponding word in UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B35 | A[6–31] to $\overline{\text{CS}}$ valid - as requested by control bit BST4 in the corresponding word in UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B35a | A[6–31] and D[0–31] to $\overline{\text{BS}}$ valid - as requested by BST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B35b | A[6–31] and D[0–31] to $\overline{\text{BS}}$ valid - as requested by control bit BST2 in the corresponding word in the UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B36 | A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B37 | UPWAIT valid to CLKOUT falling edge [10] | 6.00 | — | 6.00 | — | 6.00 | — | — | 50.00 | ns |
| B38 | CLKOUT falling edge to UPWAIT valid [10] | 1.00 | — | 1.00 | — | 1.00 | — | — | 50.00 | ns |
| B39 | $\overline{\text{AS}}$ valid to CLKOUT rising edge [11] | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B40 | A[6–31], TSIZ[0–1], RD/$\overline{\text{WR}}$, $\overline{\text{BURST}}$, valid to CLKOUT rising edge. | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B41 | $\overline{\text{TS}}$ valid to CLKOUT rising edge (setup time) | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |

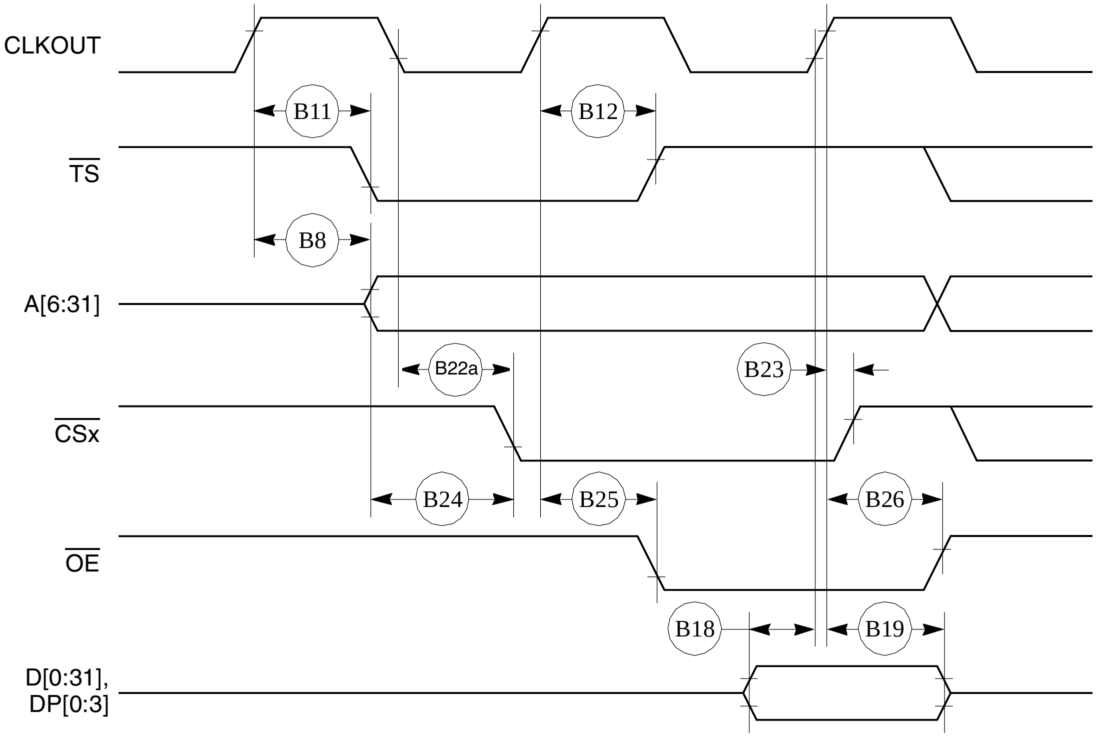


Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

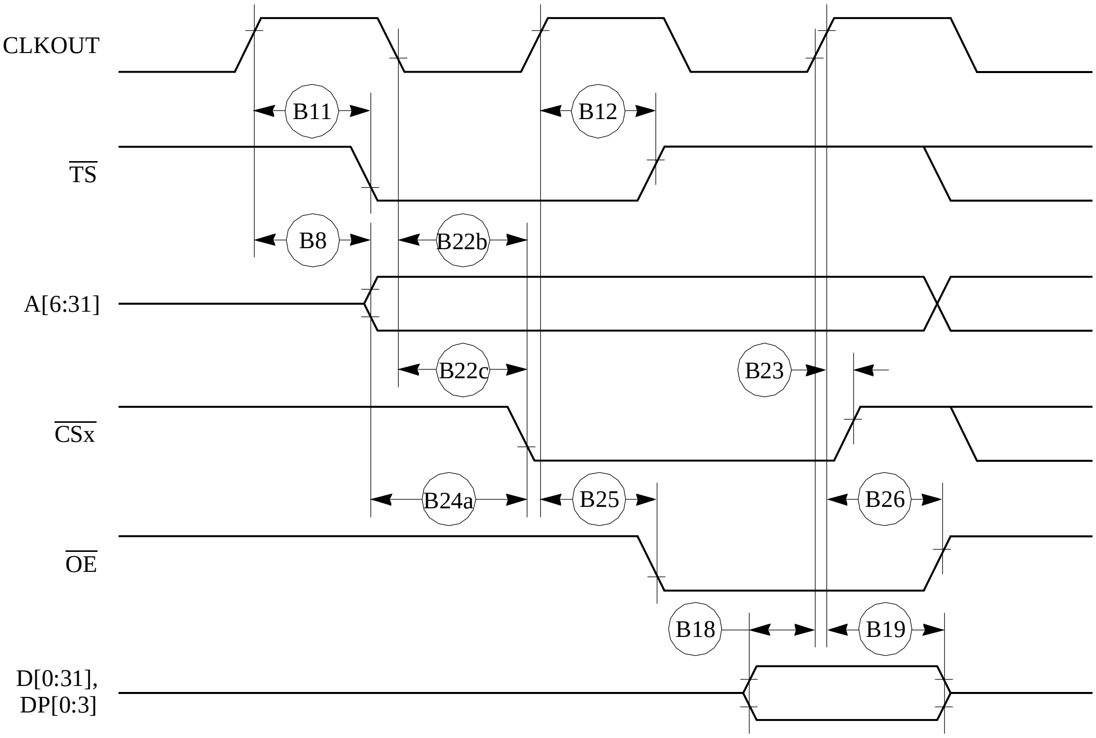


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

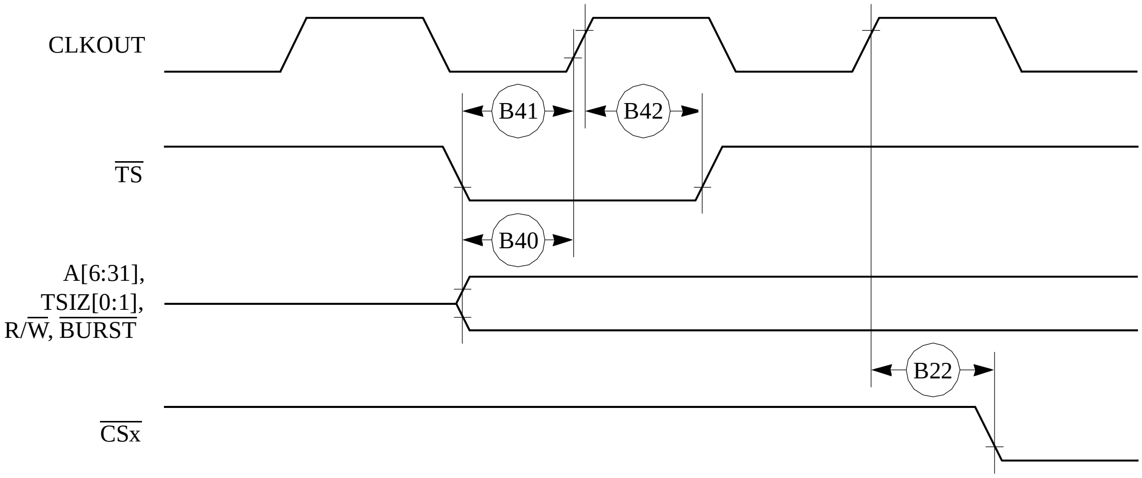


**Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)**

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.

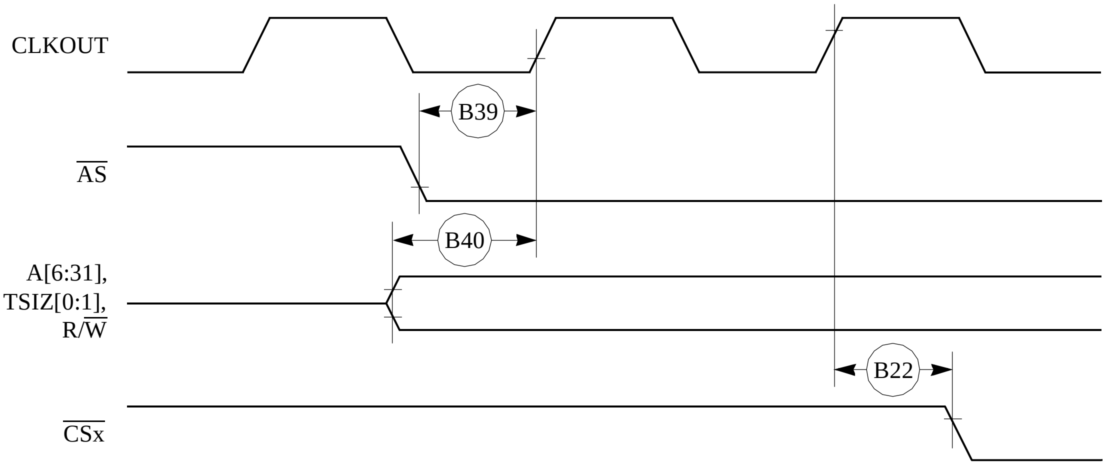


**Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)**

Figure 21 provides the timing for the asynchronous external master control signals negation.

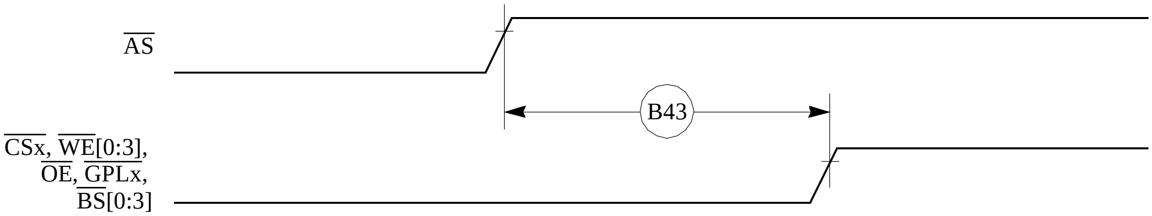


**Figure 21. Asynchronous External Master—Control Signals Negation Timing**

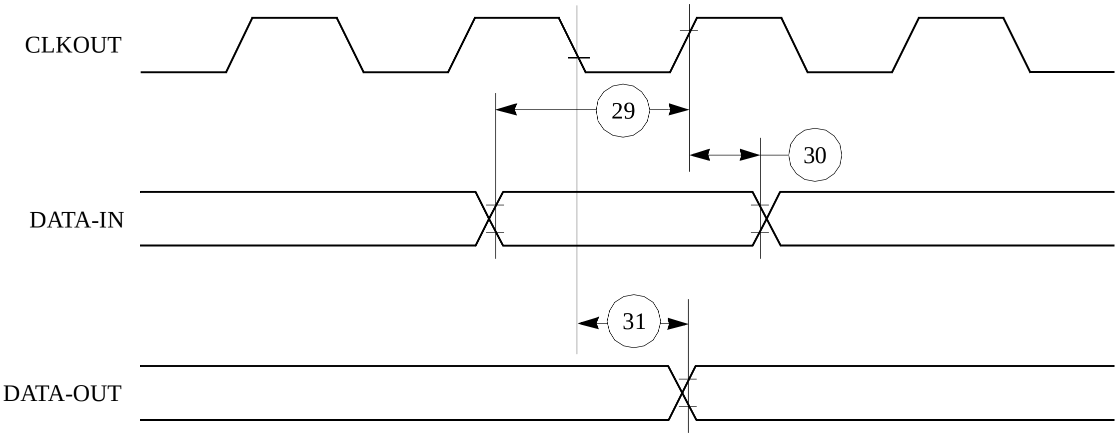


**Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram**

## 8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

**Table 14. IDMA Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7.00 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high | 3.00 | — | ns |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12.00 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12.00 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20.00 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15.00 | ns |
| 46 | $\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7.00 | — | ns |

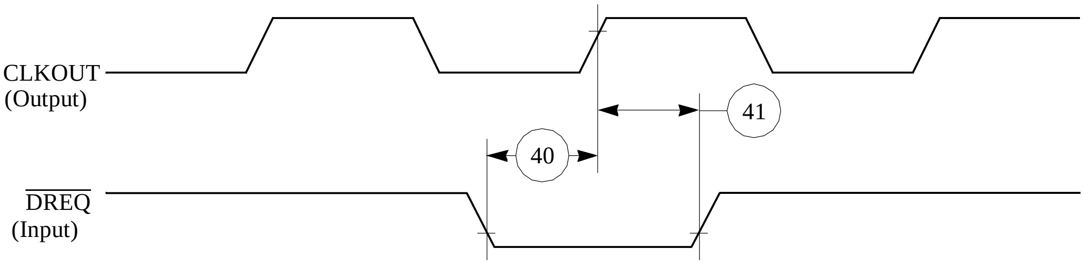


**Figure 39. IDMA External Requests Timing Diagram**

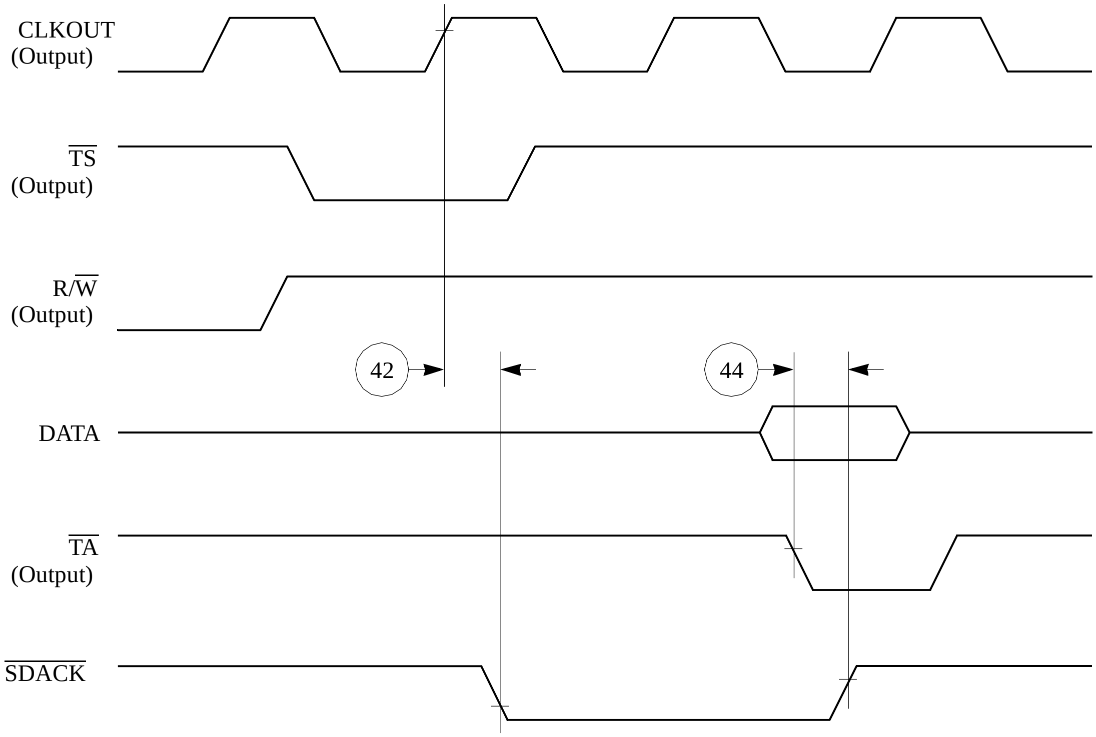


**Figure 41. SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock**

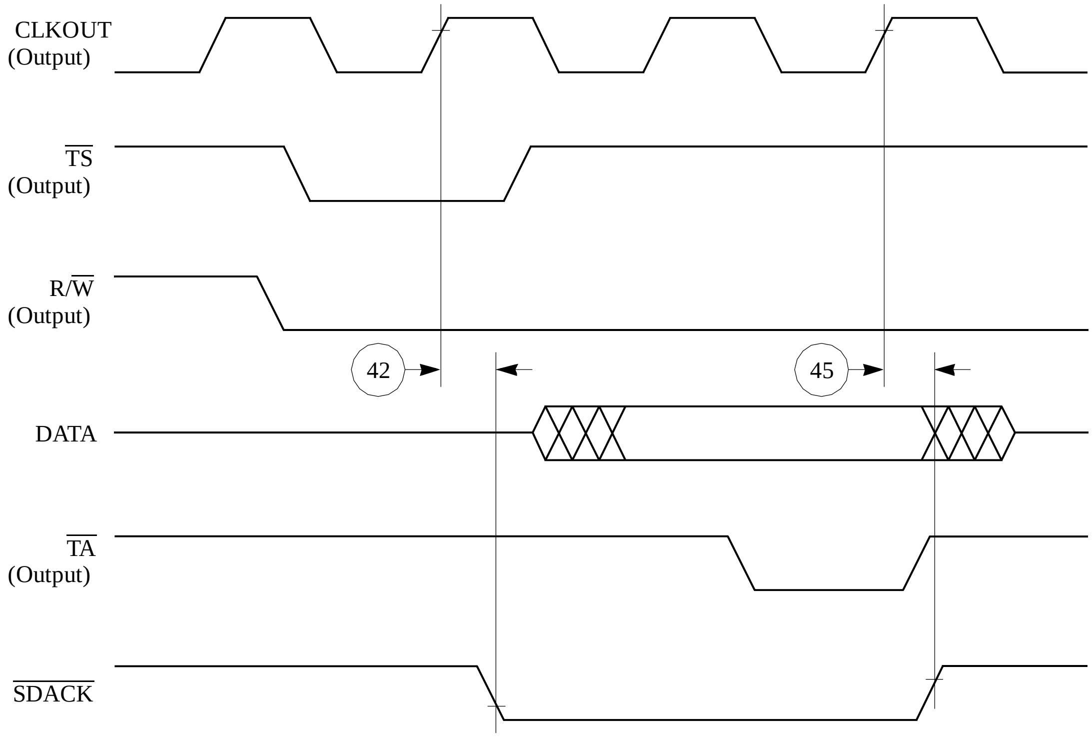


**Figure 42. SDACK Timing Diagram—Peripheral Read**

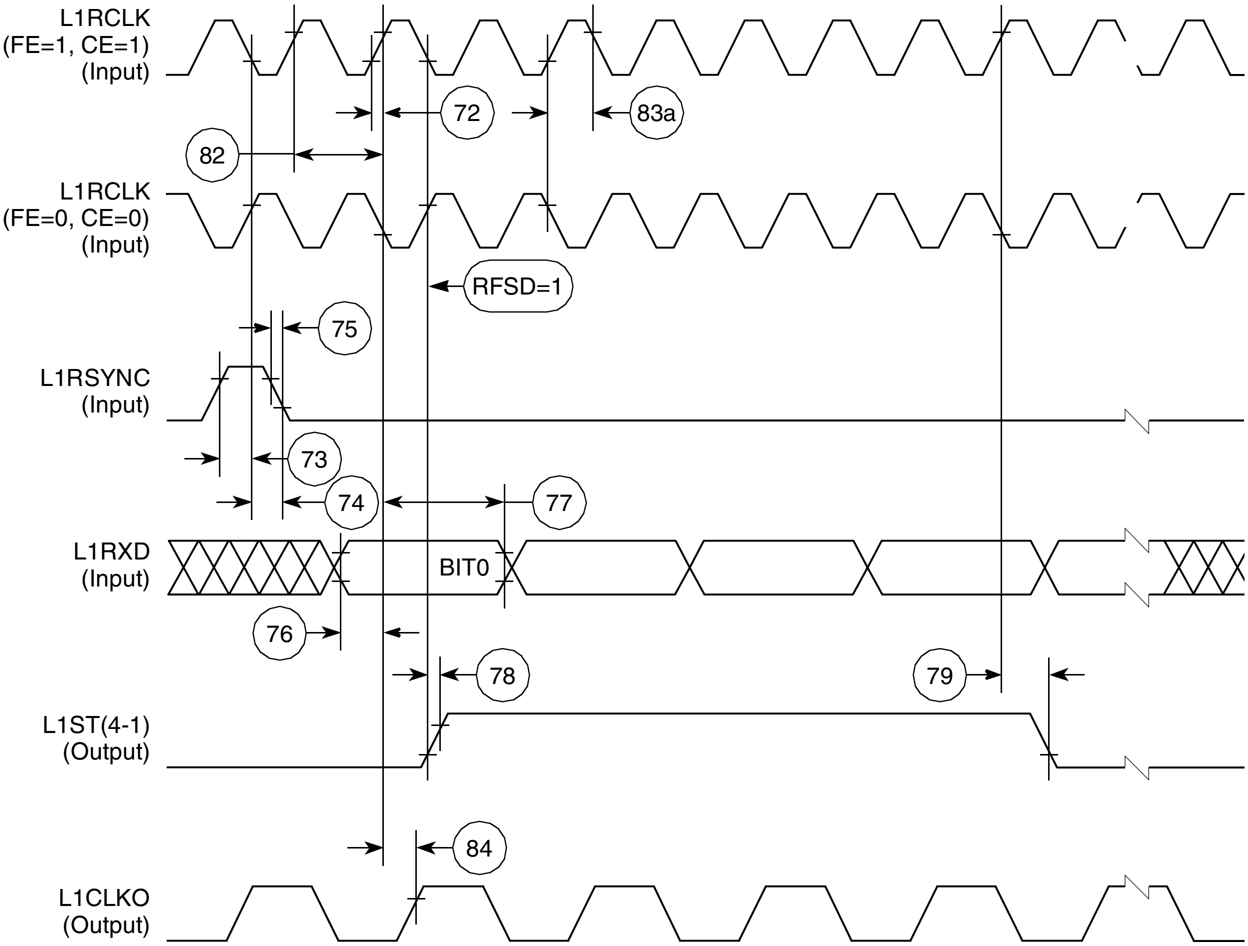


Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

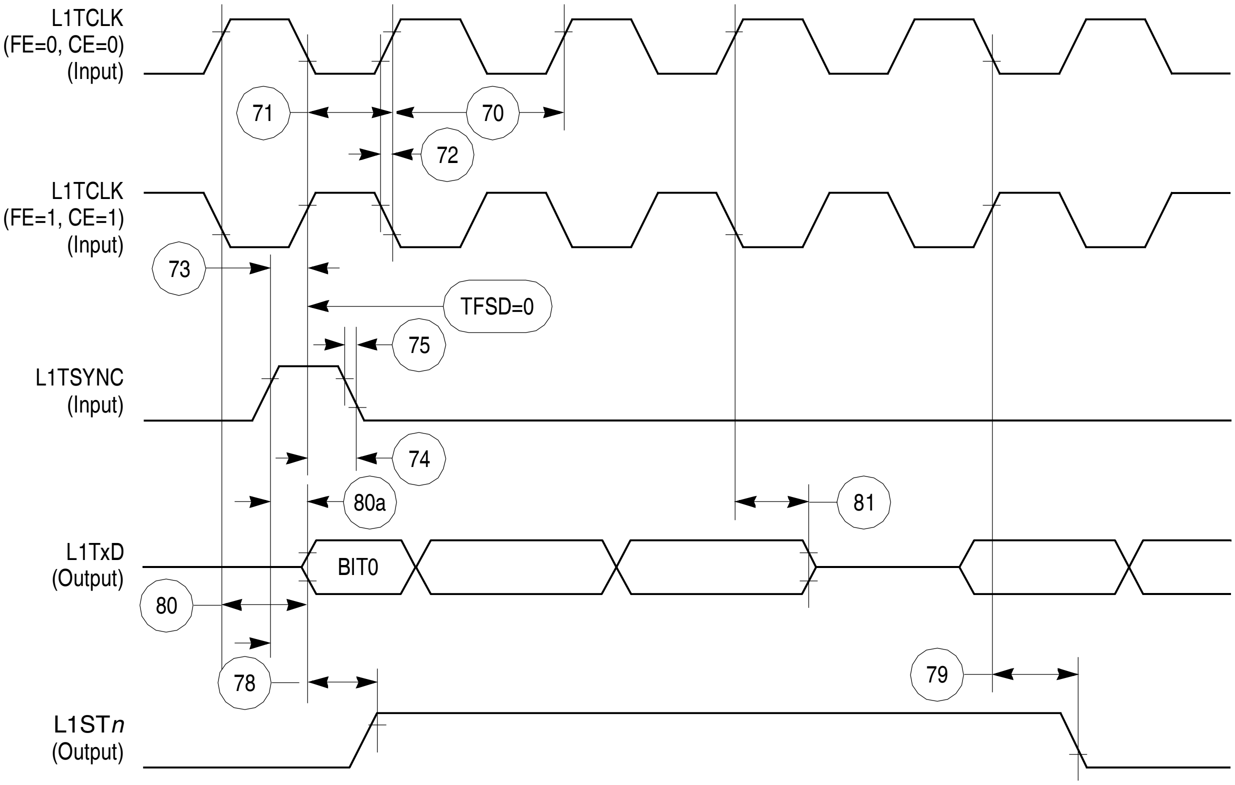


Figure 47. SI Transmit Timing Diagram

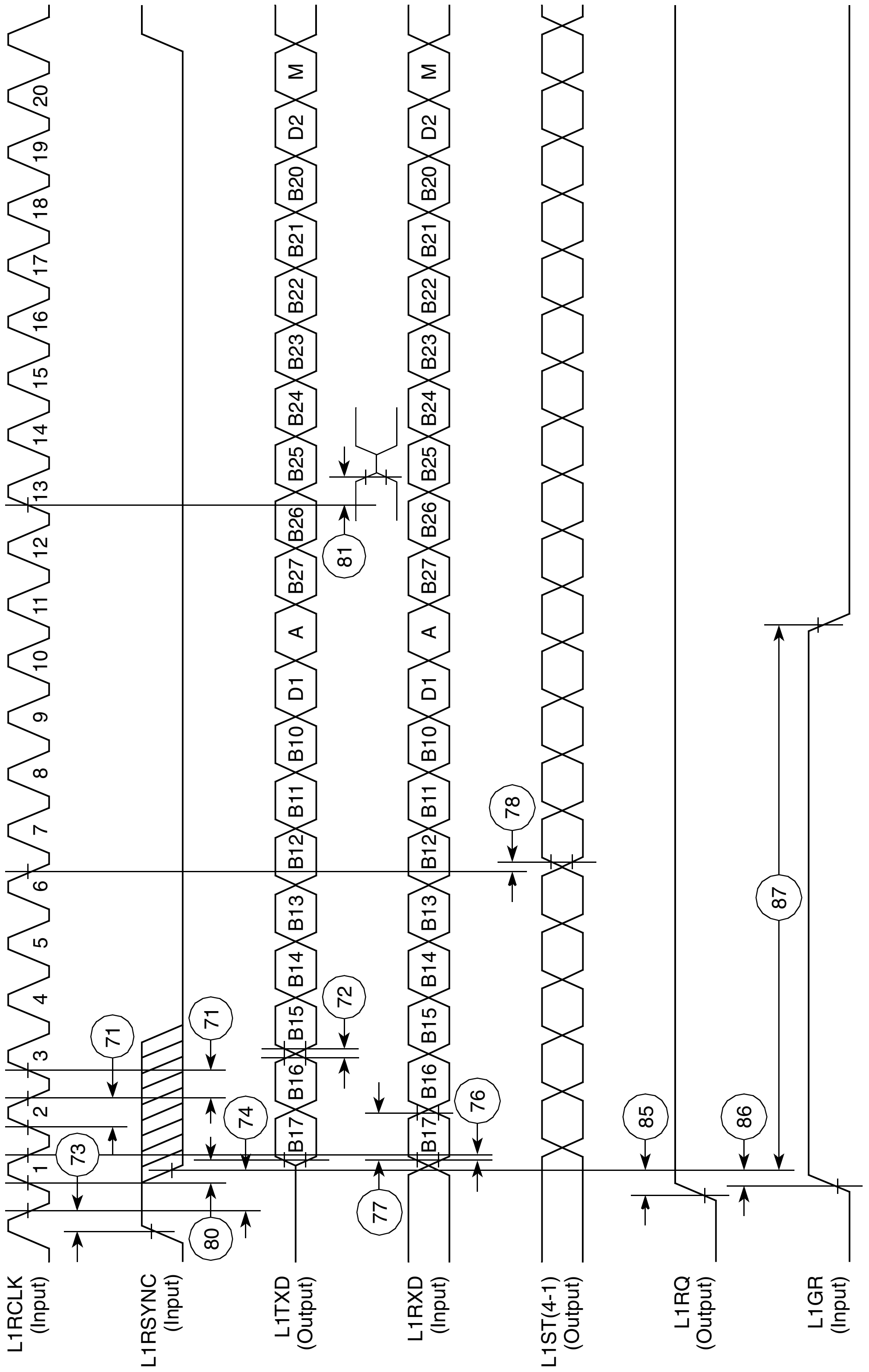


Figure 49. IDL Timing

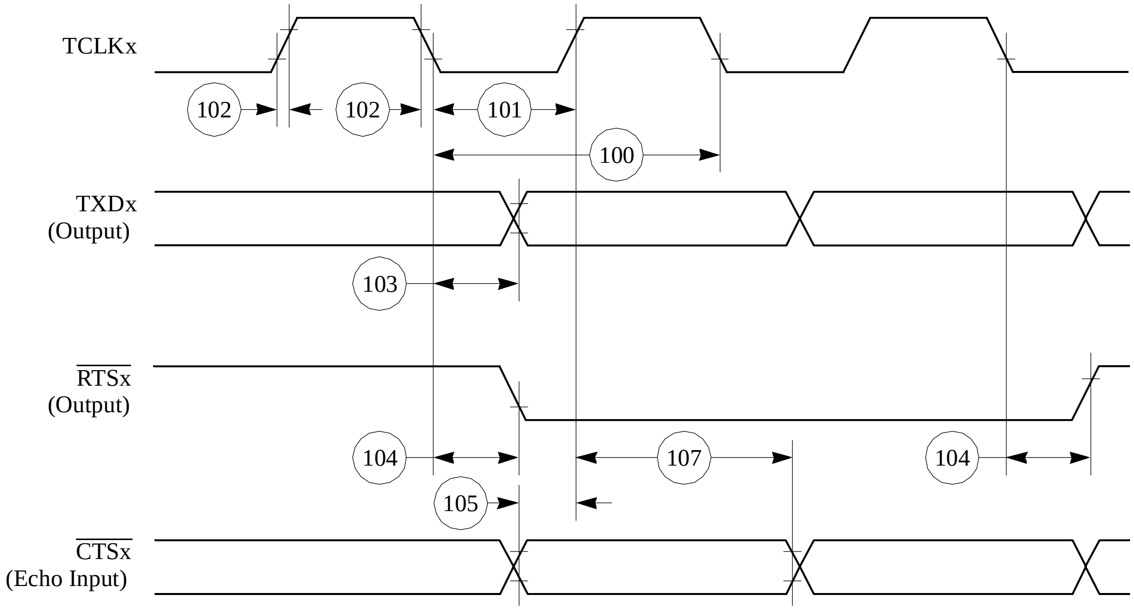


Figure 52. HDLC Bus Timing Diagram

## 8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40.00 | — | ns |
| 121 | RCLKx rise/fall time (x = 2, 3 for all specs in this table) | — | 15.00 | ns |
| 122 | RCLKx width low | 40.00 | — | ns |
| 123 | RCLKx clock period [1] | 80.00 | 120.00 | ns |
| 124 | RXDx setup time | 20.00 | — | ns |
| 125 | RXDx hold time | 5.00 | — | ns |
| 126 | RENA active delay (from RCLKx rising edge of the last data bit) | 10.00 | — | ns |
| 127 | RENA width low | 100.00 | — | ns |
| 128 | TCLKx rise/fall time | — | 15.00 | ns |
| 129 | TCLKx width low | 40.00 | — | ns |
| 130 | TCLKx clock period[1] | 99.00 | 101.00 | ns |
| 131 | TXDx active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 132 | TXDx inactive delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 133 | TENA active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |

Table 20. Ethernet Timing (continued)

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 134 | TENA inactive delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 138 | CLKOUT low to $\overline{\text{SDACK}}$ asserted [2] | — | 20.00 | ns |
| 139 | CLKOUT low to $\overline{\text{SDACK}}$ negated [2] | — | 20.00 | ns |

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame destination address into memory.

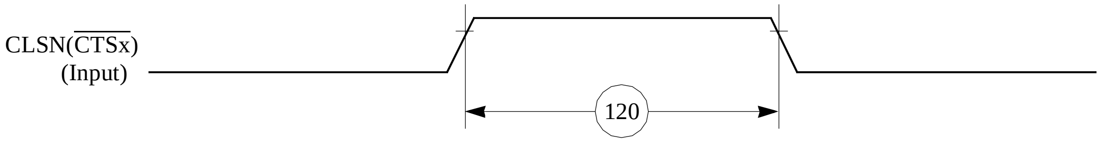


Figure 53. Ethernet Collision Timing Diagram

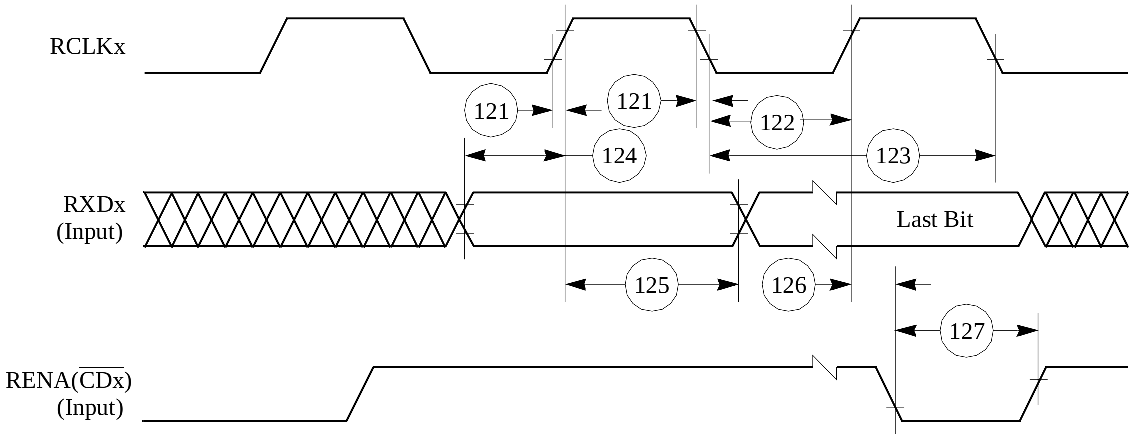
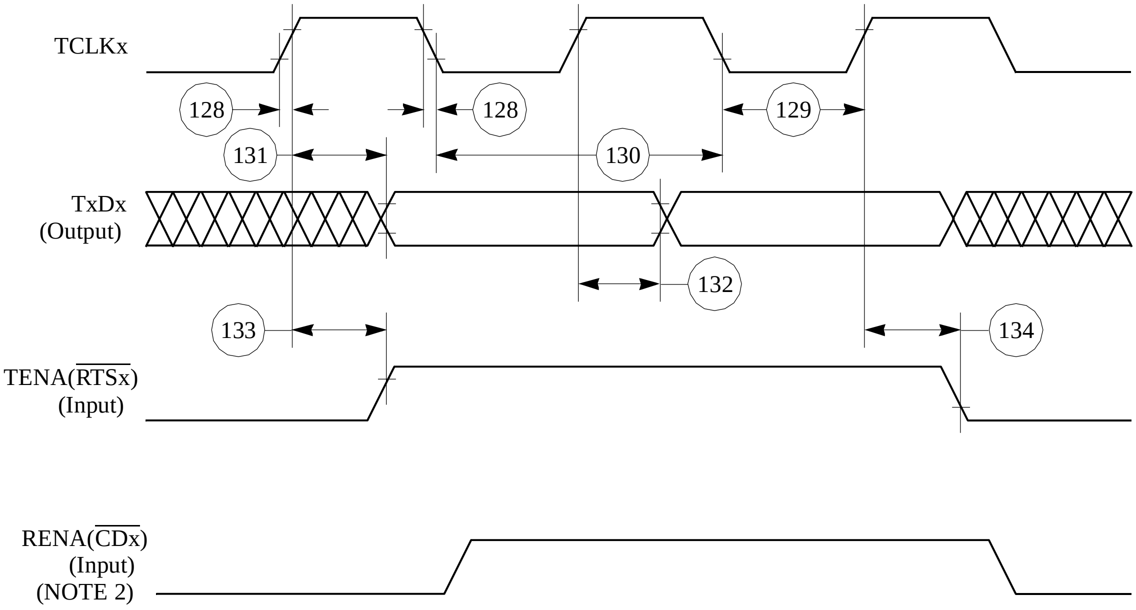


Figure 54. Ethernet Receive Timing Diagram



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 55. Ethernet Transmit Timing Diagram

## 8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

Table 21. Serial Management Controller Timing

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 150 | SMCLKx clock period [1] | 100.00 | — | ns |
| 151 | SMCLKx width low | 50.00 | — | ns |
| 151a | SMCLKx width high | 50.00 | — | ns |
| 152 | SMCLKx rise/fall time | — | 15.00 | ns |
| 153 | SMTXDx active delay (from SMCLKx falling edge) | 10.00 | 50.00 | ns |
| 154 | SMRXDx/$\overline{\text{SMSYNx}}$ setup time | 20.00 | — | ns |
| 155 | SMRXDx/$\overline{\text{SMSYNx}}$ hold time | 5.00 | — | ns |

[1] The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.

## 8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

Table 23. SPI Slave Timing

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15.00 | — | ns |
| 172 | Slave enable lag time | 15.00 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20.00 | — | ns |
| 176 | Slave data hold time (inputs) | 20.00 | — | ns |
| 177 | Slave access time | — | 50.00 | ns |
| 178 | Slave SPI MISO disable time | — | 50.00 | ns |
| 179 | Slave data valid (after SPICLK edge) | — | 50.00 | ns |
| 180 | Slave data hold time (outputs) | 0.00 | — | ns |
| 181 | Rise time (input) | — | 15.00 | ns |
| 182 | Fall time (input) | — | 15.00 | ns |

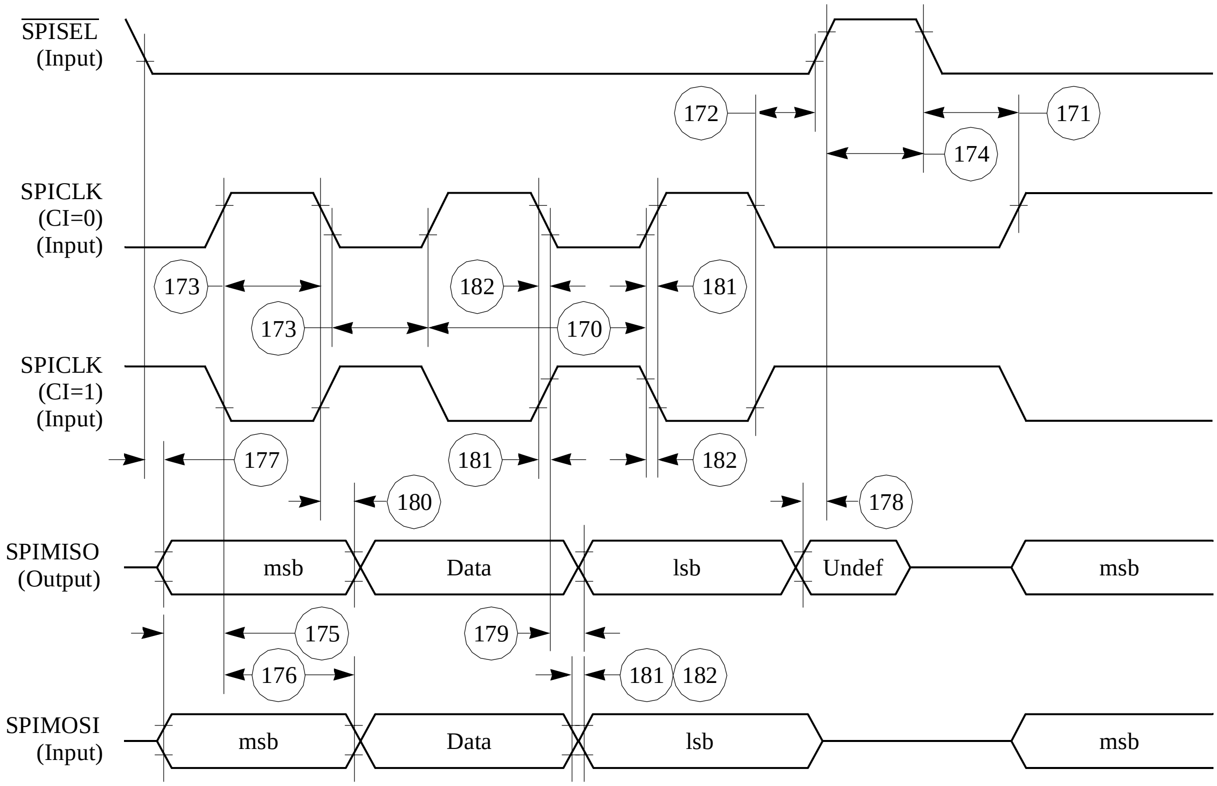


**Figure 59. SPI Slave (CP = 0) Timing Diagram**

# 9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

**Table 26. MPC850 Family Derivatives**

| Device | Ethernet Support | Number of SCCs [1] | 32-Channel HDLC Support | 64-Channel HDLC Support [2] |
|---|---|---|---|---|
| MPC850 | N/A | One | N/A | N/A |
| MPC850DE | Yes | Two | N/A | N/A |
| MPC850SR | Yes | Two | N/A | Yes |
| MPC850DSL | Yes | Two | No | No |

[1] Serial Communication Controller (SCC)

[2] 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

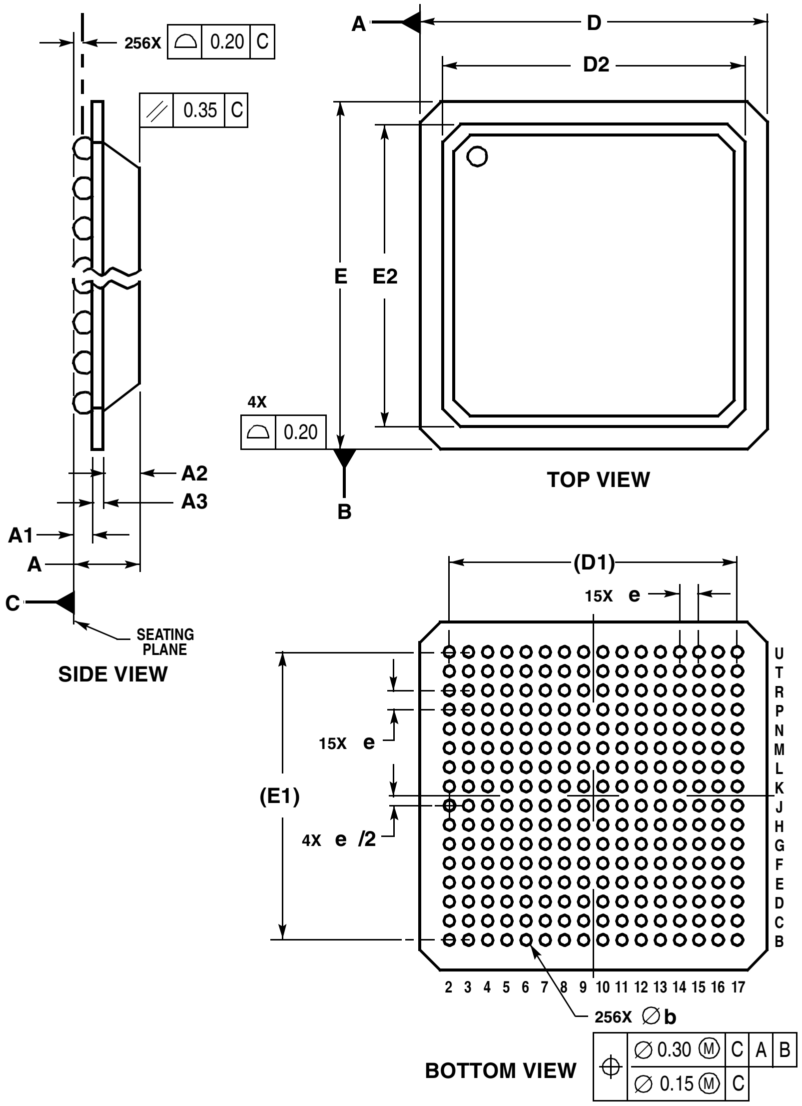
**Table 27. MPC850 Package/Frequency/Availability**

| Package Type | Frequency (MHz) | Temperature (Tj) | Order Number |
|---|---|---|---|
| 256-Lead Plastic Ball Grid Array (ZT suffix) | 50 | 0°C to 95°C | XPC850ZT50BU<br>XPC850DEZT50BU<br>XPC850SRZT50BU<br>XPC850DSLZT50BU |
| | 66 | 0°C to 95°C | XPC850ZT66BU<br>XPC850DEZT66BU<br>XPC850SRZT66BU |
| | 80 | 0°C to 95°C | XPC850ZT80BU<br>XPC850DEZT80BU<br>XPC850SRZT80BU |
| 256-Lead Plastic Ball Grid Array (CZT suffix) | 50 | -40°C to 95°C | XPC850CZT50BU<br>XPC850DECZT50BU<br>XPC850SRCZT50BU<br>XPC850DSLCZT50BU |
| | 66 | | XPC850CZT66BU<br>XPC850DECZT66BU<br>XPC850SRCZT66BU |
| | 80 | | XPC850CZT80B<br>XPC850DECZT80B<br>XPC850SRCZT80B |

## 9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

Figure 65 shows the JEDEC package dimensions of the PBGA.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND THE SEATING PLANE ARE

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.91 | 2.35 |
| A1 | 0.50 | 0.70 |
| A2 | 1.12 | 1.22 |
| A3 | 0.29 | 0.43 |
| b | 0.60 | 0.90 |
| D | 23.00 BSC | |
| D1 | 19.05 REF | |
| D2 | 19.00 | 20.00 |
| E | 23.00 BSC | |
| E1 | 19.05 REF | |
| E2 | 19.00 | 20.00 |
| e | 1.27 BSC | |

CASE 1130-01
ISSUE B

Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard

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