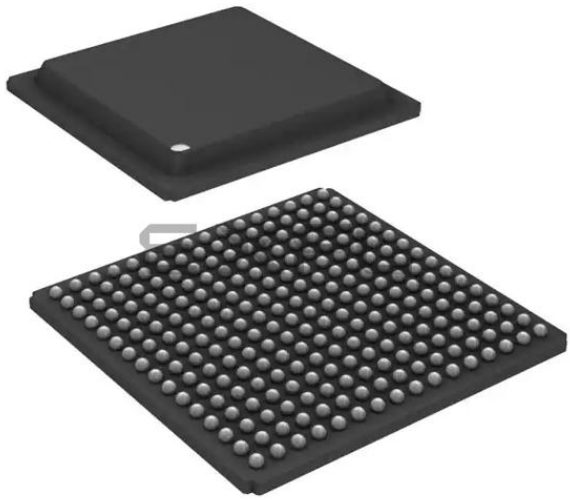

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 66MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 256-BBGA |
| Supplier Device Package | 256-PBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850cvr66bu |

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One $I^2C$ port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

**Table 1. MPC850 Functionality Matrix**

| Part | Number of SCCs Supported | Ethernet Support | ATM Support | USB Support | Multi-channel HDLC Support | Number of PCMCIA Slots Supported |
|---|---|---|---|---|---|---|
| MPC850 | 1 | Yes | - | Yes | - | 1 |
| MPC850DE | 2 | Yes | - | Yes | - | 1 |
| MPC850SR | 2 | Yes | Yes | Yes | Yes | 1 |
| MPC850DSL | 2 | Yes | Yes | Yes | No | 1 |

Additional documentation may be provided for parts listed in Table 1.

  - 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
    - Caches are two-way, set-associative
    - Physically addressed
    - Cache blocks can be updated with a 4-word line burst
    - Least-recently used (LRU) replacement algorithm
    - Lockable one-line granularity
  - Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
  - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
  - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
  - Hardware bus monitor
  - Spurious interrupt monitor
  - Software watchdog
  - Periodic interrupt timer
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
  - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
  - Memory controller programmable to support most size and speed memory interfaces
  - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
  - Variable block sizes, 32 Kbytes to 256 Mbytes
  - Selectable write protection
  - On-chip bus arbiter supports one external bus master
  - Special features for burst mode support
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers

  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

$\theta_{JA}$ = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts—chip internal power

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between $P_D$ and $T_J$ is:

$P_D = K \div (T_J + 273°C)$(2)

Solving equations (1) and (2) for K gives:

$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$(3)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 5.1 Layout Practices

Each $V_{CC}$ pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{CC}$ power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$ and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

# 6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B33a | CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM | 5.00 | 12.00 | 8.00 | 14.00 | 6.00 | 13.00 | 0.250 | 50.00 | ns |
| B34 | A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B34a | A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B34b | A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B35 | A[6–31] to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B35a | A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by BST1 in the corresponding word in the UPM | 8.00 | — | 13.00 | — | 11.00 | — | 0.500 | 50.00 | ns |
| B35b | A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM | 13.00 | — | 21.00 | — | 17.00 | — | 0.750 | 50.00 | ns |
| B36 | A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM | 3.00 | — | 6.00 | — | 4.00 | — | 0.250 | 50.00 | ns |
| B37 | UPWAIT valid to CLKOUT falling edge [10] | 6.00 | — | 6.00 | — | 6.00 | — | — | 50.00 | ns |
| B38 | CLKOUT falling edge to UPWAIT valid [10] | 1.00 | — | 1.00 | — | 1.00 | — | — | 50.00 | ns |
| B39 | $\overline{AS}$ valid to CLKOUT rising edge [11] | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B40 | A[6–31], TSIZ[0–1], RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge. | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |
| B41 | $\overline{TS}$ valid to CLKOUT rising edge (setup time) | 7.00 | — | 7.00 | — | 7.00 | — | — | 50.00 | ns |

Figure 6 provides the timing for the synchronous input signals.

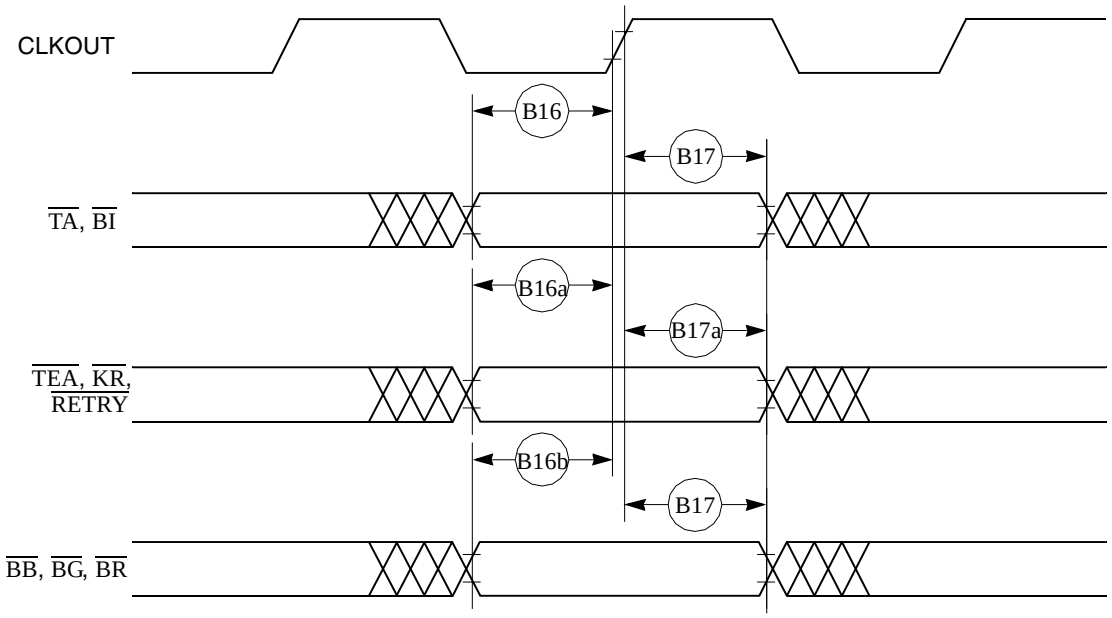



**Figure 6. Synchronous Input Signals Timing**

Figure 7 provides normal case timing for input data.

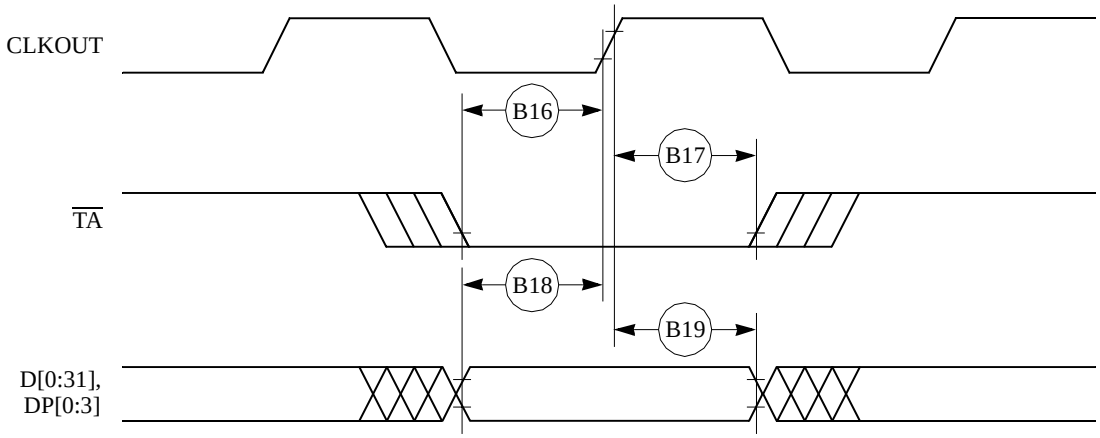



**Figure 7. Input Data Timing in Normal Case**

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

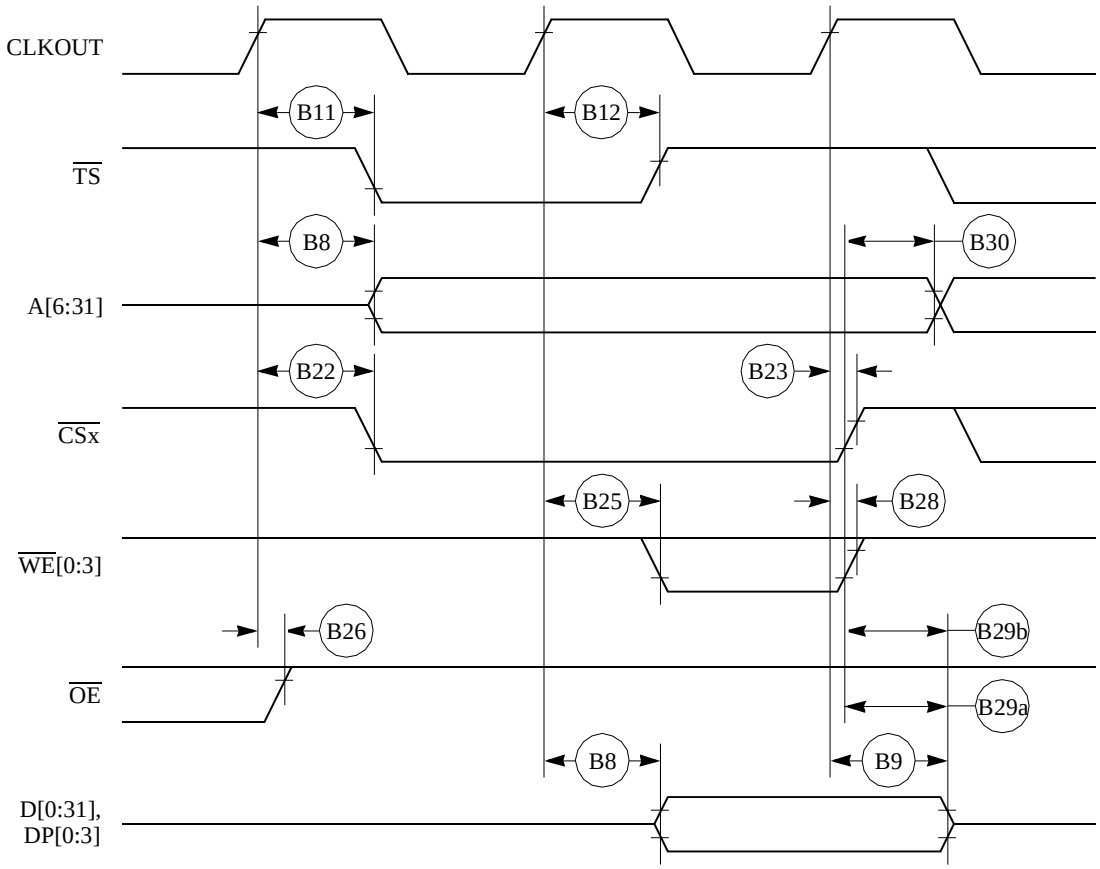



**Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)**

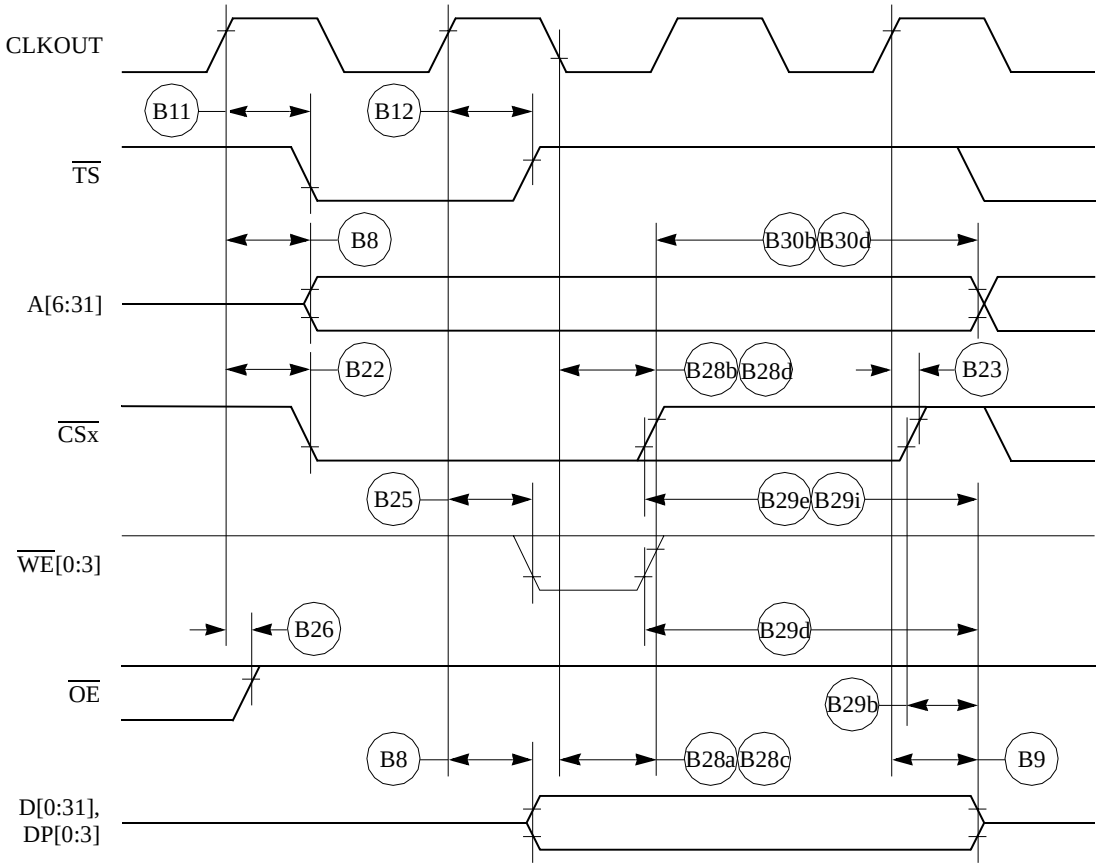



**Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)**

Figure 16 provides the timing for the external bus controlled by the UPM.

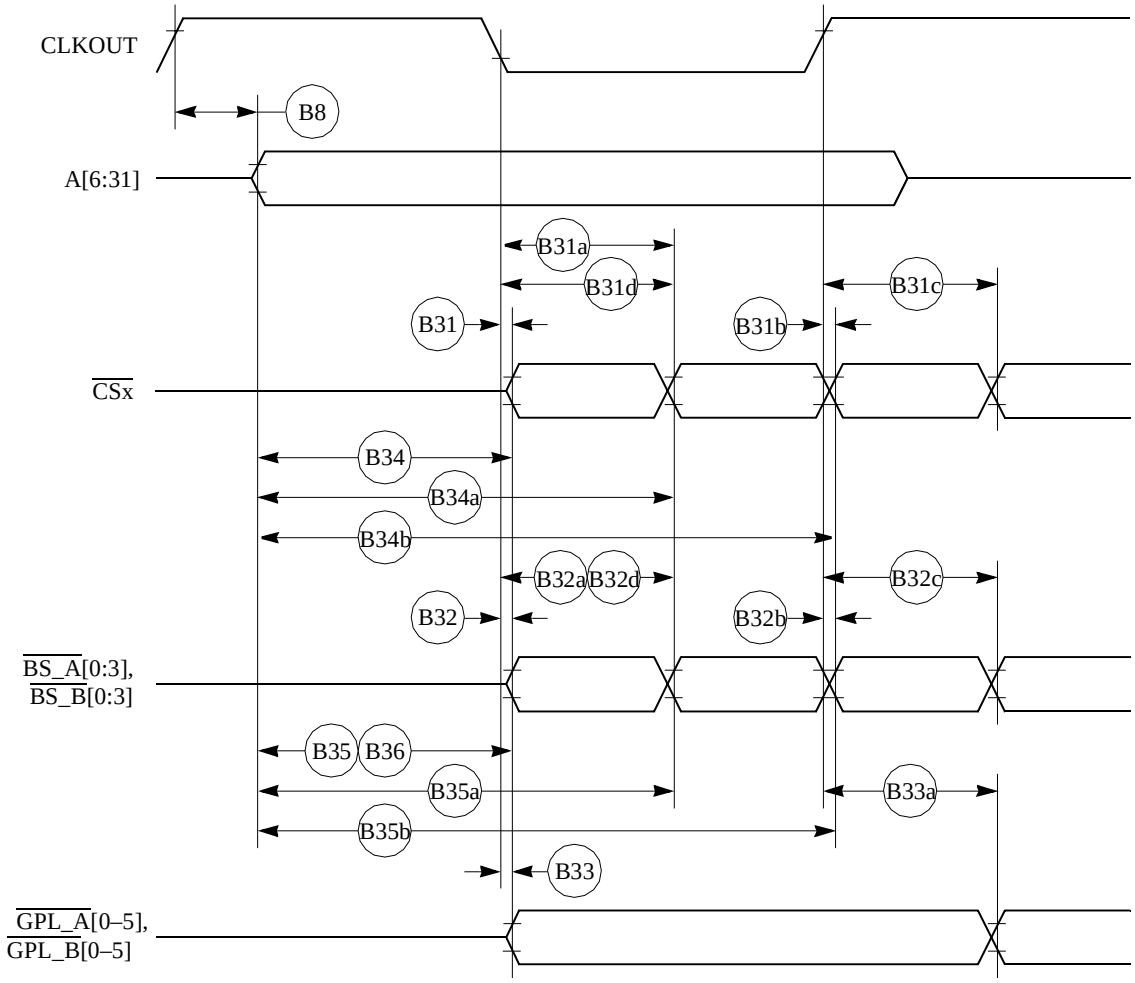



**Figure 16. External Bus Timing (UPM Controlled Signals)**

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

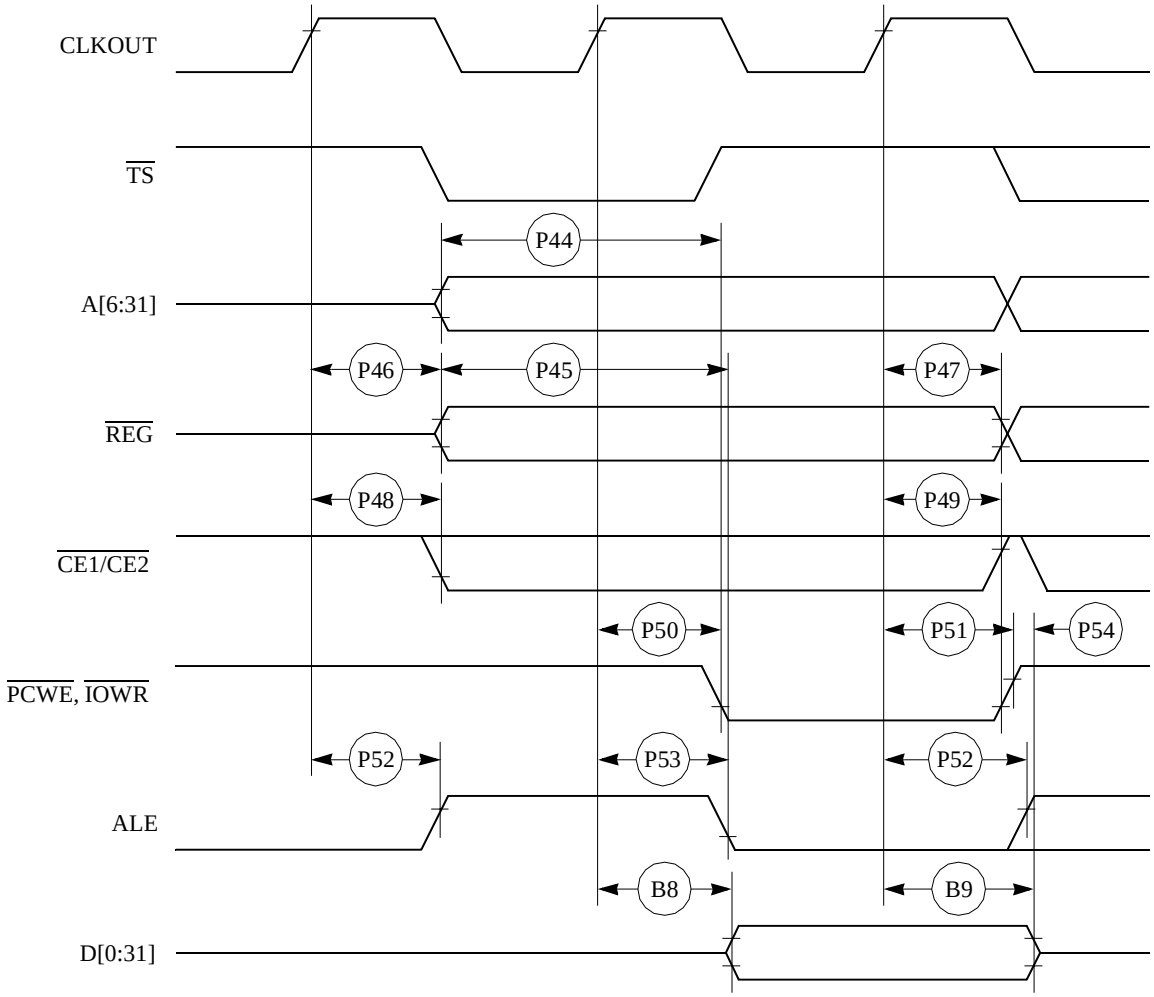



**Figure 25. PCMCIA Access Cycles Timing External Bus Write**

Figure 26 provides the PCMCIA WAIT signals detection timing.

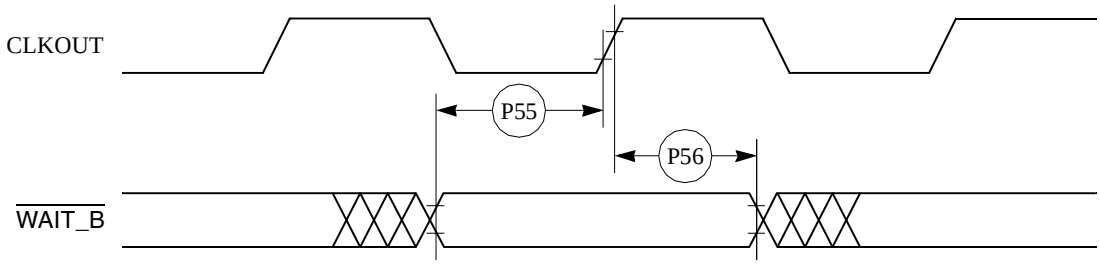



**Figure 26. PCMCIA WAIT Signal Detection Timing**

Figure 31 shows the reset timing for the data bus configuration.

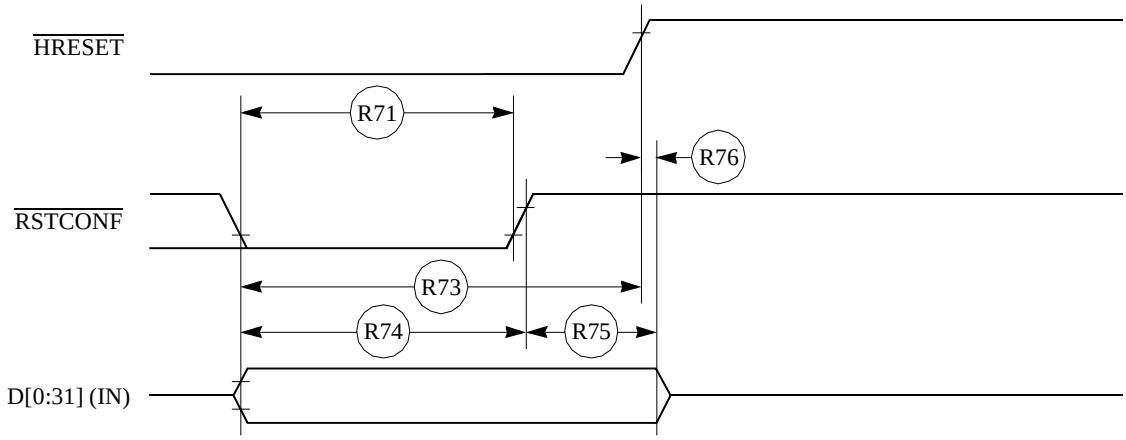



**Figure 31. Reset Timing—Configuration from Data Bus**

Figure 32 provides the reset timing for the data bus weak drive during configuration.

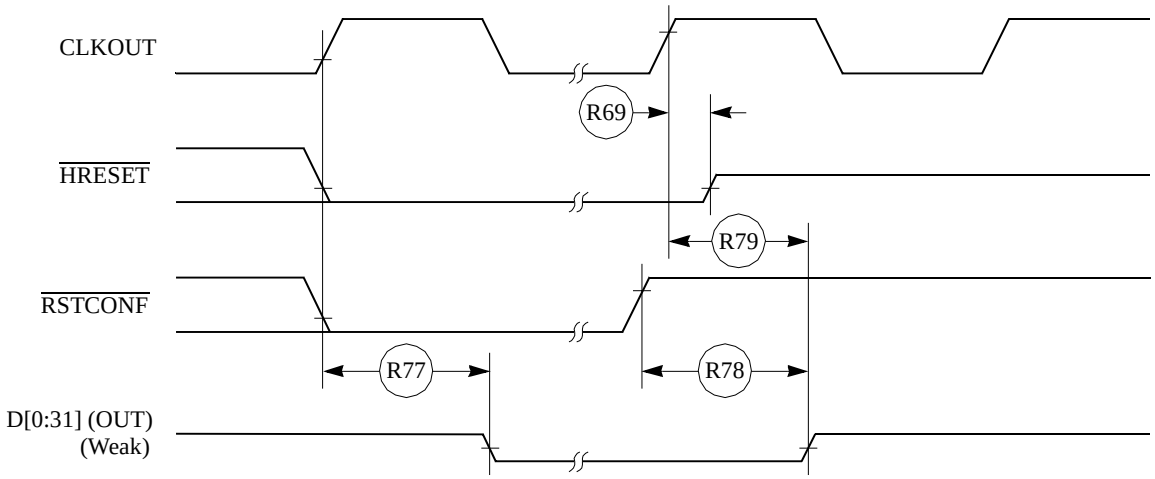



**Figure 32. Reset Timing—Data Bus Weak Drive during Configuration**

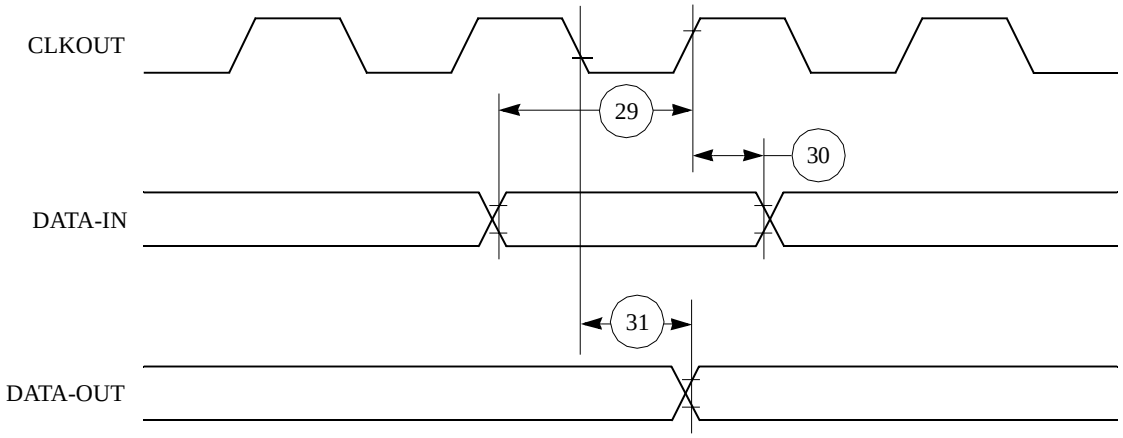



**Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram**

## 8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

**Table 14. IDMA Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7.00 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high | 3.00 | — | ns |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12.00 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12.00 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20.00 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15.00 | ns |
| 46 | $\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7.00 | — | ns |

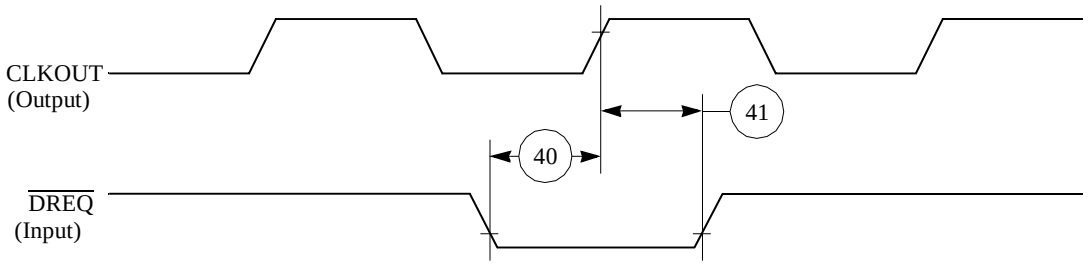



**Figure 39. IDMA External Requests Timing Diagram**

## 8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

**Table 18. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table) | 1/SYNCCLK | — | ns |
| 101 | RCLKx and TCLKx width low | 1/SYNCCLK +5 | — | ns |
| 102 | RCLKx and TCLKx rise/fall time | — | 15.00 | ns |
| 103 | TXDx active delay (from TCLKx falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTSx}}$ setup time to TCLKx rising edge | 5.00 | — | ns |
| 106 | RXDx setup time to RCLKx rising edge | 5.00 | — | ns |
| 107 | RXDx hold time from RCLKx rising edge [2] | 5.00 | — | ns |
| 108 | $\overline{\text{CDx}}$ setup time to RCLKx rising edge | 5.00 | — | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

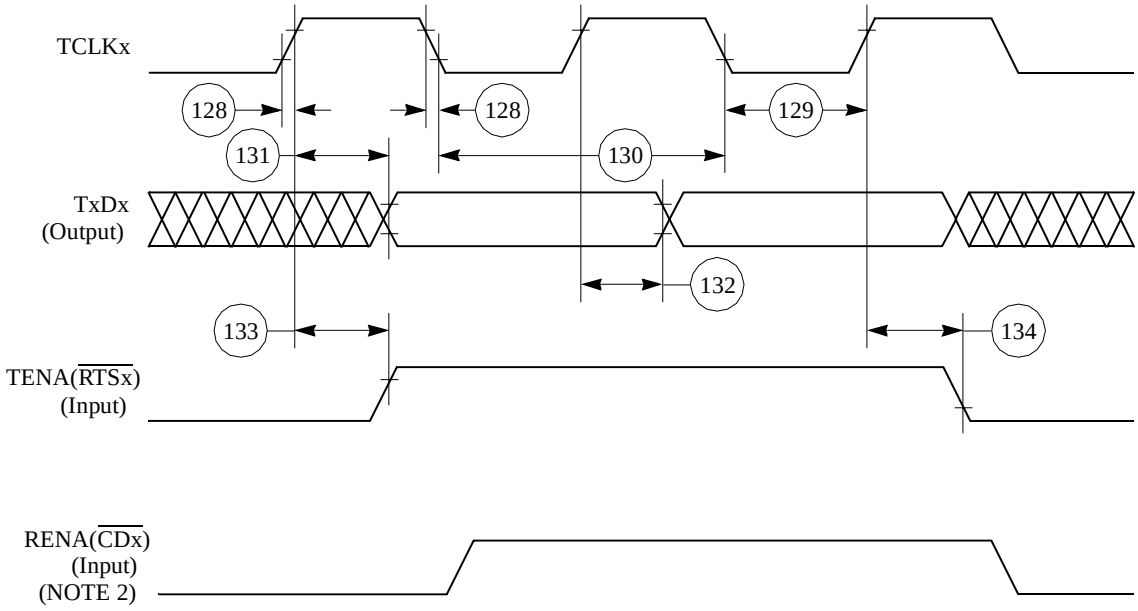
Table 19 provides the NMSI internal clock timing.

**Table 19. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table) | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLKx and TCLKx rise/fall time | — | — | ns |
| 103 | TXDx active delay (from TCLKx falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTSx}}$ setup time to TCLKx rising edge | 40.00 | — | ns |
| 106 | RXDx setup time to RCLKx rising edge | 40.00 | — | ns |
| 107 | RXDx hold time from RCLKx rising edge [2] | 0.00 | — | ns |
| 108 | $\overline{\text{CDx}}$ setup time to RCLKx rising edge | 40.00 | — | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.




NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

**Figure 55. Ethernet Transmit Timing Diagram**

## 8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

**Table 21. Serial Management Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 150 | SMCLKx clock period [1] | 100.00 | — | ns |
| 151 | SMCLKx width low | 50.00 | — | ns |
| 151a | SMCLKx width high | 50.00 | — | ns |
| 152 | SMCLKx rise/fall time | — | 15.00 | ns |
| 153 | SMTXDx active delay (from SMCLKx falling edge) | 10.00 | 50.00 | ns |
| 154 | SMRXDx/SMSYNx setup time | 20.00 | — | ns |
| 155 | SMRXDx/SMSYNx hold time | 5.00 | — | ns |

[1] The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.

## 8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

**Table 23. SPI Slave Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15.00 | — | ns |
| 172 | Slave enable lag time | 15.00 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20.00 | — | ns |
| 176 | Slave data hold time (inputs) | 20.00 | — | ns |
| 177 | Slave access time | — | 50.00 | ns |
| 178 | Slave SPI MISO disable time | — | 50.00 | ns |
| 179 | Slave data valid (after SPICLK edge) | — | 50.00 | ns |
| 180 | Slave data hold time (outputs) | 0.00 | — | ns |
| 181 | Rise time (input) | — | 15.00 | ns |
| 182 | Fall time (input) | — | 15.00 | ns |

**Table 24. I²C Timing (SCL < 100 KHz) (CONTINUED)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 210 | SDL/SCL fall time | — | 300.00 | ns |
| 211 | Stop condition setup time | 4.70 | — | µs |

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I²C (SCL > 100 KHz) timings.

**Table 25. I²C Timing (SCL > 100 KHz)**

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master) [1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | | 1/(2.2 * fSCL) | — | s |
| 203 | Low period of SCL | | 1/(2.2 * fSCL) | — | s |
| 204 | High period of SCL | | 1/(2.2 * fSCL) | — | s |
| 205 | Start condition setup time | | 1/(2.2 * fSCL) | — | s |
| 206 | Start condition hold time | | 1/(2.2 * fSCL) | — | s |
| 207 | Data hold time | | 0 | — | s |
| 208 | Data setup time | | 1/(40 * fSCL) | — | s |
| 209 | SDL/SCL rise time | | — | 1/(10 * fSCL) | s |
| 210 | SDL/SCL fall time | | — | 1/(33 * fSCL) | s |
| 211 | Stop condition setup time | | 1/2(2.2 * fSCL) | — | s |

1 SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 61 shows the I²C bus timing.

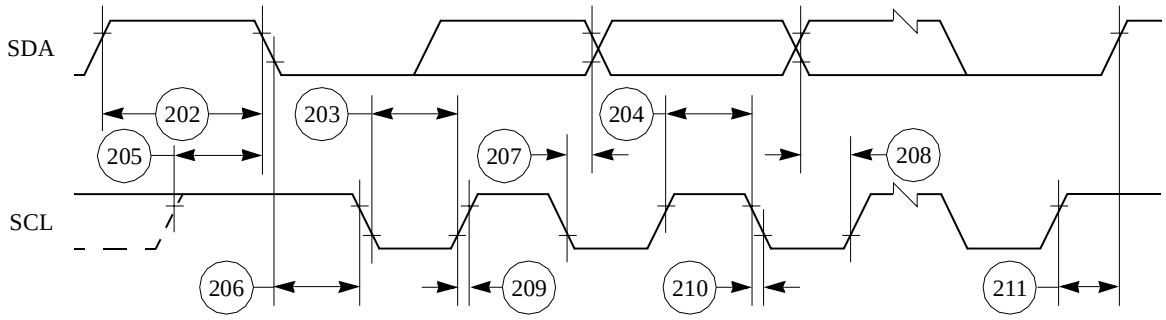



**Figure 61. I²C Bus Timing Diagram**

# 9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

**Table 26. MPC850 Family Derivatives**

| Device | Ethernet Support | Number of SCCs [1] | 32-Channel HDLC Support | 64-Channel HDLC Support [2] |
|---|---|---|---|---|
| MPC850 | N/A | One | N/A | N/A |
| MPC850DE | Yes | Two | N/A | N/A |
| MPC850SR | Yes | Two | N/A | Yes |
| MPC850DSL | Yes | Two | No | No |

1 Serial Communication Controller (SCC)

2 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

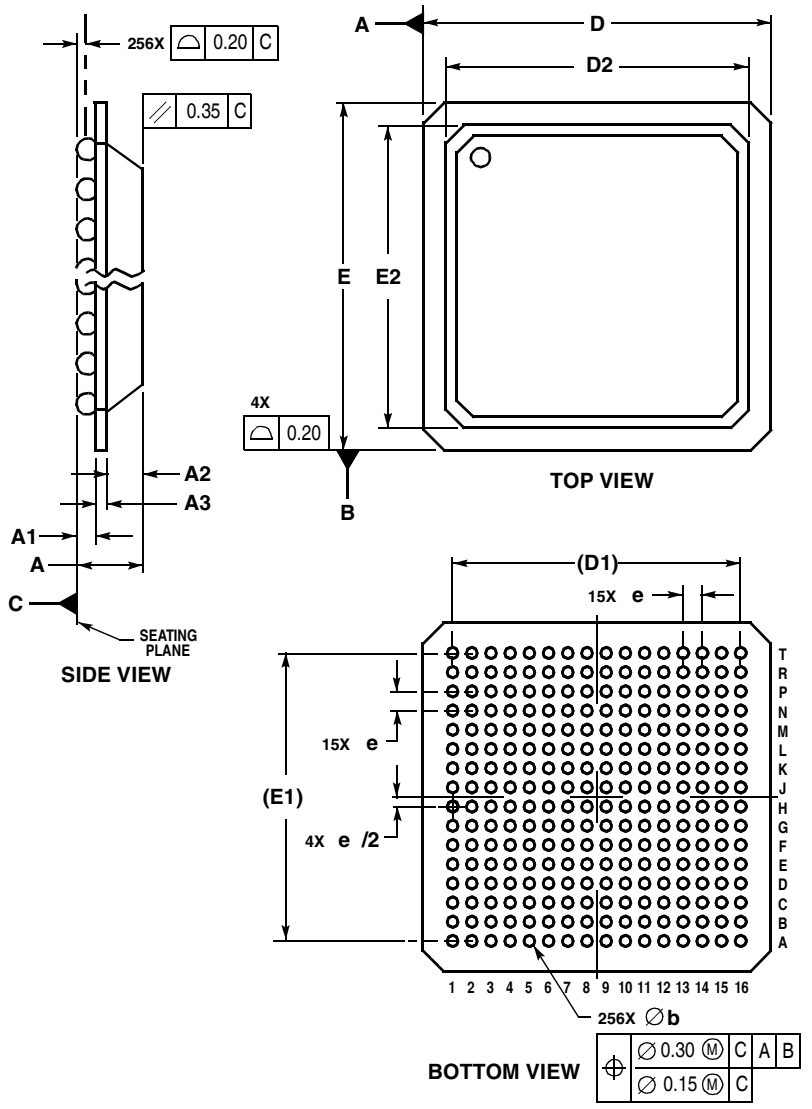
**Table 27. MPC850 Package/Frequency/Availability**

| Package Type | Frequency (MHz) | Temperature (Tj) | Order Number |
|---|---|---|---|
| 256-Lead Plastic Ball Grid Array (ZT suffix) | 50 | 0°C to 95°C | XPC850ZT50BU<br>XPC850DEZT50BU<br>XPC850SRZT50BU<br>XPC850DSLZT50BU |
| | 66 | 0°C to 95°C | XPC850ZT66BU<br>XPC850DEZT66BU<br>XPC850SRZT66BU |
| | 80 | 0°C to 95°C | XPC850ZT80BU<br>XPC850DEZT80BU<br>XPC850SRZT80BU |
| 256-Lead Plastic Ball Grid Array (CZT suffix) | 50 | -40°C to 95°C | XPC850CZT50BU<br>XPC850DECZT50BU<br>XPC850SRCZT50BU<br>XPC850DSLCZT50BU |
| | 66 | | XPC850CZT66BU<br>XPC850DECZT66BU<br>XPC850SRCZT66BU |
| | 80 | | XPC850CZT80B<br>XPC850DECZT80B<br>XPC850SRCZT80B |

## 9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

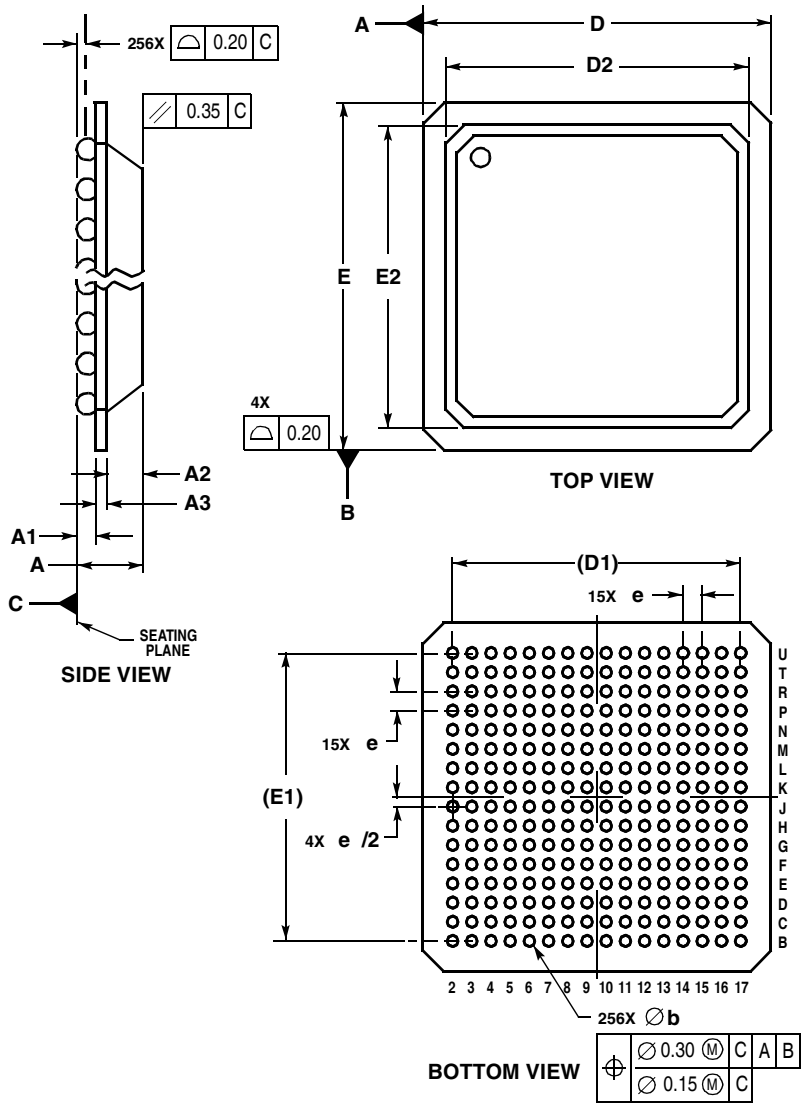



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND THE SEATING PLANE ARE

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.91 | 2.35 |
| A1 | 0.50 | 0.70 |
| A2 | 1.12 | 1.22 |
| A3 | 0.29 | 0.43 |
| b | 0.60 | 0.90 |
| D | 23.00 BSC | |
| D1 | 19.05 REF | |
| D2 | 19.00 | 20.00 |
| E | 23.00 BSC | |
| E1 | 19.05 REF | |
| E2 | 19.00 | 20.00 |
| e | 1.27 BSC | |

**Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard**

Figure 65 shows the JEDEC package dimensions of the PBGA.




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND THE SEATING PLANE ARE

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.91 | 2.35 |
| A1 | 0.50 | 0.70 |
| A2 | 1.12 | 1.22 |
| A3 | 0.29 | 0.43 |
| b | 0.60 | 0.90 |
| D | 23.00 BSC | |
| D1 | 19.05 REF | |
| D2 | 19.00 | 20.00 |
| E | 23.00 BSC | |
| E1 | 19.05 REF | |
| E2 | 19.00 | 20.00 |
| e | 1.27 BSC | |

**CASE 1130-01**
**ISSUE B**

**Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard**

# 10 Document Revision History

Table 28 lists significant changes between revisions of this document.

**Table 28. Document Revision History**

| Revision | Date | Change |
|---|---|---|
| 2 | 7/2005 | Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit. |
| 1 | 10/2002 | Added MPC850DSL. Corrected Figure 25 on page 34. |
| 0.2 | 04/2002 | Updated power numbers and added Rev. C |
| 0.1 | 11/2001 | Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table. |