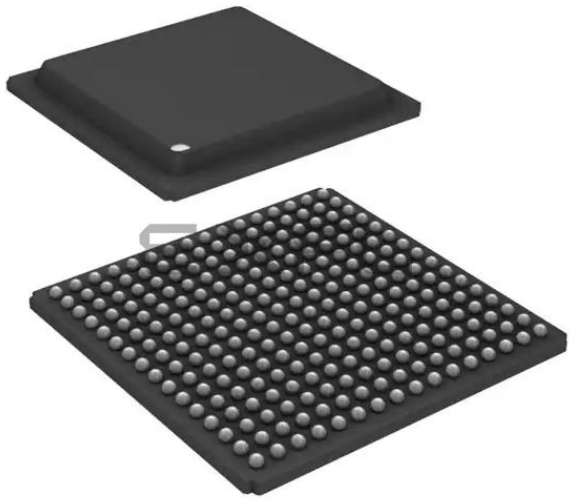

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MPC8xx |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 50MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 95°C (TA) |
| Security Features | - |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-PBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850czt50bur2 |

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One $I^2C$ port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

**Table 1. MPC850 Functionality Matrix**

| Part | Number of SCCs Supported | Ethernet Support | ATM Support | USB Support | Multi-channel HDLC Support | Number of PCMCIA Slots Supported |
|---|---|---|---|---|---|---|
| MPC850 | 1 | Yes | - | Yes | - | 1 |
| MPC850DE | 2 | Yes | - | Yes | - | 1 |
| MPC850SR | 2 | Yes | Yes | Yes | Yes | 1 |
| MPC850DSL | 2 | Yes | Yes | Yes | No | 1 |

Additional documentation may be provided for parts listed in Table 1.

# 2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:

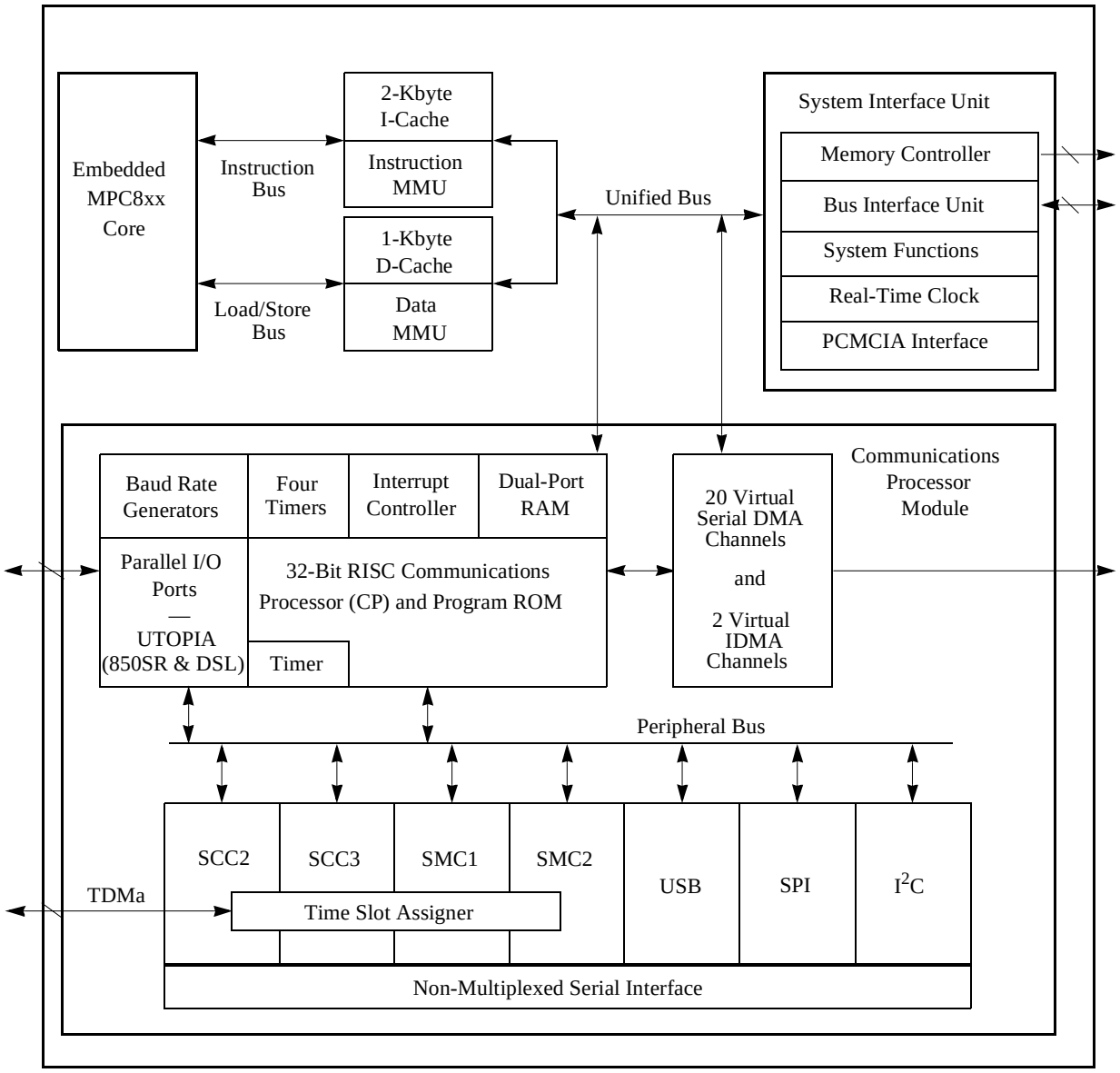



**Figure 1. MPC850 Microprocessor Block Diagram**

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

**Table 6. Bus Operation Timing [1] (continued)**

| Num | Characteristic | 50 MHz | | 66 MHz | | 80 MHz | | FFACT | Cap Load (default 50 pF) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| B42 | CLKOUT rising edge to $\overline{TS}$ valid (hold time) | 2.00 | — | 2.00 | — | 2.00 | — | — | 50.00 | ns |
| B43 | $\overline{AS}$ negation to memory controller signals negation | — | TBD | — | TBD | TBD | — | — | 50.00 | ns |

1 The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR)$$

For maxima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR) + 1ns(CAP\ LOAD - 50) / 10$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

$D_{50}$ is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

2 Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.

3 If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

4 The timing for $\overline{BR}$ output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC850 is selected to work with internal bus arbiter.

5 The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).

6 The timing required for $\overline{BR}$ input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC850 is selected to work with the external bus arbiter.

7 The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

8 The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

9 The timing B30 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE[0:3]}$ when CSNT = '0'.

10 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.

11 The $\overline{AS}$ signal is considered asynchronous to CLKOUT.

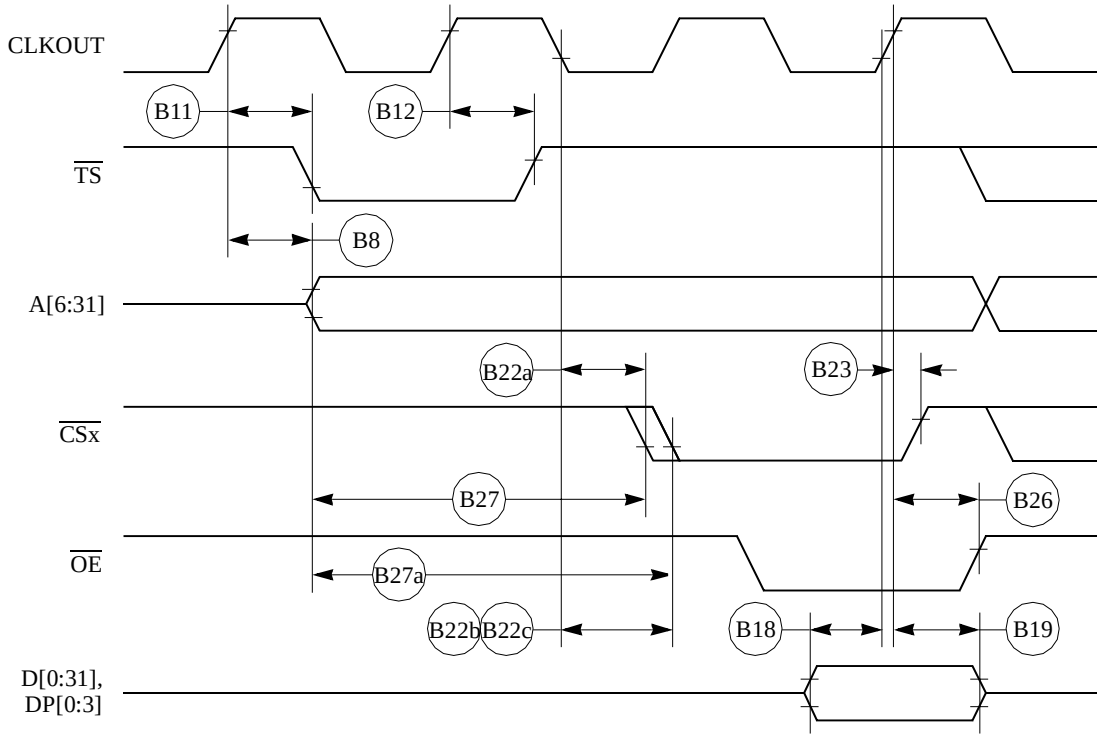



**Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)**

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

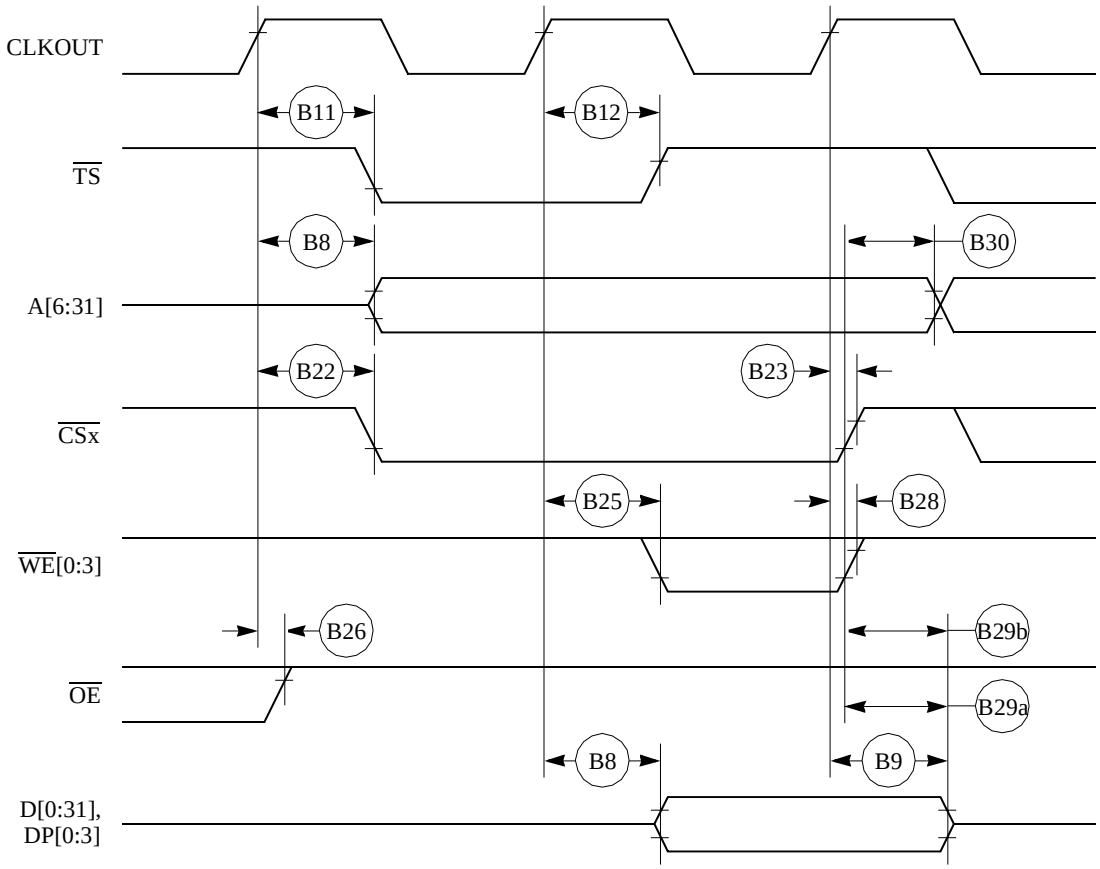



**Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)**

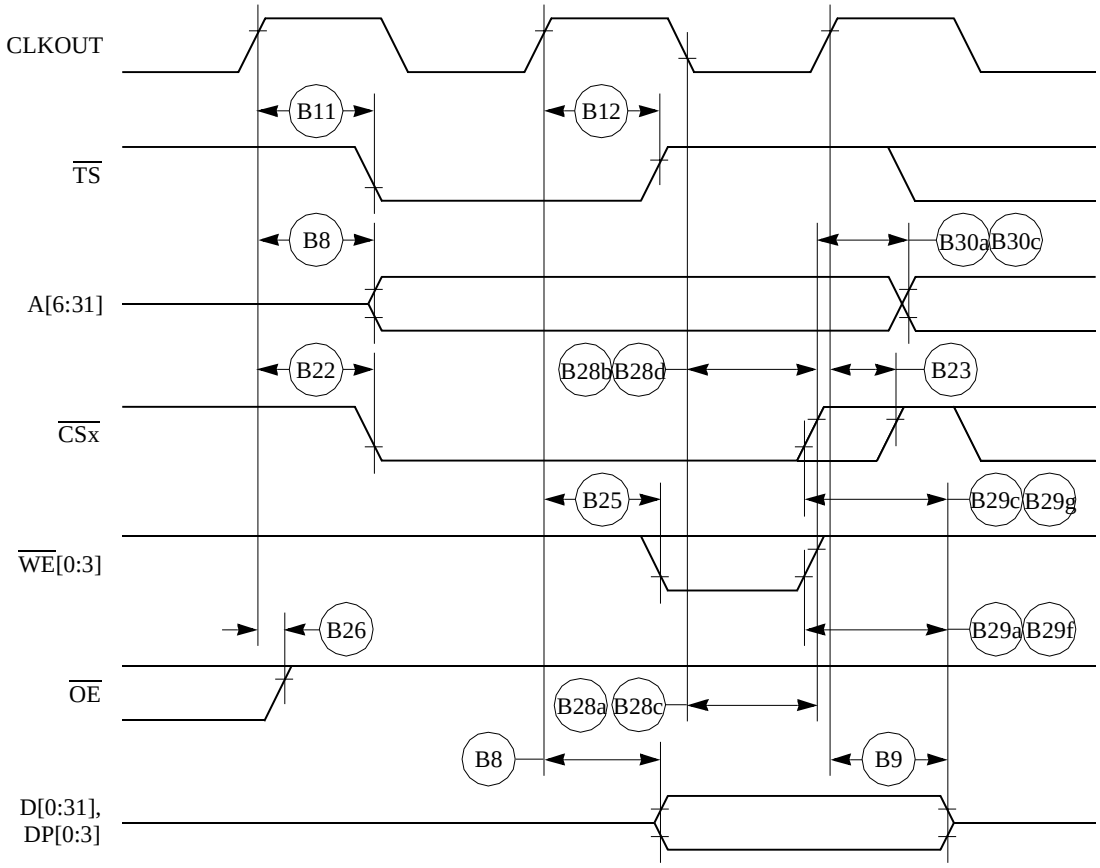



**Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)**

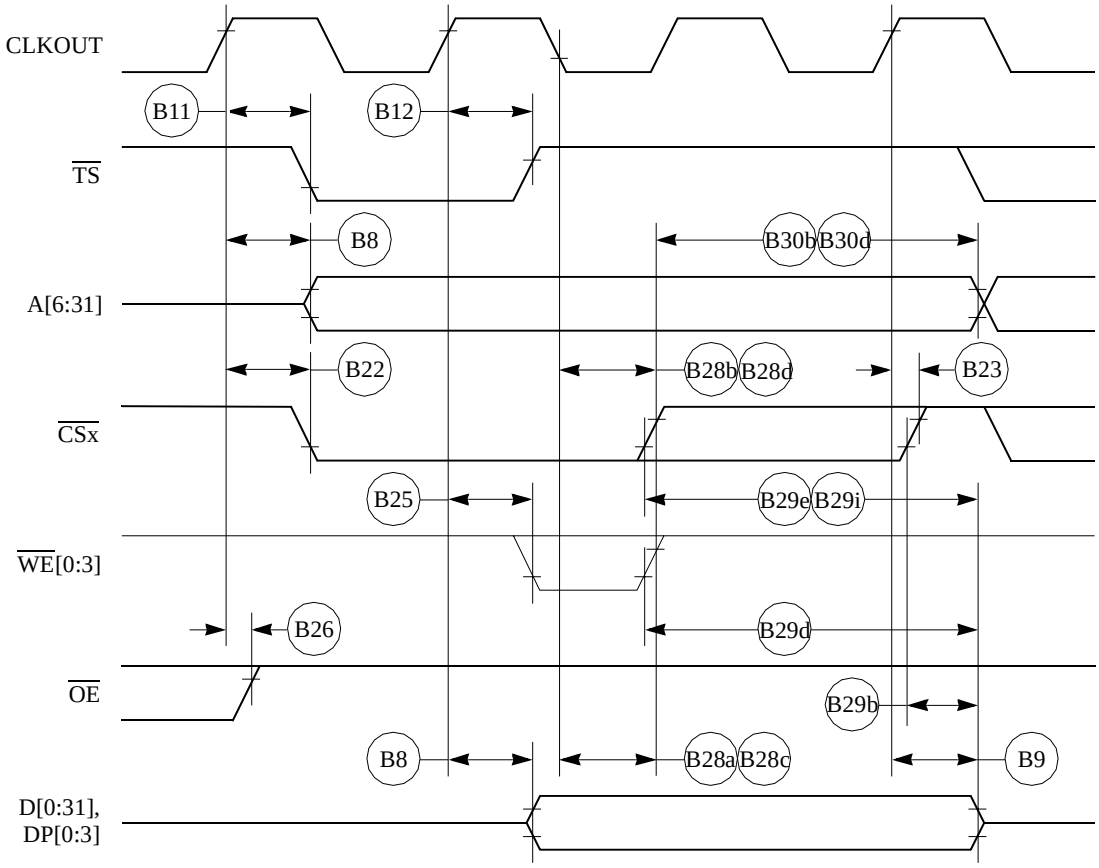



**Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)**

Table 11 shows the reset timing for the MPC850.

**Table 11. Reset Timing**

| Num | Characteristic | 50 MHz | | 66MHz | | 80 MHz | | FFACTOR | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| R69 | CLKOUT to $\overline{\text{HRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | ns |
| R70 | CLKOUT to $\overline{\text{SRESET}}$ high impedance | — | 20.00 | — | 20.00 | — | 20.00 | — | ns |
| R71 | $\overline{\text{RSTCONF}}$ pulse width | 340.00 | — | 515.00 | — | 425.00 | — | 17.000 | ns |
| R72 | | — | — | — | — | — | — | — | |
| R73 | Configuration data to $\overline{\text{HRESET}}$ rising edge set up time | 350.00 | — | 505.00 | — | 425.00 | — | 15.000 | ns |
| R74 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time | 350.00 | — | 350.00 | — | 350.00 | — | — | ns |
| R75 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R76 | Configuration data hold time after $\overline{\text{HRESET}}$ negation | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R77 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R78 | $\overline{\text{RSTCONF}}$ negated to data out high impedance. | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R79 | CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance. | — | 25.00 | — | 25.00 | — | 25.00 | — | ns |
| R80 | DSDI, DSCK set up | 60.00 | — | 90.00 | — | 75.00 | — | 3.000 | ns |
| R81 | DSDI, DSCK hold time | 0.00 | — | 0.00 | — | 0.00 | — | — | ns |
| R82 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample | 160.00 | — | 242.00 | — | 200.00 | — | 8.000 | ns |

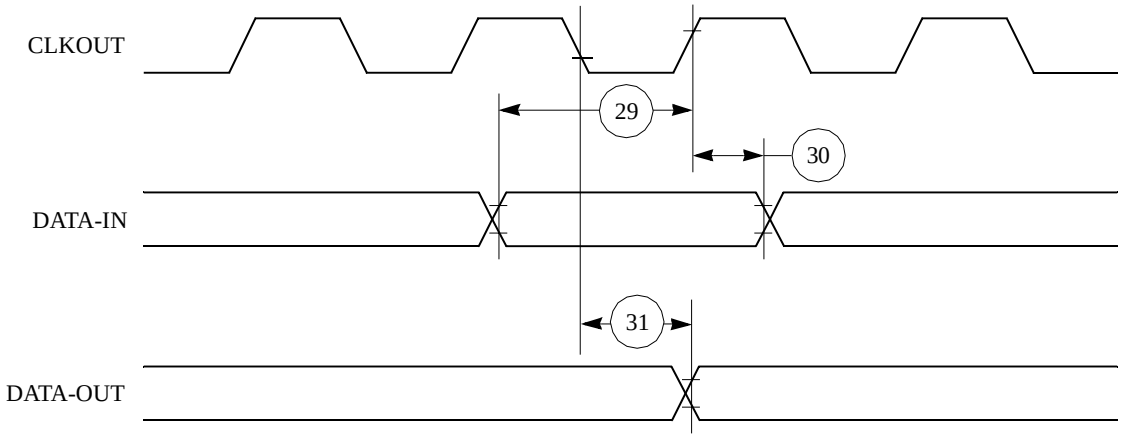



**Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram**

## 8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

**Table 14. IDMA Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7.00 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high | 3.00 | — | ns |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12.00 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12.00 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20.00 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15.00 | ns |
| 46 | $\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7.00 | — | ns |

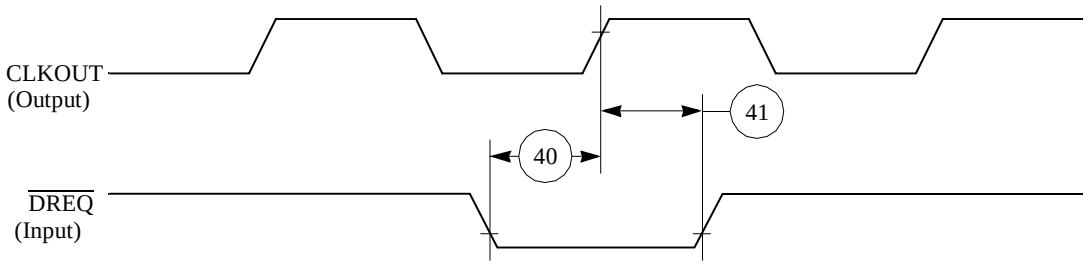



**Figure 39. IDMA External Requests Timing Diagram**

**Table 17. SI Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 82 | L1RCLK, L1TCLK frequency (DSC =1) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLK, L1TCLK width low (DSC =1) | P + 10 | — | ns |
| 83A | L1RCLK, L1TCLK width high (DSC = 1)[3] | P + 10 | — | ns |
| 84 | L1CLK edge to L1CLKO valid (DSC = 1) | — | 30.00 | ns |
| 85 | $\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4] | 1.00 | — | L1TCLK |
| 86 | L1GR setup time[2] | 42.00 | — | ns |
| 87 | L1GR hold time | 42.00 | — | ns |
| 88 | L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0) | — | 0.00 | ns |

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

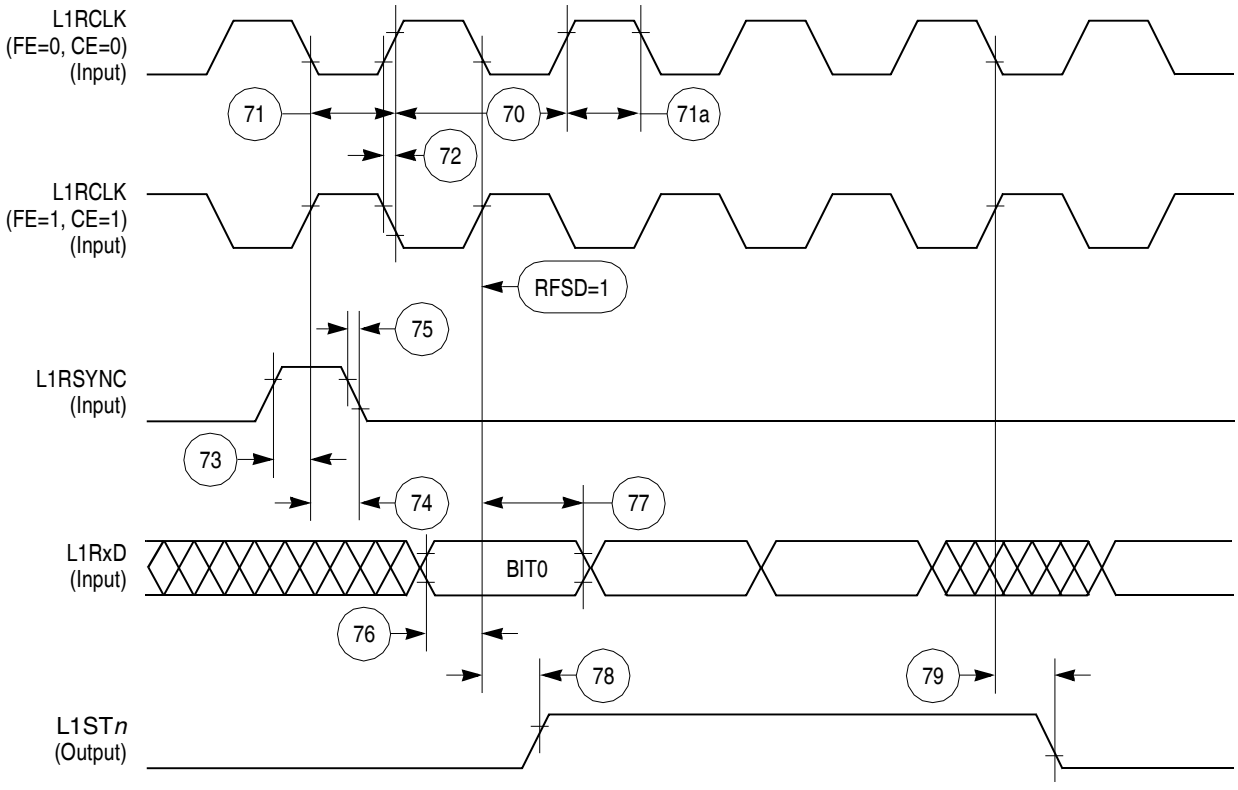



**Figure 45. SI Receive Timing Diagram with Normal Clocking (DSC = 0)**

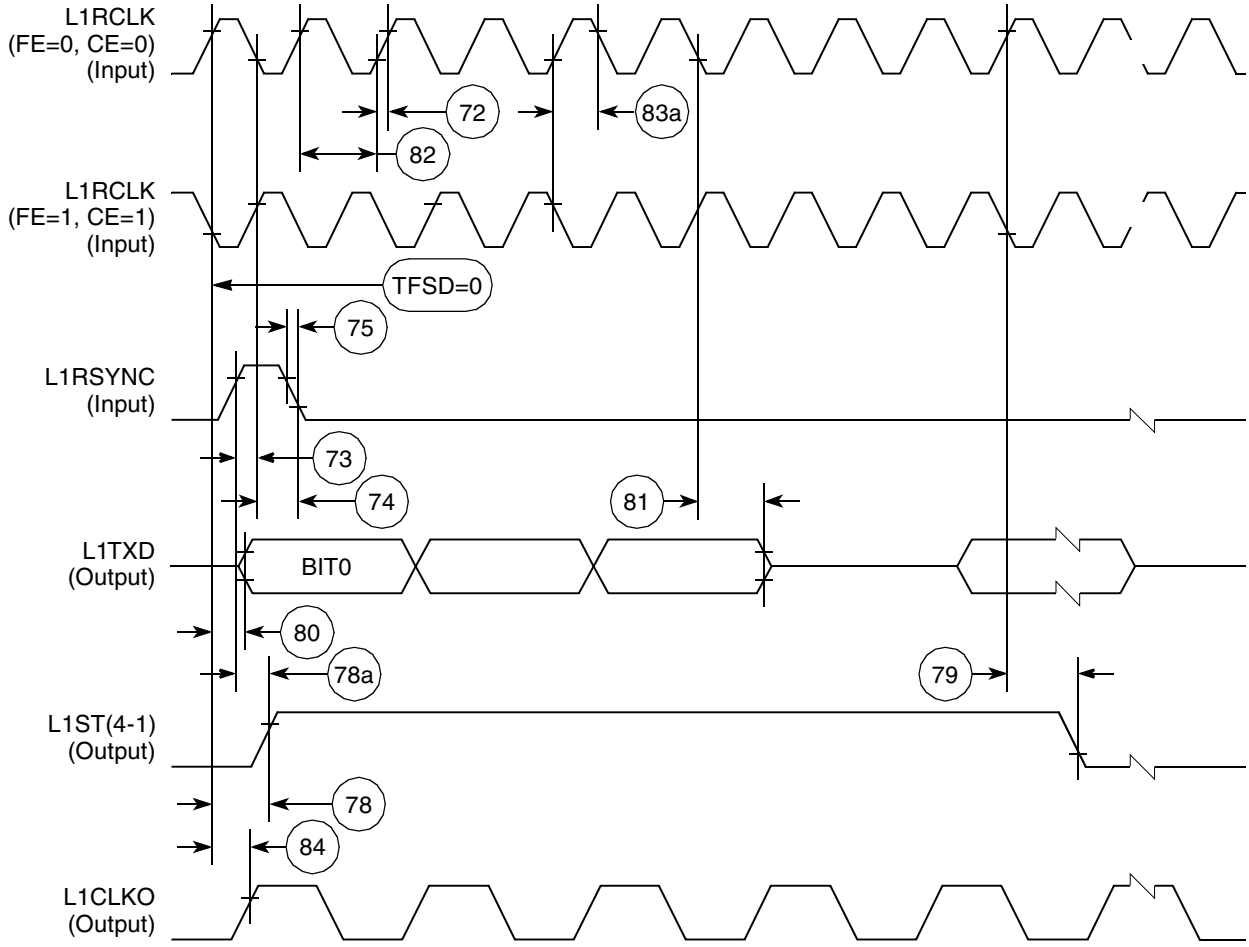



**Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)**

## 8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

**Table 18. NMSI External Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table) | 1/SYNCCLK | — | ns |
| 101 | RCLKx and TCLKx width low | 1/SYNCCLK +5 | — | ns |
| 102 | RCLKx and TCLKx rise/fall time | — | 15.00 | ns |
| 103 | TXDx active delay (from TCLKx falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTSx}}$ setup time to TCLKx rising edge | 5.00 | — | ns |
| 106 | RXDx setup time to RCLKx rising edge | 5.00 | — | ns |
| 107 | RXDx hold time from RCLKx rising edge [2] | 5.00 | — | ns |
| 108 | $\overline{\text{CDx}}$ setup time to RCLKx rising edge | 5.00 | — | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

**Table 19. NMSI Internal Clock Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table) | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLKx and TCLKx rise/fall time | — | — | ns |
| 103 | TXDx active delay (from TCLKx falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTSx}}$ setup time to TCLKx rising edge | 40.00 | — | ns |
| 106 | RXDx setup time to RCLKx rising edge | 40.00 | — | ns |
| 107 | RXDx hold time from RCLKx rising edge [2] | 0.00 | — | ns |
| 108 | $\overline{\text{CDx}}$ setup time to RCLKx rising edge | 40.00 | — | ns |

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

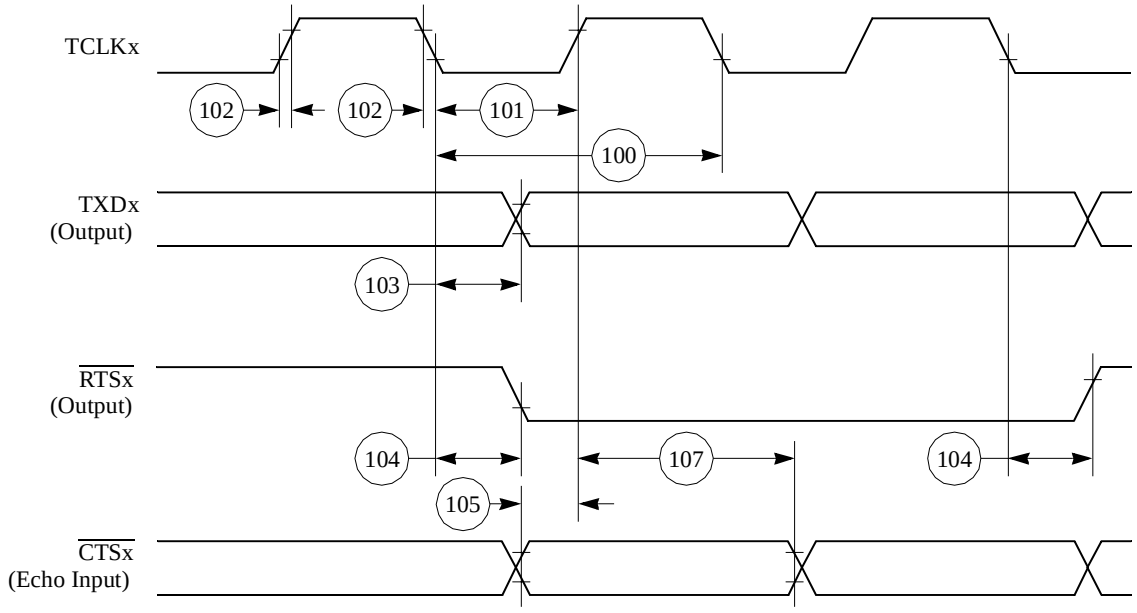



**Figure 52. HDLC Bus Timing Diagram**

## 8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

**Table 20. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40.00 | — | ns |
| 121 | RCLKx rise/fall time (x = 2, 3 for all specs in this table) | — | 15.00 | ns |
| 122 | RCLKx width low | 40.00 | — | ns |
| 123 | RCLKx clock period [1] | 80.00 | 120.00 | ns |
| 124 | RXDx setup time | 20.00 | — | ns |
| 125 | RXDx hold time | 5.00 | — | ns |
| 126 | RENA active delay (from RCLKx rising edge of the last data bit) | 10.00 | — | ns |
| 127 | RENA width low | 100.00 | — | ns |
| 128 | TCLKx rise/fall time | — | 15.00 | ns |
| 129 | TCLKx width low | 40.00 | — | ns |
| 130 | TCLKx clock period[1] | 99.00 | 101.00 | ns |
| 131 | TXDx active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 132 | TXDx inactive delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |
| 133 | TENA active delay (from TCLKx rising edge) | 10.00 | 50.00 | ns |

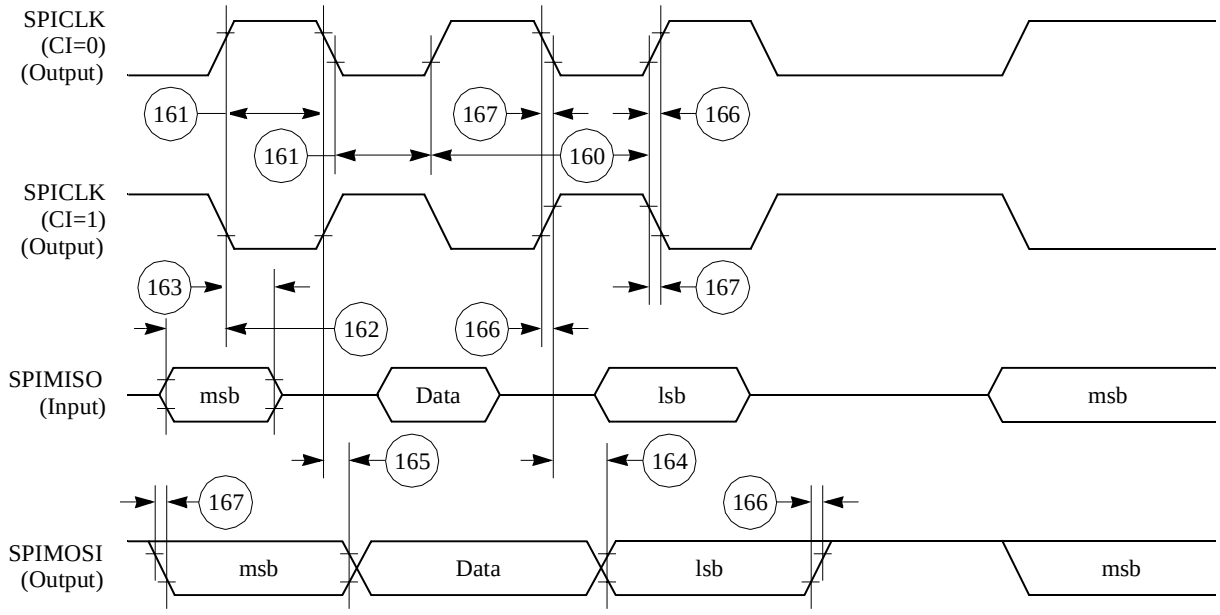



**Figure 57. SPI Master (CP = 0) Timing Diagram**

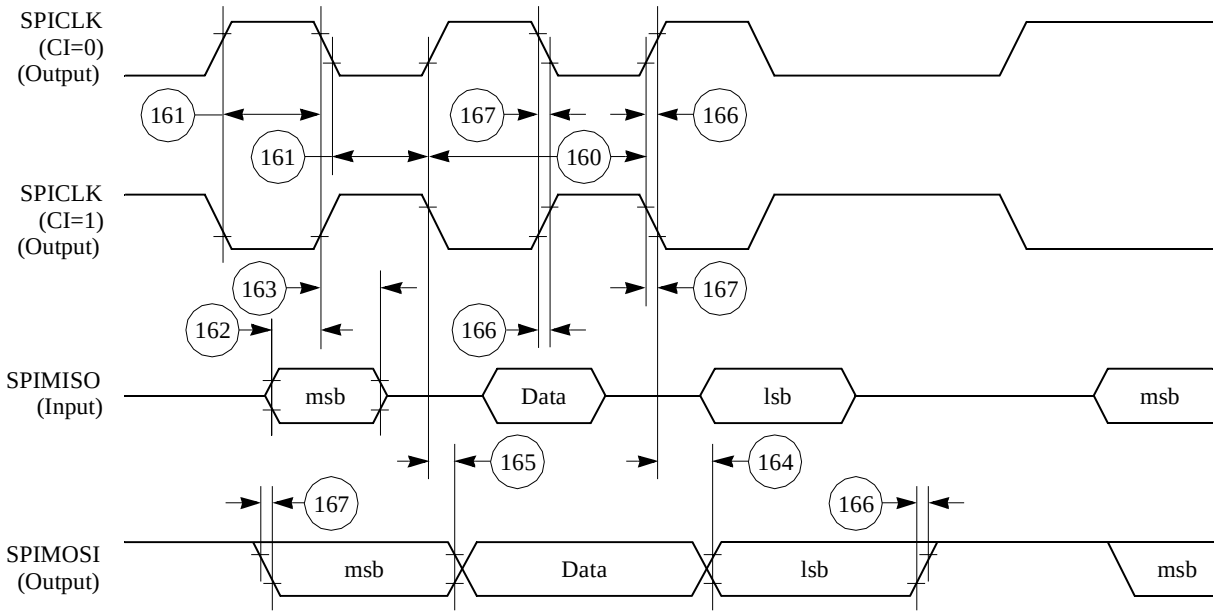



**Figure 58. SPI Master (CP = 1) Timing Diagram**

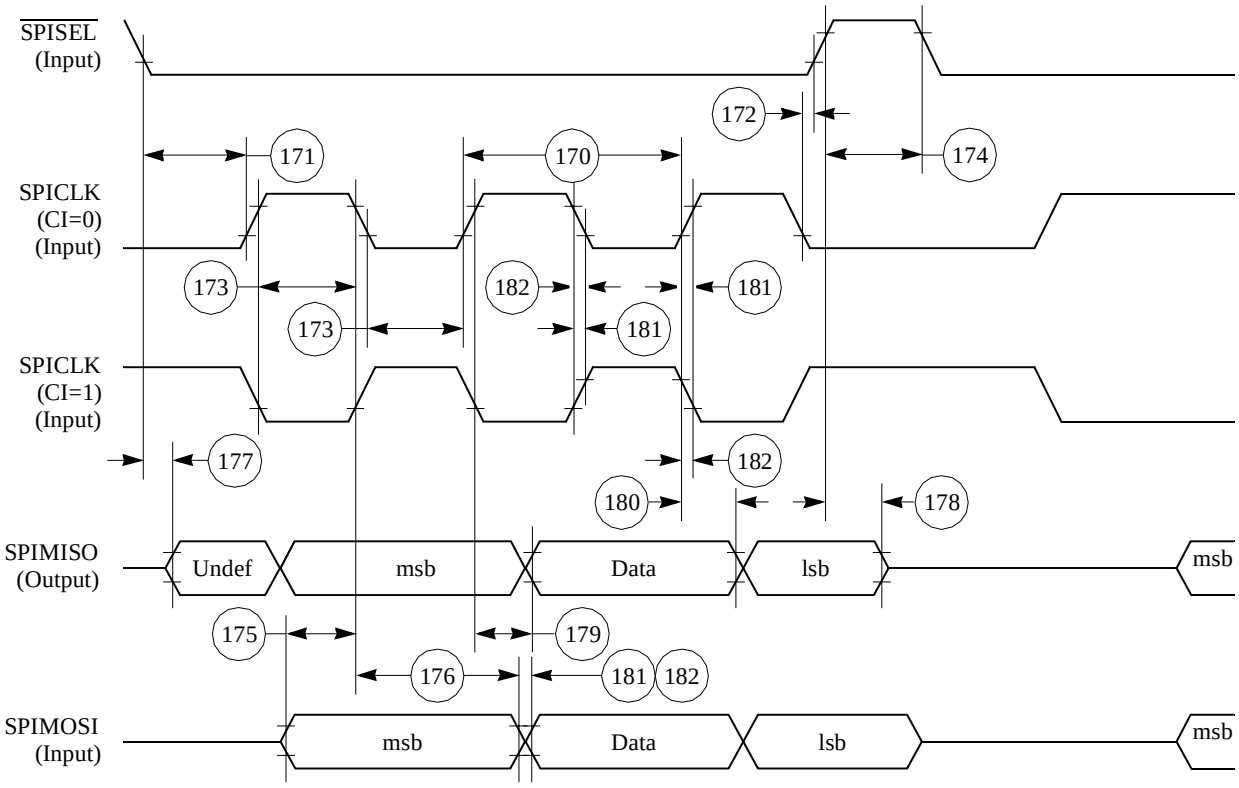



**Figure 60. SPI Slave (CP = 1) Timing Diagram**

## 8.11 I²C AC Electrical Specifications

Table 24 provides the I²C (SCL < 100 KHz) timings.

**Table 24. I²C Timing (SCL < 100 KHz)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 200 | SCL clock frequency (slave) | 0.00 | 100.00 | KHz |
| 200 | SCL clock frequency (master) [1] | 1.50 | 100.00 | KHz |
| 202 | Bus free time between transmissions | 4.70 | — | µs |
| 203 | Low period of SCL | 4.70 | — | µs |
| 204 | High period of SCL | 4.00 | — | µs |
| 205 | Start condition setup time | 4.70 | — | µs |
| 206 | Start condition hold time | 4.00 | — | µs |
| 207 | Data hold time | 0.00 | — | µs |
| 208 | Data setup time | 250.00 | — | ns |
| 209 | SDL/SCL rise time | — | 1.00 | µs |

**Table 24. I²C Timing (SCL < 100 KHz) (CONTINUED)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 210 | SDL/SCL fall time | — | 300.00 | ns |
| 211 | Stop condition setup time | 4.70 | — | µs |

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 25 provides the I²C (SCL > 100 KHz) timings.

**Table 25. I²C Timing (SCL > 100 KHz)**

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master) [1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | | 1/(2.2 * fSCL) | — | s |
| 203 | Low period of SCL | | 1/(2.2 * fSCL) | — | s |
| 204 | High period of SCL | | 1/(2.2 * fSCL) | — | s |
| 205 | Start condition setup time | | 1/(2.2 * fSCL) | — | s |
| 206 | Start condition hold time | | 1/(2.2 * fSCL) | — | s |
| 207 | Data hold time | | 0 | — | s |
| 208 | Data setup time | | 1/(40 * fSCL) | — | s |
| 209 | SDL/SCL rise time | | — | 1/(10 * fSCL) | s |
| 210 | SDL/SCL fall time | | — | 1/(33 * fSCL) | s |
| 211 | Stop condition setup time | | 1/2(2.2 * fSCL) | — | s |

1 SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2). The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 61 shows the I²C bus timing.

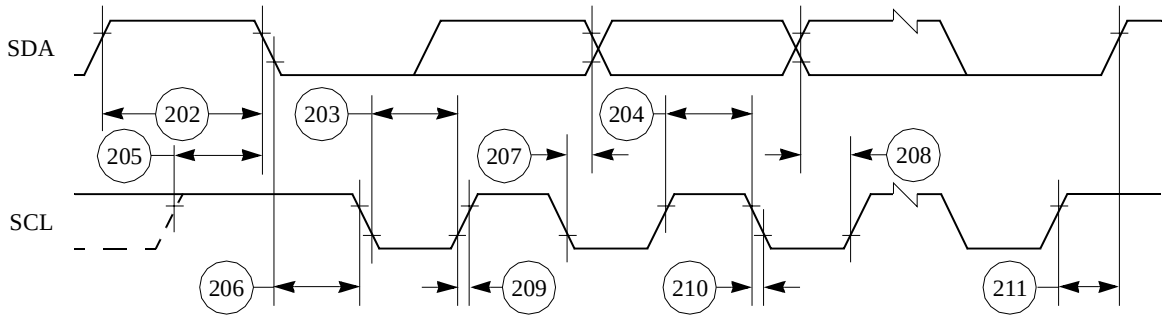



**Figure 61. I²C Bus Timing Diagram**

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

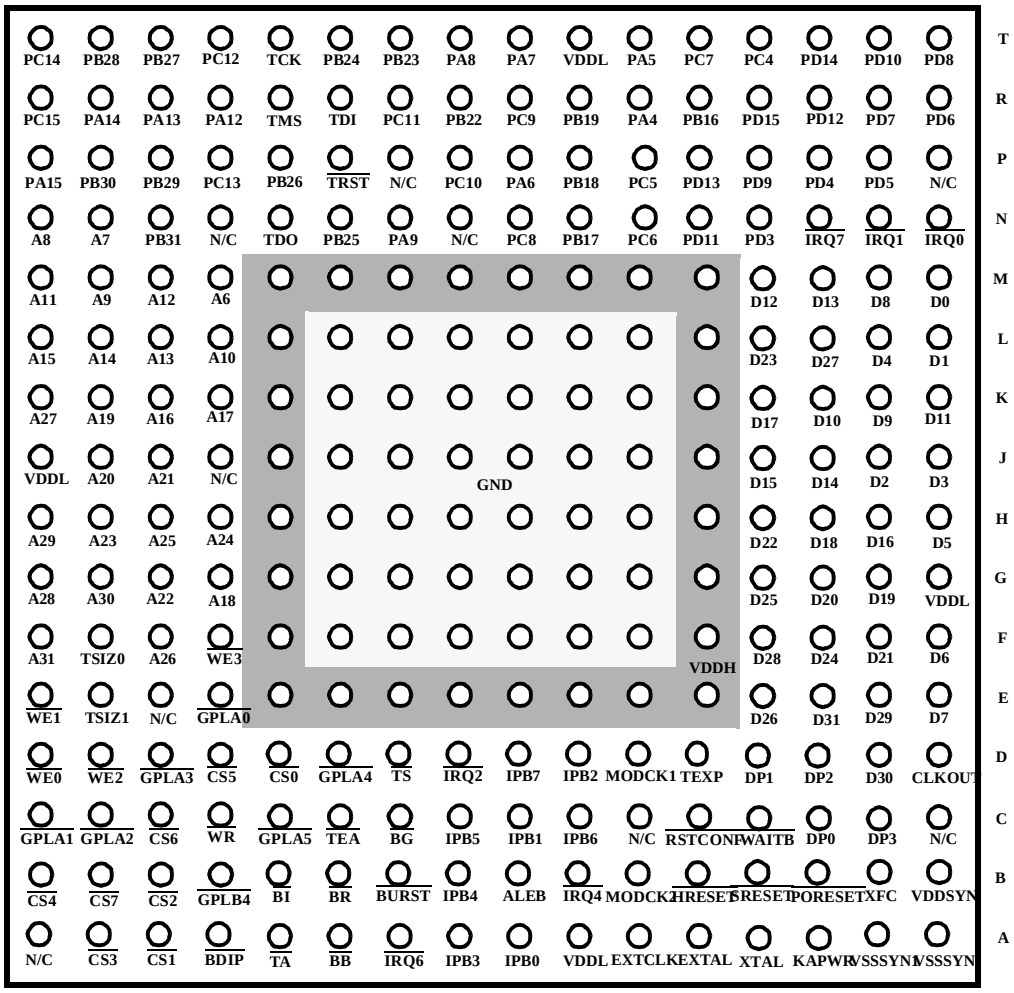
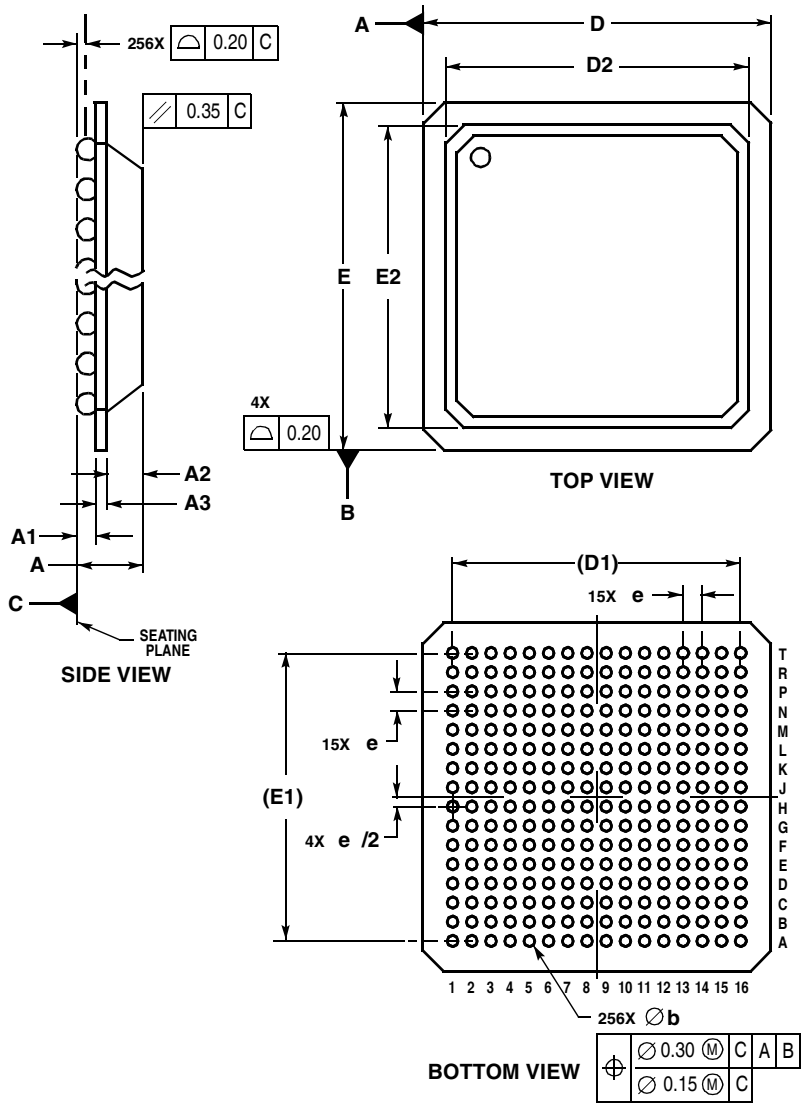



**Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard**

Figure 64 shows the non-JEDEC package dimensions of the PBGA.




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND THE SEATING PLANE ARE

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.91 | 2.35 |
| A1 | 0.50 | 0.70 |
| A2 | 1.12 | 1.22 |
| A3 | 0.29 | 0.43 |
| b | 0.60 | 0.90 |
| D | 23.00 BSC | |
| D1 | 19.05 REF | |
| D2 | 19.00 | 20.00 |
| E | 23.00 BSC | |
| E1 | 19.05 REF | |
| E2 | 19.00 | 20.00 |
| e | 1.27 BSC | |

**Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard**

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