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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850czt66bu

- 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
 - Caches are two-way, set-associative
 - Physically addressed
 - Cache blocks can be updated with a 4-word line burst
 - Least-recently used (LRU) replacement algorithm
 - Lockable one-line granularity
- Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
- MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
 - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
 - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
 - Hardware bus monitor
 - Spurious interrupt monitor
 - Software watchdog
 - Periodic interrupt timer
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
 - Reset controller
 - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
 - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
 - Memory controller programmable to support most size and speed memory interfaces
 - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
 - Variable block sizes, 32 Kbytes to 256 Mbytes
 - Selectable write protection
 - On-chip bus arbiter supports one external bus master
 - Special features for burst mode support
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers

- Gate mode can enable/disable counting
- Interrupt can be masked on reference match and event capture
- Interrupts
 - Eight external interrupt request (IRQ) lines
 - Twelve port pins with interrupt capability
 - Fifteen internal interrupt sources
 - Programmable priority among SCCs and USB
 - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
 - Master (socket) interface, release 2.1 compliant
 - Single PCMCIA socket
 - Supports eight memory or I/O windows
- Communications processor module (CPM)
 - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
 - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 8 Kbytes of dual-port RAM
 - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
 - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
 - Can be connected to any SCC, SMC, or USB
 - Allow changes during operation
 - Autobaud support option
- Two SCCs (serial communications controllers)
 - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
 - HDLC/SDLC™ (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support PPP (point-to-point protocol)
 - AppleTalk®
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input low voltage	VIL	GND	0.8	V
EXTAL, EXTCLK input high voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input leakage current, Vin = 5.5 V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I _{in}	—	100	μA
Input leakage current, Vin = 3.6V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I _{in}	—	10	μA
Input leakage current, Vin = 0V (Except TMS, $\overline{\text{TRST}}$, DSCK and DSDI pins)	I _{in}	—	10	μA
Input capacitance	C _{in}	—	20	pF
Output high voltage, IOH = -2.0 mA, VDDH = 3.0V except XTAL, XFC, and open-drain pins	VOH	2.4	—	V
Output low voltage CLKOUT ³ IOL = 3.2 mA ¹ IOL = 5.3 mA ² IOL = 7.0 mA PA[14]/ $\overline{\text{USBOE}}$, PA[12]/TXD2 IOL = 8.9 mA $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BI}}$, $\overline{\text{BB}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$	VOL	—	0.5	V

¹ A[6:31], TSIZ0/ $\overline{\text{REG}}$, TSIZ1, D[0:31], DP[0:3]/ $\overline{\text{IRQ}}[3:6]$, RD/ $\overline{\text{WR}}$, BURST, RSV/ $\overline{\text{IRQ2}}$, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/ $\overline{\text{IOIS16_B/AT2}}$, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/ $\overline{\text{PTR/AT3}}$, PA[15]/ $\overline{\text{USBRXD}}$, PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/TOUT1/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/TOUT2/TIN4, PB[31]/SPISEL, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/BRGO1, PB[26]/I2CSCL/BRGO2, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/SDACK1, PB[22]/SMSYN2/SDACK2, PB[19]/L1ST1, PB[18]/RTS2/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/DREQ0/L1ST5, PC[14]/DREQ1/RTS2/L1ST6, PC[13]/L1ST7/RTS3, PC[12]/L1RQa/L1ST8, PC[11]/ $\overline{\text{USBRXP}}$, PC[10]/TGATE1/ $\overline{\text{USBRXN}}$, PC[9]/CTS2, PC[8]/CD2/TGATE1, PC[7]/ $\overline{\text{USBTXP}}$, PC[6]/ $\overline{\text{USBTXN}}$, PC[5]/CTS3/L1TSYNCA/SDACK1, PC[4]/CD3/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

² $\overline{\text{BDIP/GPL_B5}}$, $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ/ $\overline{\text{IRQ6}}$, $\overline{\text{CS}}[0:5]$, $\overline{\text{CS6/CE1_B}}$, $\overline{\text{CS7/CE2_B}}$, $\overline{\text{WE0/BS_AB0/IORD}}$, $\overline{\text{WE1/BS_AB1/IOWR}}$, $\overline{\text{WE2/BS_AB2/PCOE}}$, $\overline{\text{WE3/BS_AB3/PCWE}}$, $\overline{\text{GPL_A0/GPL_B0}}$, $\overline{\text{OE/GPL_A1/GPL_B1}}$, $\overline{\text{GPL_A2:3/GPL_B2:3/CS2:3}}$, UPWAITA/ $\overline{\text{GPL_A4/AS}}$, UPWAITB/ $\overline{\text{GPL_B4}}$, $\overline{\text{GPL_A5}}$, $\overline{\text{ALE_B/DSCK/AT1}}$, OP2/MODCK1/STS, OP3/MODCK2/DSDO

³ The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, IOH and IOL for Clkout should be extracted from the IBIS model at any output voltage level.

5 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the equation:

$$T_J = T_A + (P_D \cdot \theta_{JA})(1)$$

where

$$T_A = \text{Ambient temperature, } ^\circ\text{C}$$

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = 0,1	—	8.00	—	8.00	—	8.00	—	50.00	ns
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	—	50.00	ns
B24	A[6–31] to \overline{CS} asserted GPCM ACS = 10, TRLX = 0.	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B24a	A[6–31] to \overline{CS} asserted GPCM ACS = 11, TRLX = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B25	CLKOUT rising edge to \overline{OE} , WE[0–3] asserted	—	9.00	—	9.00	—	9.00	—	50.00	ns
B26	CLKOUT rising edge to \overline{OE} negated	2.00	9.00	2.00	9.00	2.00	9.00	—	50.00	ns
B27	A[6–31] to \overline{CS} asserted GPCM ACS = 10, TRLX = 1	23.00	—	36.00	—	29.00	—	1.250	50.00	ns
B27a	A[6–31] to \overline{CS} asserted GPCM ACS = 11, TRLX = 1	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B28	CLKOUT rising edge to WE[0–3] negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	50.00	ns
B28a	CLKOUT falling edge to WE[0–3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	—	12.00	—	14.00	—	13.00	0.250	50.00	ns

Figure 2 is the control timing diagram.

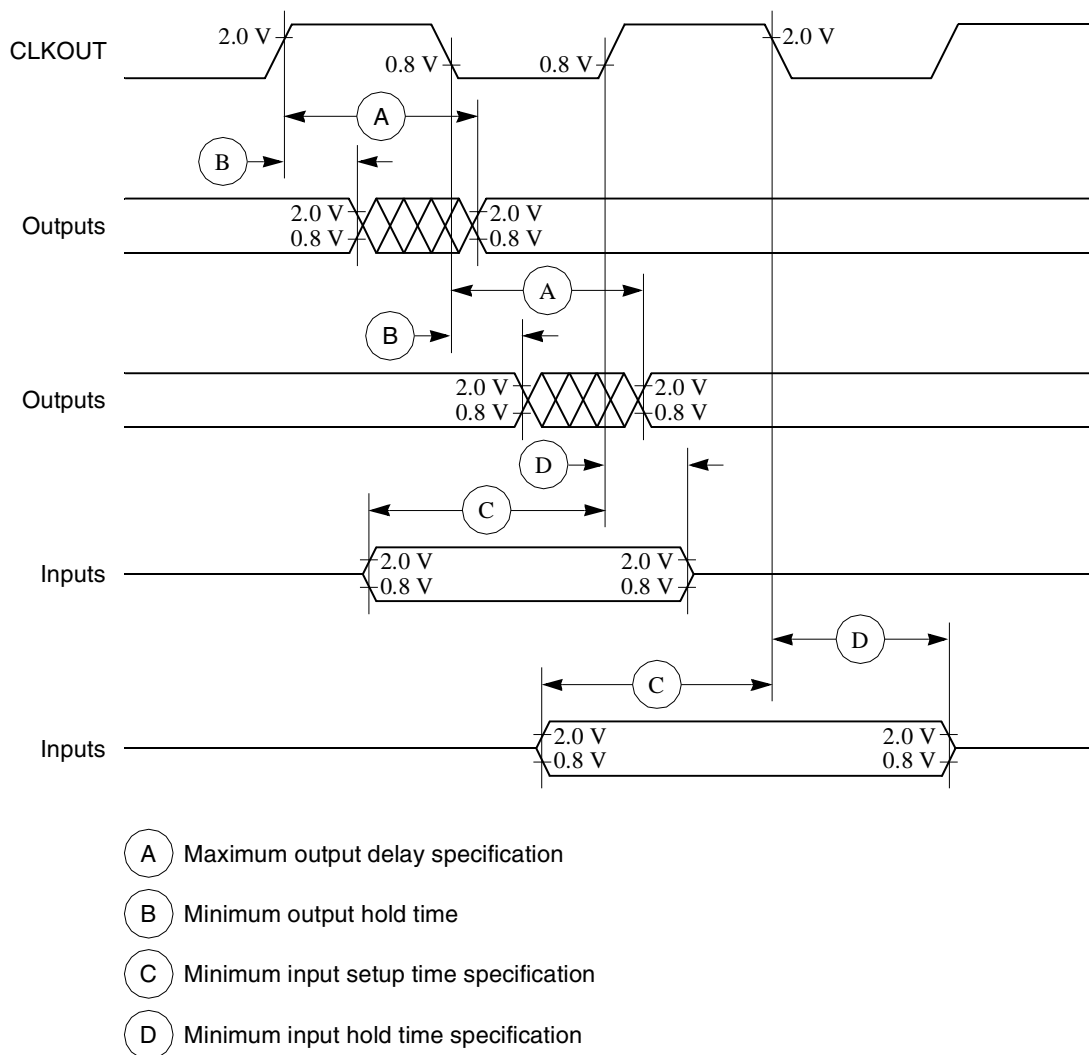


Figure 2. Control Timing

Figure 3 provides the timing for the external clock.

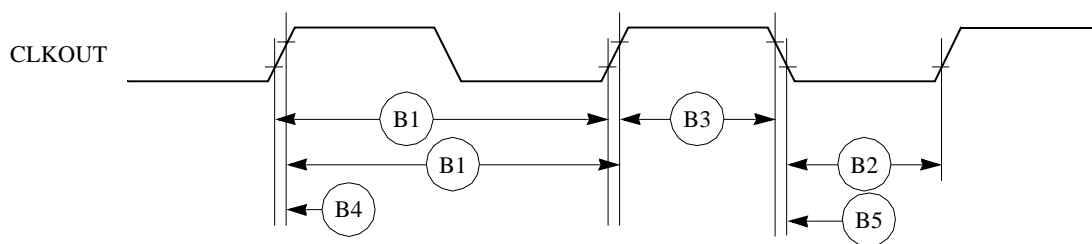


Figure 3. External Clock Timing

Figure 6 provides the timing for the synchronous input signals.

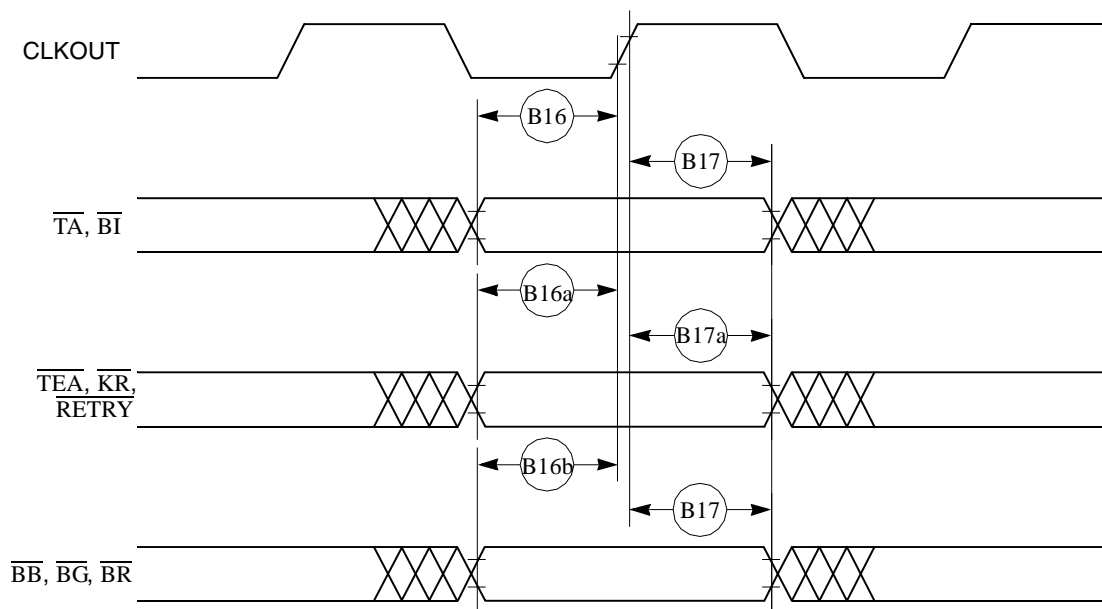


Figure 6. Synchronous Input Signals Timing

Figure 7 provides normal case timing for input data.

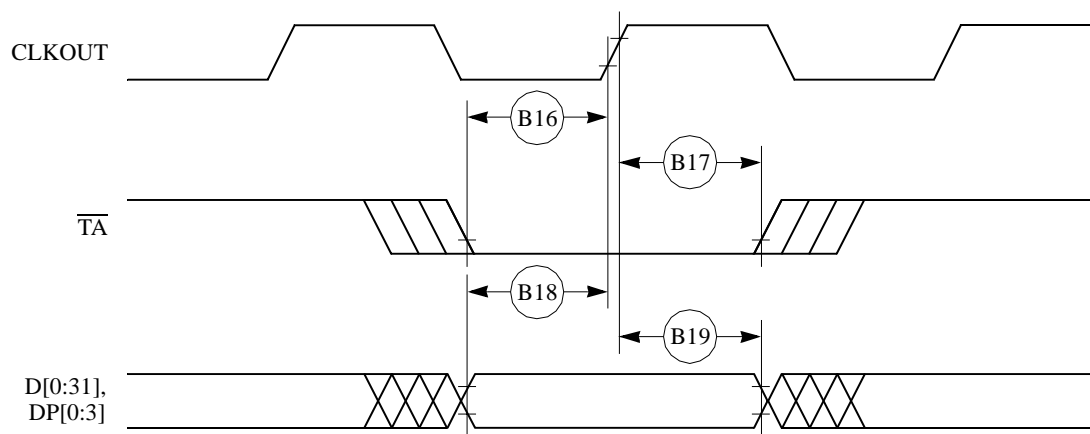


Figure 7. Input Data Timing in Normal Case

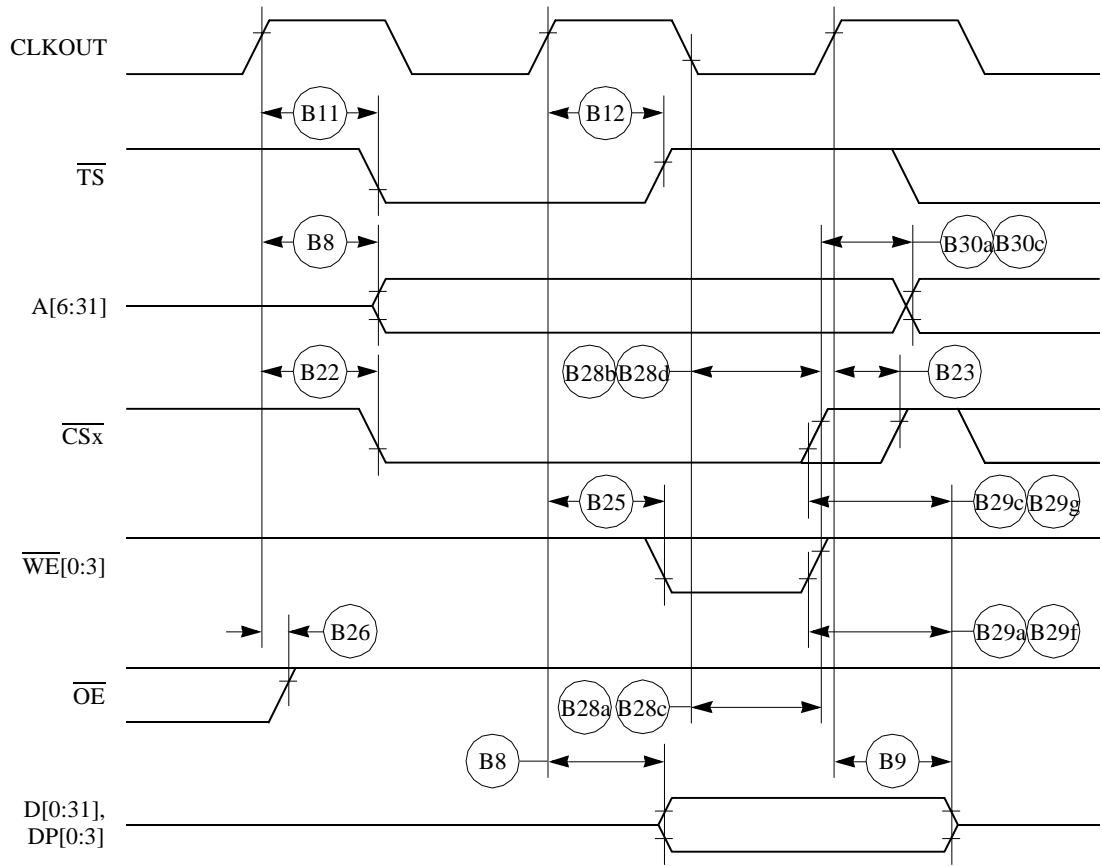


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

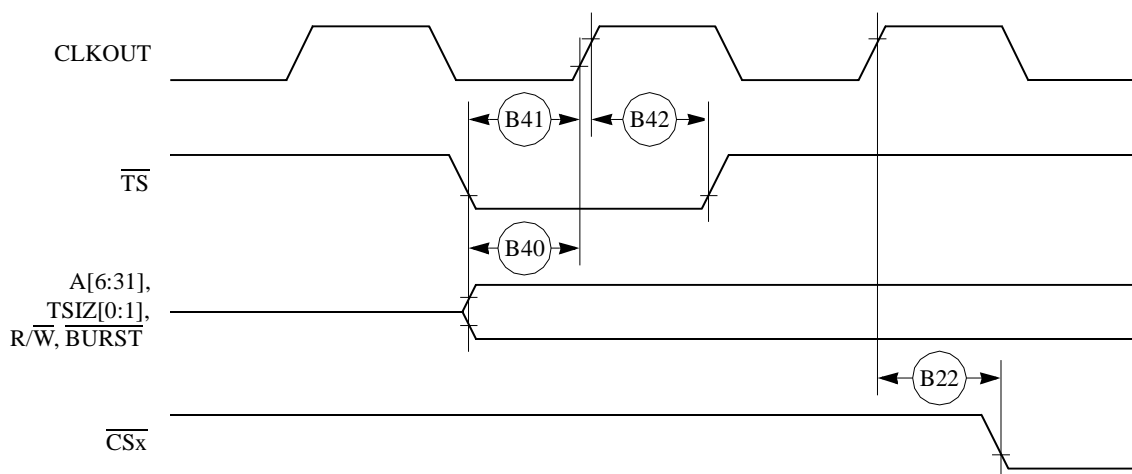


Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.

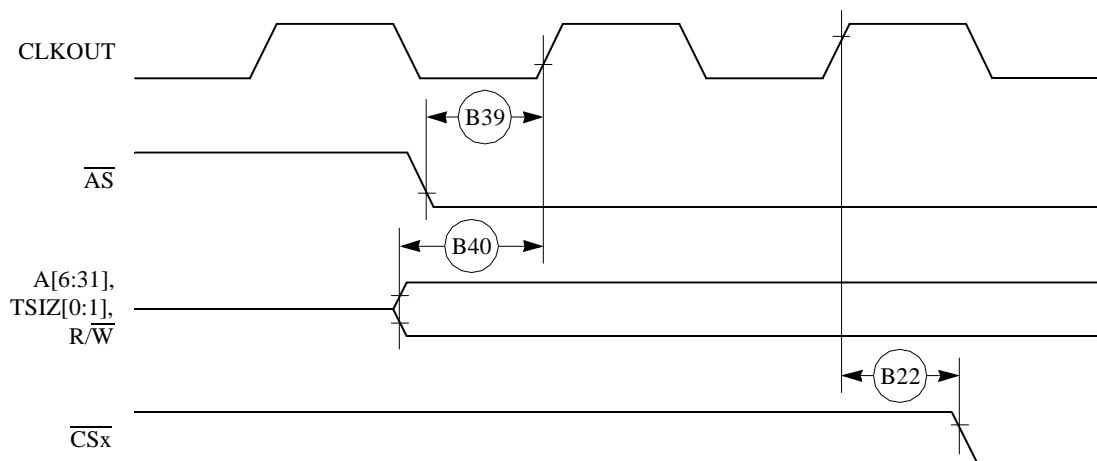


Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 21 provides the timing for the asynchronous external master control signals negation.

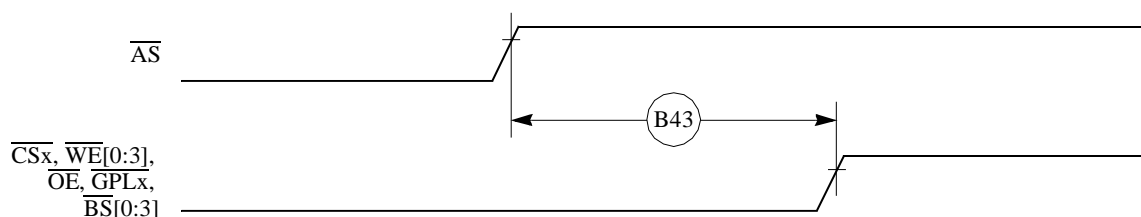


Figure 21. Asynchronous External Master—Control Signals Negation Timing

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

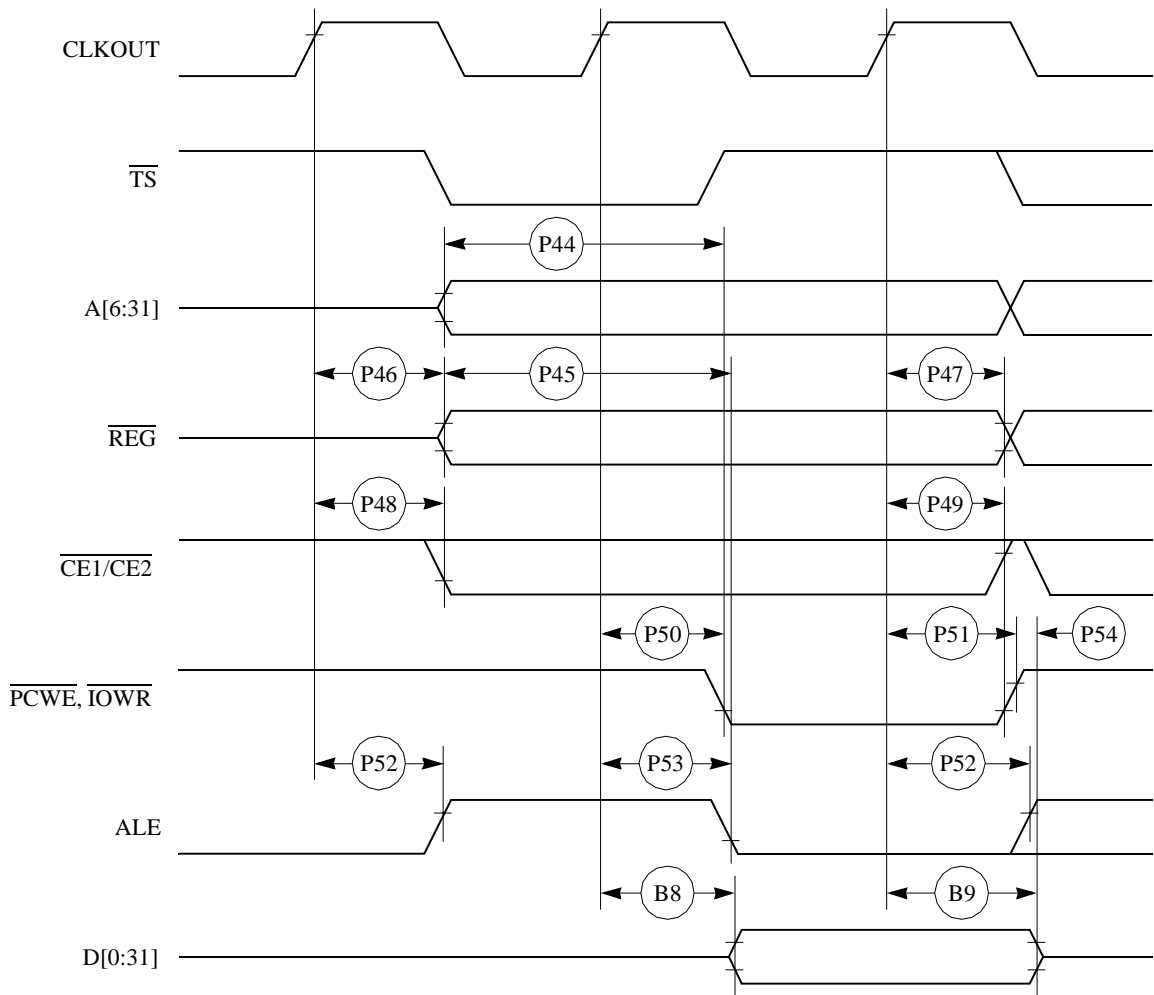


Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.

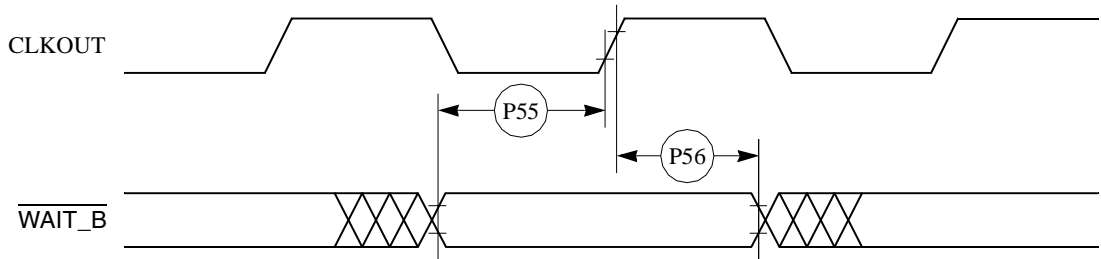


Figure 26. PCMCIA $\overline{\text{WAIT}}$ Signal Detection Timing

Table 10 shows the debug port timing for the MPC850.

Table 10. Debug Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
D61	DSCK cycle time	60.00	—	91.00	—	75.00	—	ns
D62	DSCK clock pulse width	25.00	—	38.00	—	31.00	—	ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	8.00	—	8.00	—	ns
D65	DSDI data hold time	5.00	—	5.00	—	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	0.00	2.00	ns

Figure 29 provides the input timing for the debug port clock.

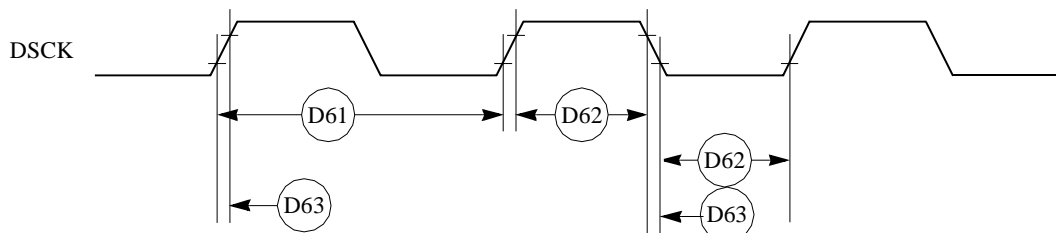


Figure 29. Debug Port Clock Input Timing

Figure 30 provides the timing for the debug port.

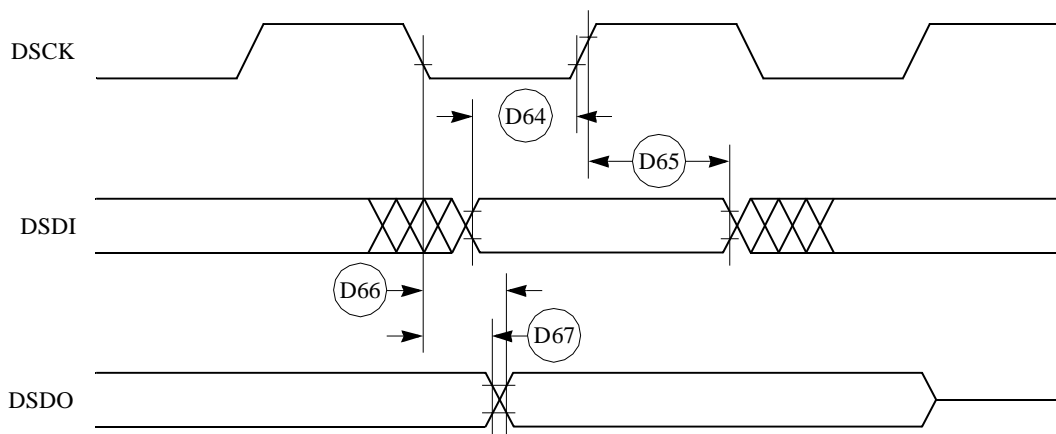


Figure 30. Debug Port Timings

Figure 31 shows the reset timing for the data bus configuration.

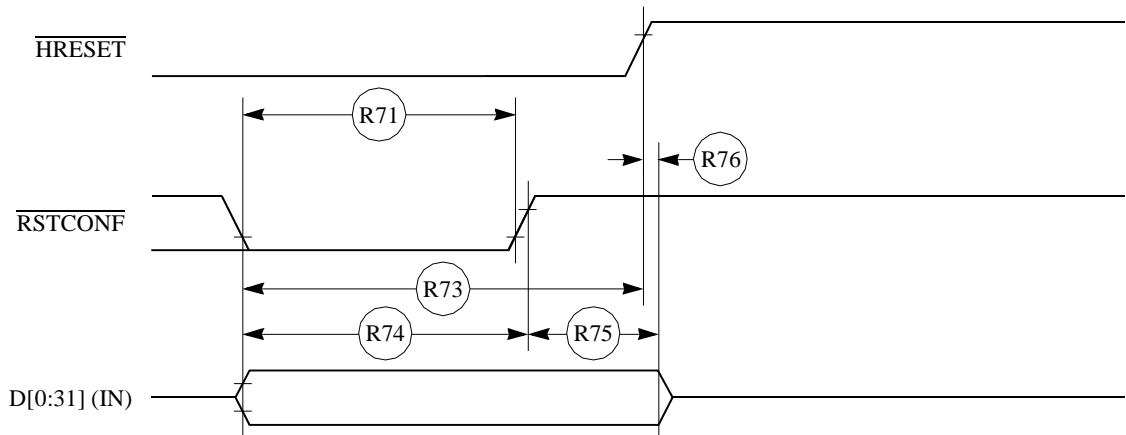


Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

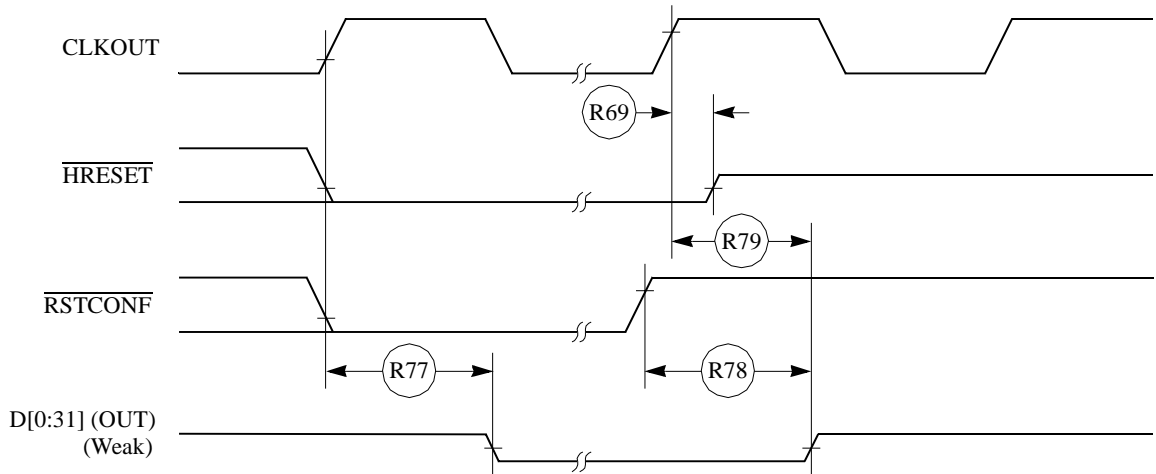


Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

Table 18. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency ¹ (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	—	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge ²	5.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	5.00	—	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency ¹ (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time	—	—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	40.00	—	ns
106	RXDx setup time to RCLKx rising edge	40.00	—	ns
107	RXDx hold time from RCLKx rising edge ²	0.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	40.00	—	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

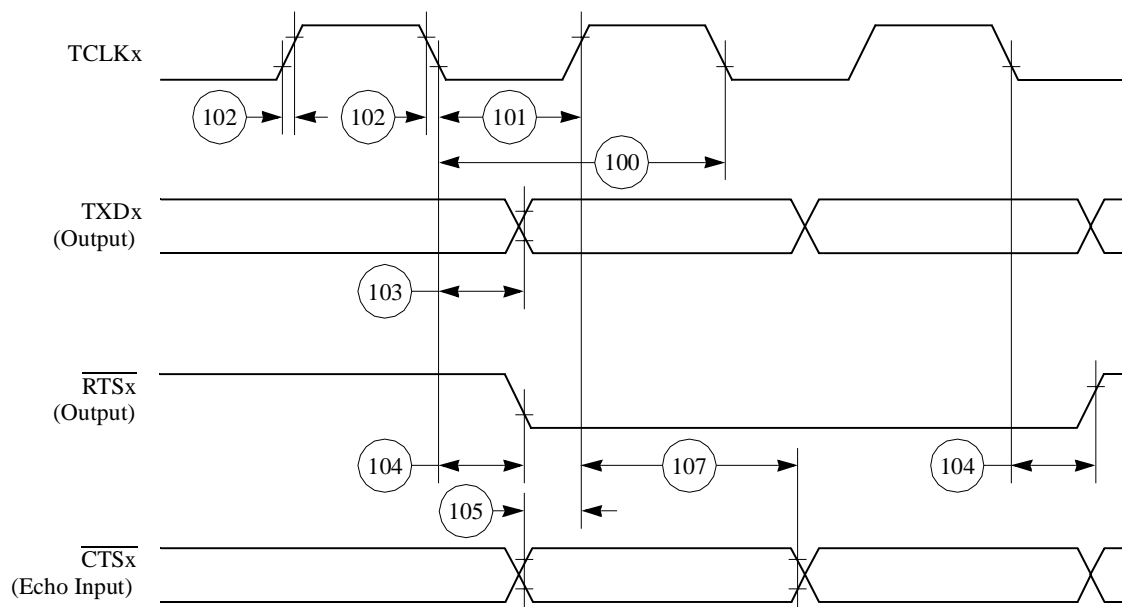


Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period ¹	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period ¹	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns

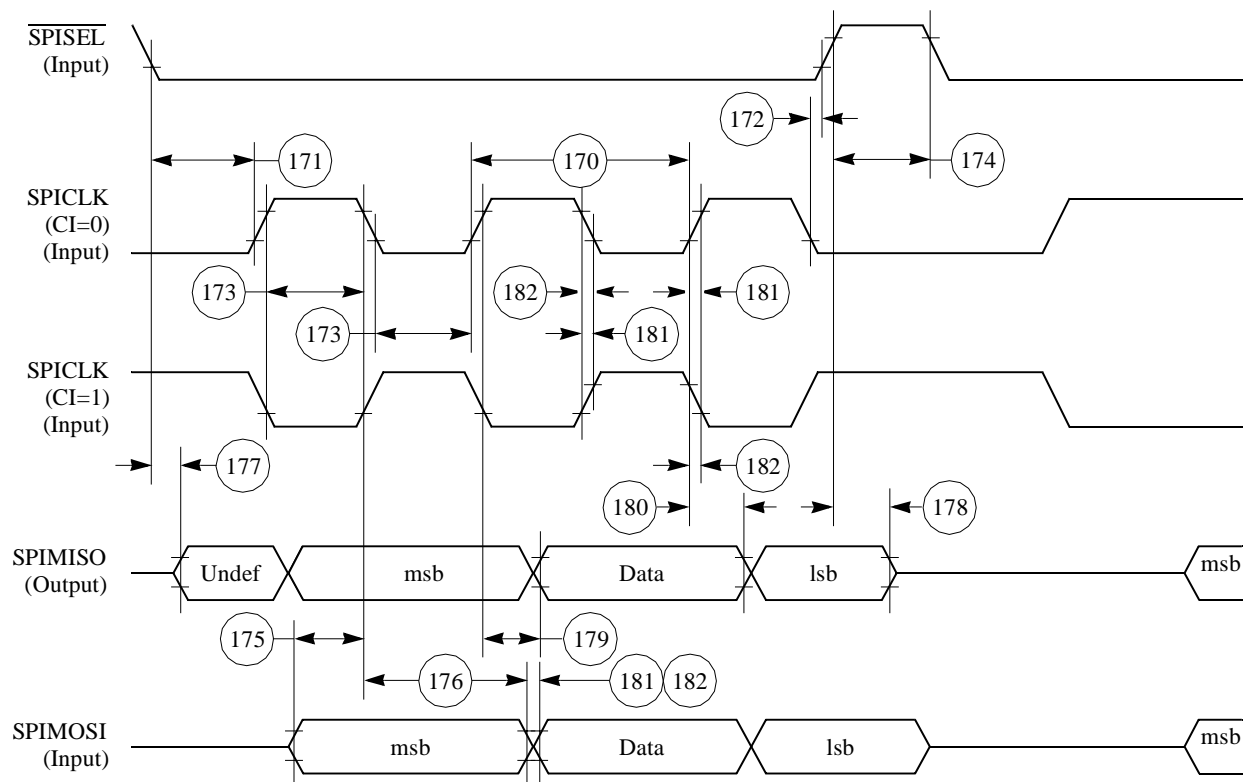


Figure 60. SPI Slave (CP = 1) Timing Diagram

8.11 I²C AC Electrical Specifications

Table 24 provides the I²C (SCL < 100 KHz) timings.

Table 24. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) ¹	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	—	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	—	ns
209	SDL/SCL rise time	—	1.00	μs

9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivatives

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

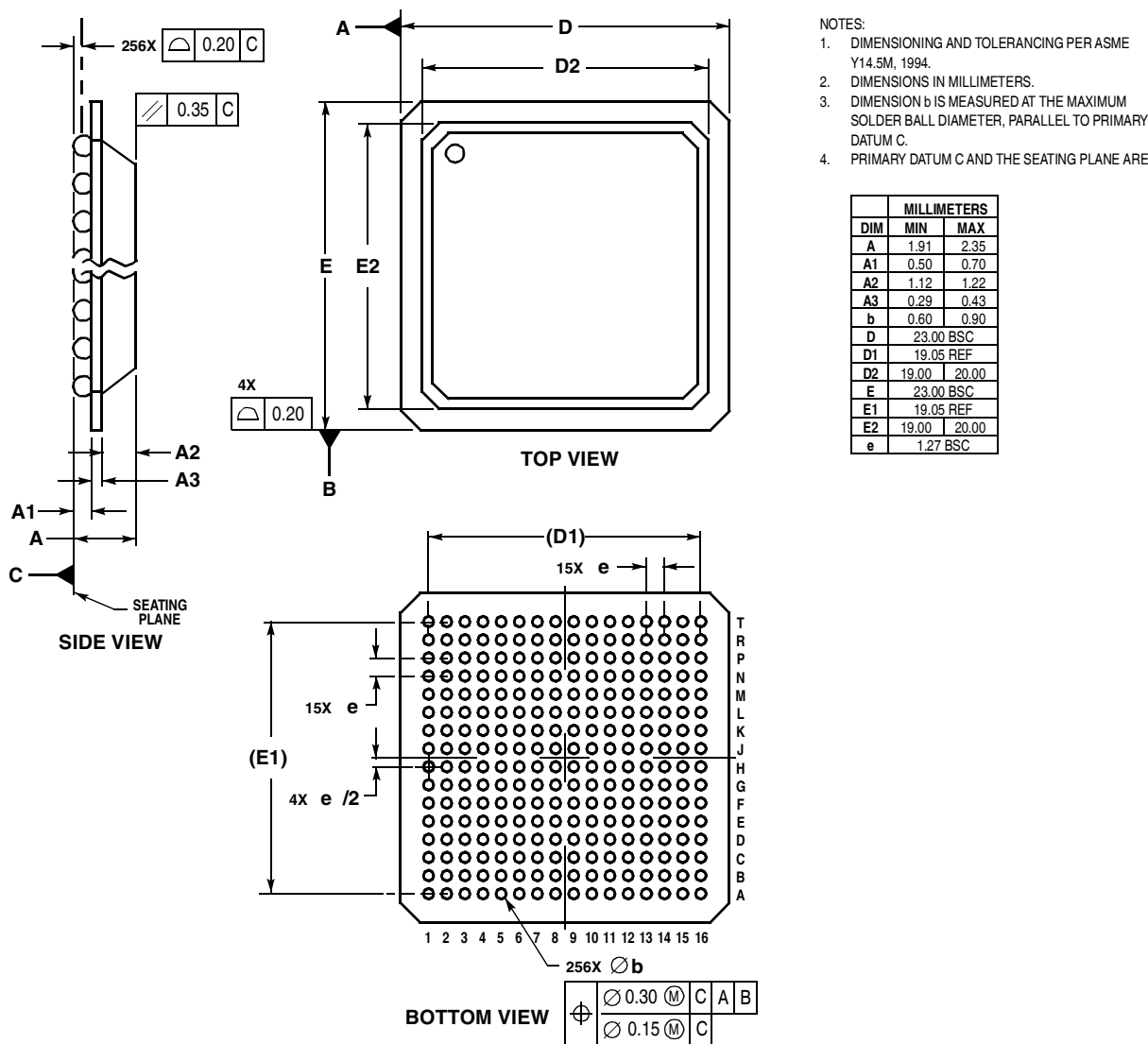
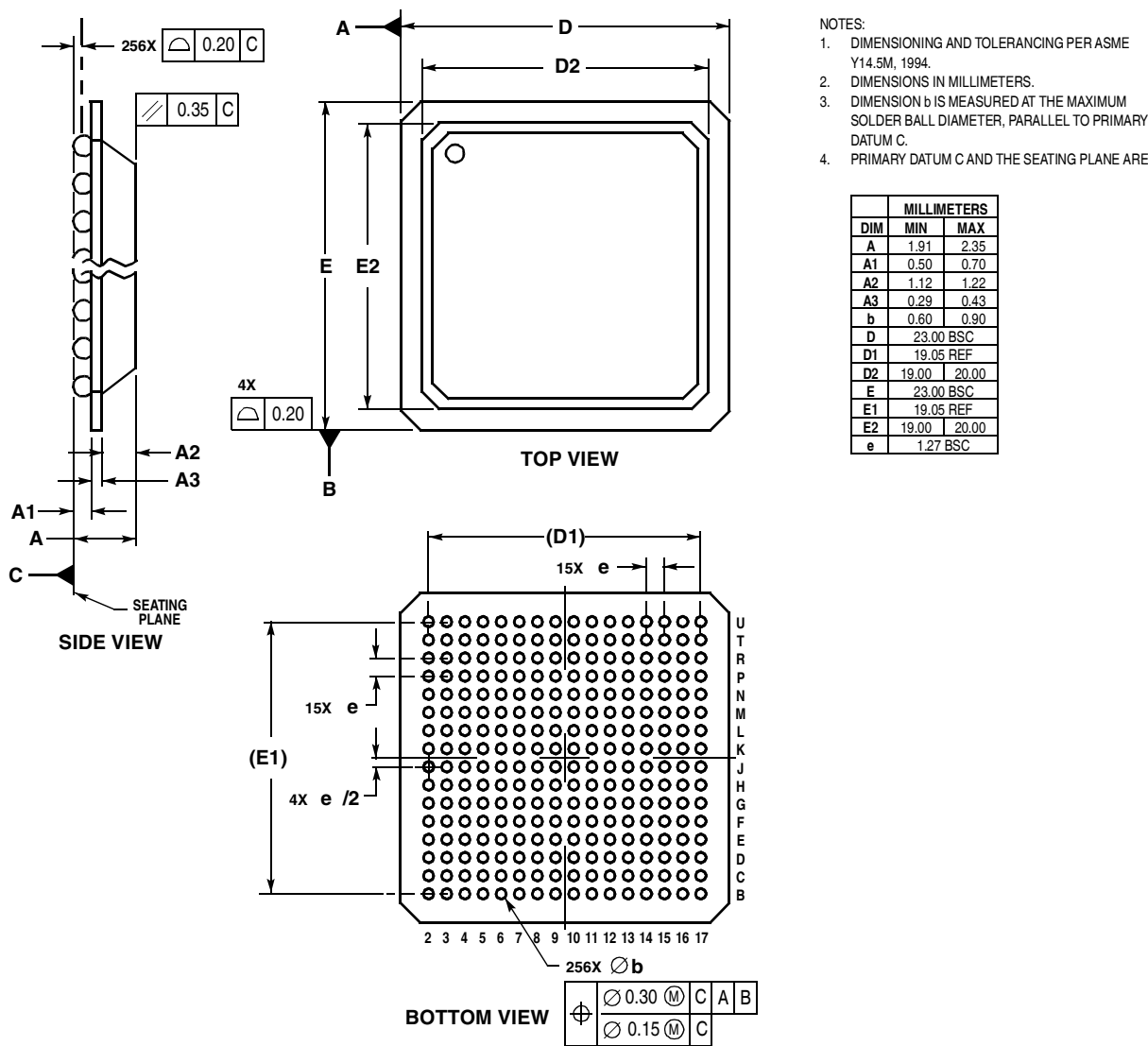


Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard

Figure 65 shows the JEDEC package dimensions of the PBGA.



CASE 1130-01
ISSUE B

Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard

10 Document Revision History

Table 28 lists significant changes between revisions of this document.

Table 28. Document Revision History

Revision	Date	Change
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.
0.2	04/2002	Updated power numbers and added Rev. C
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.



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