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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850decvr50bu

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:



Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
 - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution



Features

- 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
 - Caches are two-way, set-associative
 - Physically addressed
 - Cache blocks can be updated with a 4-word line burst
 - Least-recently used (LRU) replacement algorithm
 - Lockable one-line granularity
- Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
- MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
 - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
 - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
 - Hardware bus monitor
 - Spurious interrupt monitor
 - Software watchdog
 - Periodic interrupt timer
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
 - Reset controller
 - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
 - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
 - Memory controller programmable to support most size and speed memory interfaces
 - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
 - Variable block sizes, 32 Kbytes to 256 Mbytes
 - Selectable write protection
 - On-chip bus arbiter supports one external bus master
 - Special features for burst mode support
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers



Features

- QUICC multichannel controller (QMC) microcode features
 - Up to 64 independent communication channels on a single SCC
 - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
 - Supports either transparent or HDLC protocols for each channel
 - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
 - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C[®] (interprocessor-integrated circuit) port
 - Supports master and slave modes
 - Supports multimaster environment
- Time slot assigner
 - Allows SCCs and SMCs to run in multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame syncs, clocking
 - Allows dynamic changes
 - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
 - Full high: all units fully powered at high clock frequency
 - Full low: all units fully powered at low clock frequency
 - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and CPM in low-power standby
 - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
 - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
 - Low-power stop: to provide lower power dissipation



Bus Signal Timing

 θ_{IA} = Package thermal resistance, junction to ambient, °C/W

 $\begin{aligned} \mathbf{P}_{\mathrm{D}} &= \mathbf{P}_{\mathrm{INT}} + \mathbf{P}_{\mathrm{I/O}} \\ \mathbf{P}_{\mathrm{INT}} &= \mathbf{I}_{\mathrm{DD}} \ge \mathbf{V}_{\mathrm{DD}}, \text{ watts}\text{---chip internal power} \end{aligned}$

 $P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_I is:

 $P_{\rm D} = K \div (T_{\rm I} + 273^{\circ} \rm C)(2)$

Solving equations (1) and (2) for K gives:

 $\mathbf{K} = \mathbf{P}_{\mathrm{D}} \bullet (\mathbf{T}_{\mathrm{A}} + 273^{\circ}\mathrm{C}) + \mathbf{\theta}_{\mathrm{JA}} \bullet \mathbf{P}_{\mathrm{D}}^{2}(3)$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

5.1 Layout Practices

Each V_{CC} pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at http://www.mot.com/netcomm.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

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Table 6.	Bus	Operation	Timing	1
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Num	Chavastavistis	50 I	MHz	66 I	MHz	80 1	MHz	FEACT	Cap Load	
NUM	Characteristic	Min	Мах	Min	Max	Min	Мах	FFACI	50 pF)	Unit
B1	CLKOUT period	20	_	30.30	—	25	—	—		ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	—	50.00	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	_	50.00	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) 2	-0.60	0.60	-0.60	0.60	-0.60	0.60	—	50.00	ns
B1d	CLKOUT phase jitter ²	-2.00	2.00	-2.00	2.00	-2.00	2.00	—	50.00	ns
B1e	CLKOUT frequency jitter (MF < 10) ²	—	0.50	—	0.50	_	0.50	_	50.00	%
B1f	CLKOUT frequency jitter (10 < MF < 500) ²	—	2.00	—	2.00	_	2.00	—	50.00	%
B1g	CLKOUT frequency jitter (MF > 500) ²	_	3.00	—	3.00	_	3.00	_	50.00	%
B1h	Frequency jitter on EXTCLK ³	—	0.50	—	0.50	—	0.50	—	50.00	%
B2	CLKOUT pulse width low	8.00	_	12.12	—	10.00	_	—	50.00	ns
B3	CLKOUT width high	8.00	_	12.12	—	10.00	_	—	50.00	ns
B4	CLKOUT rise time	_	4.00	_	4.00	—	4.00	—	50.00	ns
B5	CLKOUT fall time	—	4.00	_	4.00	—	4.00	—	50.00	ns
B7	CLKOUT to A[6–31], RD/WR, BURST, D[0–31], DP[0–3] invalid	5.00		7.58	_	6.25	_	0.250	50.00	ns
B7a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3], BDIP, PTR invalid	5.00		7.58	—	6.25	—	0.250	50.00	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS[0–1], VF[0–2] IWP[0–2], LWP[0–1], STS invalid ⁴	5.00	_	7.58	—	6.25	—	0.250	50.00	ns
B8	CLKOUT to A[6–31], RD/WR, BURST, D[0–31], DP[0–3] valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8a	CLKOUT to TSIZ[0-1], REG, RSV, AT[0-3] BDIP, PTR valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8b	CLKOUT to BR, BG, VFLS[0–1], VF[0–2], IWP[0–2], FRZ, LWP[0–1], STS valid ⁴	5.00	11.74	7.58	14.33	6.25	13.00	0.250	50.00	ns



Bus Signal Timing

Num	Chavastavistis	50 I	MHz	66 I	MHz	80 I	MHz	FFACT	Cap Load	llmit
NUM	Characteristic	Min	Мах	Min	Max	Min	Мах	FFACI	50 pF)	Unit
B28c	CLKOUT falling edge to WE[0-3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	_	14.00	_	18.00		16.00	0.375	50.00	ns
B29	$\overline{WE[0-3]}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, CSNT = 0	3.00		6.00	—	4.00		0.250	50.00	ns
B29a	WE[0-3] negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	_	13.00	_	11.00		0.500	50.00	ns
B29b	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	_	6.00	_	4.00	_	0.250	50.00	ns
B29c	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	_	13.00		11.00		0.500	50.00	ns
B29d	$\overline{WE[0-3]}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	_	43.00	_	36.00		1.500	50.00	ns
B29e	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	_	43.00	_	36.00		1.500	50.00	ns
B29f	WE[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	_	9.00		7.00		0.375	50.00	ns
B29g	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	_	9.00		7.00		0.375	50.00	ns

Table 6.	Bus O	peration	Timing	1	(continued)
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Bus Signal Timing



Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)



Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.



Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)







Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)



Figure 17 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.



Figure 17. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing

Figure 18 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.



Figure 18. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing



Bus Signal Timing

Figure 25 provides the PCMCIA access cycle timing for the external bus write.



Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.



Figure 26. PCMCIA WAIT Signal Detection Timing



Table 11 shows the reset timing for the MPC850.

Table 11. Reset Timing

Num	um Characteristic		50 MHz		66MHz		MHz	FEACTOR	Unit
Num	Characteristic	Min	Max	Min	Max	Min	Max	TRETOR	Onne
R69	CLKOUT to HRESET high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to SRESET high impedance	—	20.00	—	20.00	_	20.00	—	ns
R71	RSTCONF pulse width	340.00	_	515.00	_	425.00	_	17.000	ns
R72		_	_	_	_	_	_	—	
R73	Configuration data to HRESET rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to RSTCONF rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after RSTCONF negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after HRESET negation	0.00	—	0.00	—	0.00	—	—	ns
R77	HRESET and RSTCONF asserted to data out drive	—	25.00	-	25.00	-	25.00	—	ns
R78	RSTCONF negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates HRESET to data out high impedance.	_	25.00	_	25.00	_	25.00	_	ns
R80	DSDI, DSCK set up	60.00	_	90.00	_	75.00	_	3.000	ns
R81	DSDI, DSCK hold time	0.00	_	0.00		0.00		—	ns
R82	SRESET negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns



CPM Electrical Characteristics



Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Num	Characteristic	All Free	Unit	
Num	Characteristic	Min	Мах	Onit
40	DREQ setup time to clock high	7.00	_	ns
41	DREQ hold time from clock high	3.00	_	ns
42	SDACK assertion delay from clock high	_	12.00	ns
43	SDACK negation delay from clock low	_	12.00	ns
44	SDACK negation delay from TA low	_	20.00	ns
45	SDACK negation delay from clock high		15.00	ns
46	\overline{TA} assertion to falling edge of the clock setup time (applies to external \overline{TA})	7.00	_	ns

Table 14. IDMA Controller Timing



Figure 39. IDMA External Requests Timing Diagram

	Table 17. SI Timing (cont	inued)		
	Oh ann a thuris tin	All Frequencies		11
NUM	Characteristic	Min	Мах	Unit
82	L1RCLK, L1TCLK frequency (DSC =1)	_	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83A	L1RCLK, L1TCLK width high (DSC = 1) ³	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)		30.00	ns
85	L1RQ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCLK
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	_	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

- 2 These specs are valid for IDL mode only.
- ³ Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.







CPM Electrical Characteristics



Figure 47. SI Transmit Timing Diagram



CPM Electrical Characteristics



Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)



CPM Electrical Characteristics

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

	Table 18.	NMSI	External	Clock	Timing
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Num	Characteristic	All Frequencie	Unit	
Num	Characteristic	Min	Max	Onit
100	RCLKx and TCLKx frequency 1 (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	_	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	RTSx active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	CTSx setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge ²	5.00	—	ns
108	CDx setup time to RCLKx rising edge	5.00	—	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Charactoristic	All Fr	Unit	
Nulli	Characteristic	Min	Мах	onn
100	RCLKx and TCLKx frequency 1 (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time		—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	RTSx active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	CTSx setup time to TCLKx rising edge	40.00	—	ns
106	RXDx setup time to RCLKx rising edge	40.00	—	ns
107	RXDx hold time from RCLKx rising edge ²	0.00	—	ns
108	CDx setup time to RCLKx rising edge	40.00		ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.



Num	Characteristic	All Frequencies		Unit
		Min	Max	Unit
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to SDACK asserted ²	—	20.00	ns
139	CLKOUT low to SDACK negated ²	—	20.00	ns

Table 20. Ethernet Timing (continued)

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame destination address into memory.



Figure 53. Ethernet Collision Timing Diagram



Figure 54. Ethernet Receive Timing Diagram



CPM Electrical Characteristics



Figure 55. Ethernet Transmit Timing Diagram

8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

Num	Characteristic	All Frequencies		Unit
		Min	Max	Unit
150	SMCLKx clock period ¹	100.00	—	ns
151	SMCLKx width low	50.00	—	ns
151a	SMCLKx width high	50.00	—	ns
152	SMCLKx rise/fall time	_	15.00	ns
153	SMTXDx active delay (from SMCLKx falling edge)	10.00	50.00	ns
154	SMRXDx/SMSYNx setup time	20.00	—	ns
155	SMRXDx/SMSYNx hold time	5.00	—	ns

Table 21.	Serial	Management	Controller	Timing
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¹ The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.



CPM Electrical Characteristics



Figure 60. SPI Slave (CP = 1) Timing Diagram

8.11 I²C AC Electrical Specifications

Table 24 provides the I^2C (SCL < 100 KHz) timings.

Table 24.	I ² C Timing	(SCL < 100 KHz)
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Num	Characteristic	All Frequencies		Unit
		Min	Max	Unit
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) ¹	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	—	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	_	ns
209	SDL/SCL rise time	—	1.00	μs