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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850deczt50bu">https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850deczt50bu</a>

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I<sup>2</sup>C port
- One serial peripheral interface (SPI).

[Table 1](#) shows the functionality supported by the members of the MPC850 family.

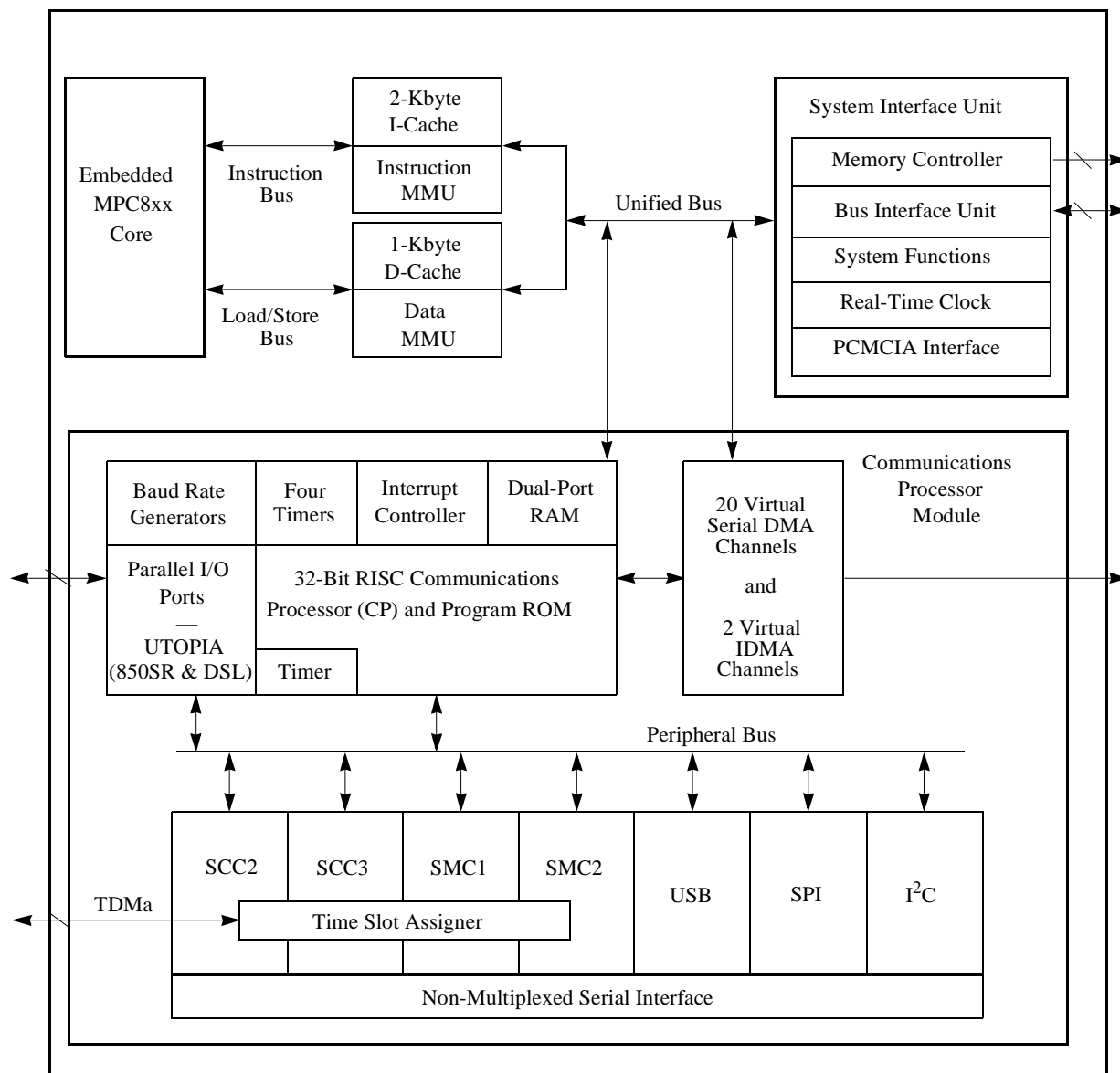
**Table 1. MPC850 Functionality Matrix**

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Additional documentation may be provided for parts listed in [Table 1](#).

## 2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:



**Figure 1. MPC850 Microprocessor Block Diagram**

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

- Gate mode can enable/disable counting
- Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

- QUICC multichannel controller (QMC) microcode features
  - Up to 64 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
  - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I<sup>2</sup>C<sup>®</sup> (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decremter, PLL, memory controller, real-time clock, and CPM in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input low voltage	VIL	GND	0.8	V
EXTAL, EXTCLK input high voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input leakage current, Vin = 5.5 V (Except TMS, $\overline{\text{TRST}}$ , DSCK and DSDI pins)	I <sub>in</sub>	—	100	μA
Input leakage current, Vin = 3.6V (Except TMS, $\overline{\text{TRST}}$ , DSCK and DSDI pins)	I <sub>in</sub>	—	10	μA
Input leakage current, Vin = 0V (Except TMS, $\overline{\text{TRST}}$ , DSCK and DSDI pins)	I <sub>in</sub>	—	10	μA
Input capacitance	C <sub>in</sub>	—	20	pF
Output high voltage, IOH = -2.0 mA, VDDH = 3.0V except XTAL, XFC, and open-drain pins	VOH	2.4	—	V
Output low voltage CLKOUT <sup>3</sup> IOL = 3.2 mA <sup>1</sup> IOL = 5.3 mA <sup>2</sup> IOL = 7.0 mA PA[14]/ $\overline{\text{USBOE}}$ , PA[12]/TXD2 IOL = 8.9 mA $\overline{\text{TS}}$ , $\overline{\text{TA}}$ , $\overline{\text{TEA}}$ , $\overline{\text{BI}}$ , $\overline{\text{BB}}$ , $\overline{\text{HRESET}}$ , $\overline{\text{SRESET}}$	VOL	—	0.5	V

<sup>1</sup> A[6:31], TSIZ0/ $\overline{\text{REG}}$ , TSIZ1, D[0:31], DP[0:3]/ $\overline{\text{IRQ}}[3:6]$ , RD/ $\overline{\text{WR}}$ , BURST, RSV/ $\overline{\text{IRQ2}}$ , IP\_B[0:1]/IWP[0:1]/VFLS[0:1], IP\_B2/ $\overline{\text{IOIS16\_B/AT2}}$ , IP\_B3/IWP2/VF2, IP\_B4/LWP0/VF0, IP\_B5/LWP1/VF1, IP\_B6/DSDI/AT0, IP\_B7/ $\overline{\text{PTR/AT3}}$ , PA[15]/ $\overline{\text{USBRXD}}$ , PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/TOUT1/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/TOUT2/TIN4, PB[31]/SPISEL, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/BRGO1, PB[26]/I2CSCL/BRGO2, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/SDACK1, PB[22]/SMSYN2/SDACK2, PB[19]/L1ST1, PB[18]/RTS2/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/DREQ0/L1ST5, PC[14]/DREQ1/RTS2/L1ST6, PC[13]/L1ST7/RTS3, PC[12]/L1RQa/L1ST8, PC[11]/ $\overline{\text{USBRXP}}$ , PC[10]/TGATE1/ $\overline{\text{USBRXN}}$ , PC[9]/CTS2, PC[8]/CD2/TGATE1, PC[7]/ $\overline{\text{USBTXP}}$ , PC[6]/ $\overline{\text{USBTXN}}$ , PC[5]/CTS3/L1TSYNCA/SDACK1, PC[4]/CD3/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

<sup>2</sup>  $\overline{\text{BDIP/GPL\_B5}}$ ,  $\overline{\text{BR}}$ ,  $\overline{\text{BG}}$ , FRZ/ $\overline{\text{IRQ6}}$ ,  $\overline{\text{CS}}[0:5]$ ,  $\overline{\text{CS6/CE1\_B}}$ ,  $\overline{\text{CS7/CE2\_B}}$ ,  $\overline{\text{WE0/BS\_AB0/IORD}}$ ,  $\overline{\text{WE1/BS\_AB1/IOWR}}$ ,  $\overline{\text{WE2/BS\_AB2/PCOE}}$ ,  $\overline{\text{WE3/BS\_AB3/PCWE}}$ ,  $\overline{\text{GPL\_A0/GPL\_B0}}$ ,  $\overline{\text{OE/GPL\_A1/GPL\_B1}}$ ,  $\overline{\text{GPL\_A2:3/GPL\_B2:3/CS2:3}}$ , UPWAITA/ $\overline{\text{GPL\_A4/AS}}$ , UPWAITB/ $\overline{\text{GPL\_B4}}$ ,  $\overline{\text{GPL\_A5}}$ ,  $\overline{\text{ALE\_B/DSCK/AT1}}$ , OP2/MODCK1/STS, OP3/MODCK2/SDO

<sup>3</sup> The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, IOH and IOL for Clkout should be extracted from the IBIS model at any output voltage level.

## 5 Power Considerations

The average chip-junction temperature, T<sub>J</sub>, in °C can be obtained from the equation:

$$T_J = T_A + (P_D \cdot \theta_{JA})(1)$$

where

$$T_A = \text{Ambient temperature, } ^\circ\text{C}$$

Figure 6 provides the timing for the synchronous input signals.

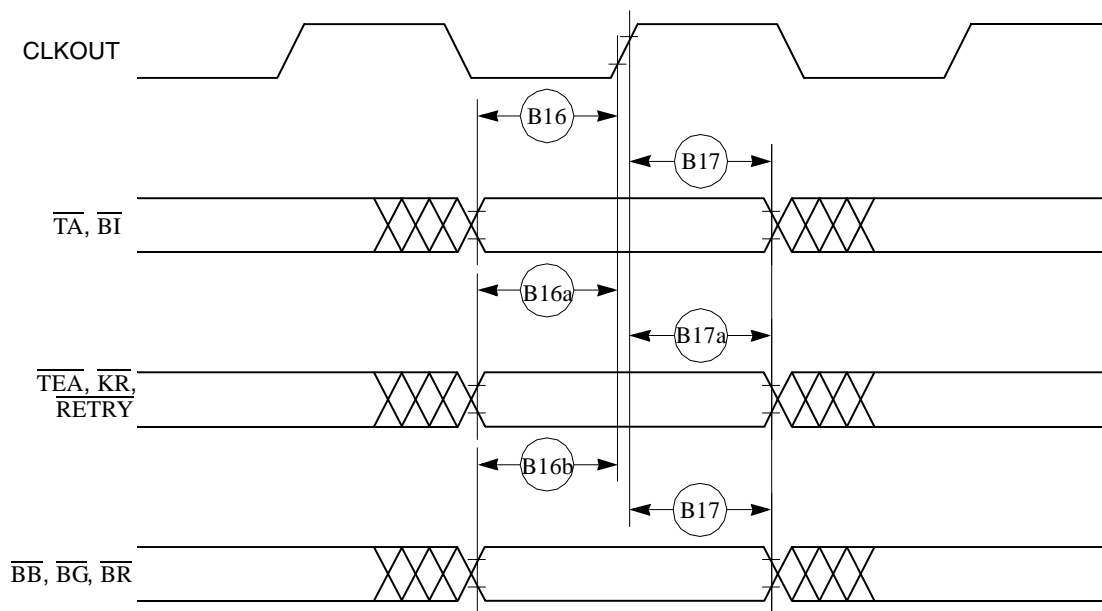


Figure 6. Synchronous Input Signals Timing

Figure 7 provides normal case timing for input data.

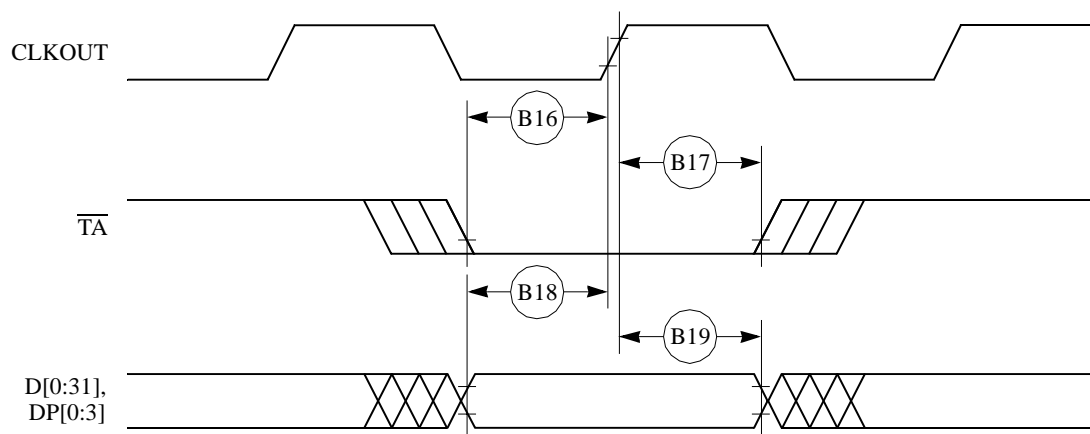
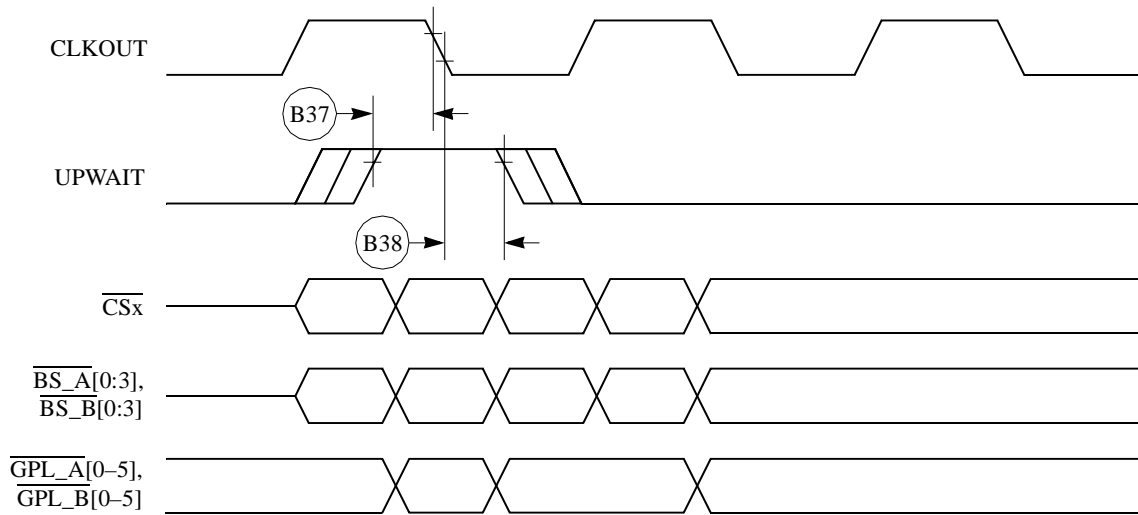


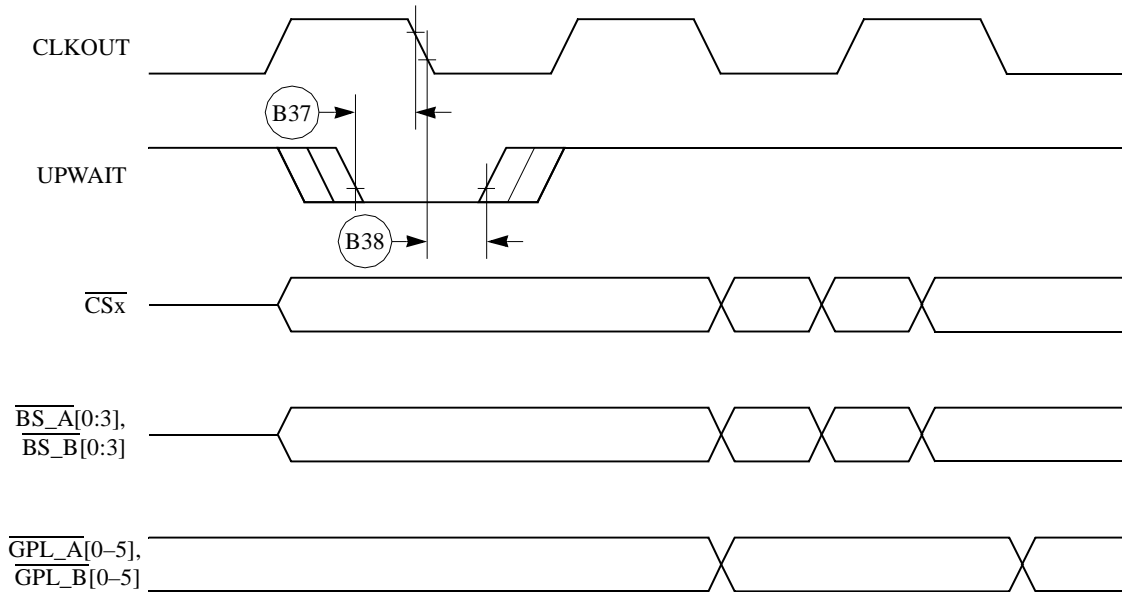
Figure 7. Input Data Timing in Normal Case

Figure 17 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.



**Figure 17. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing**

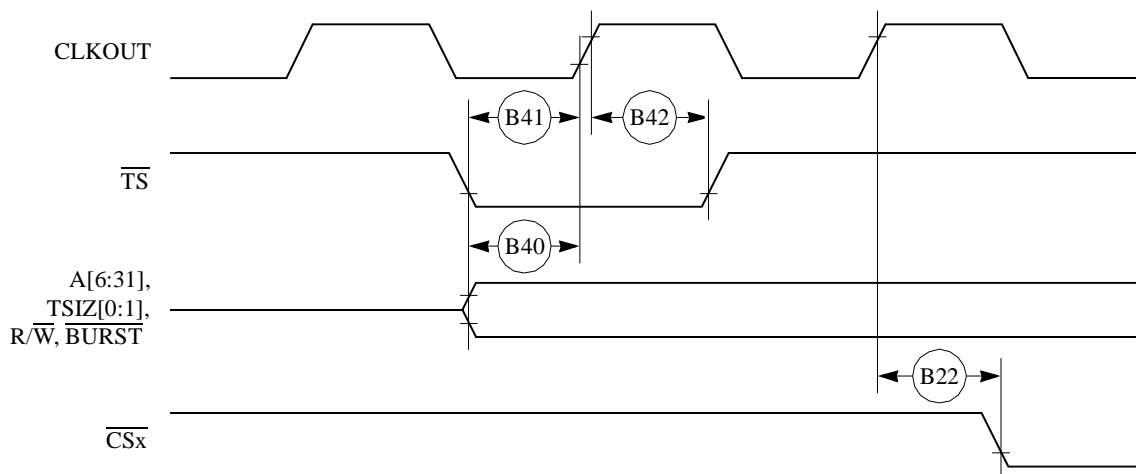
Figure 18 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.



**Figure 18. Asynchronous  $\overline{\text{UPWAIT}}$  Negated Detection in UPM Handled Cycles Timing**

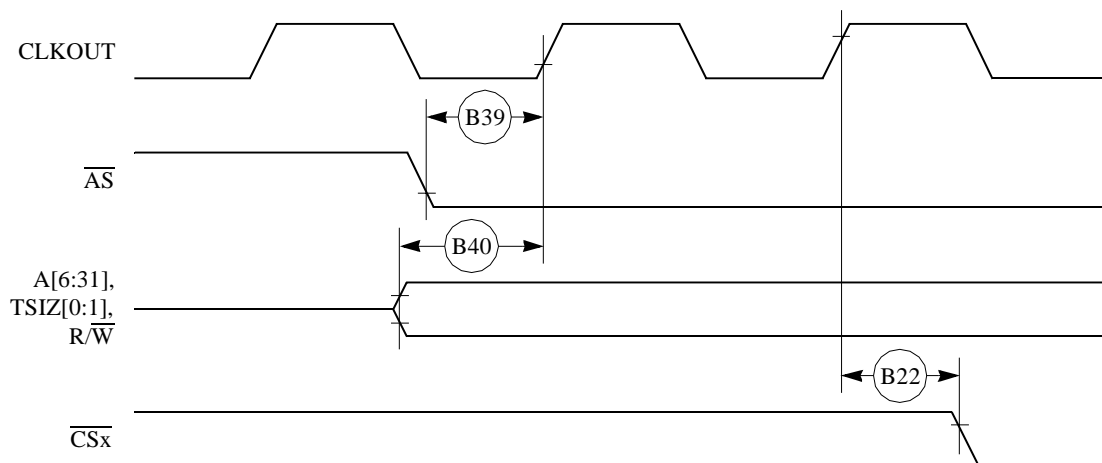


Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.



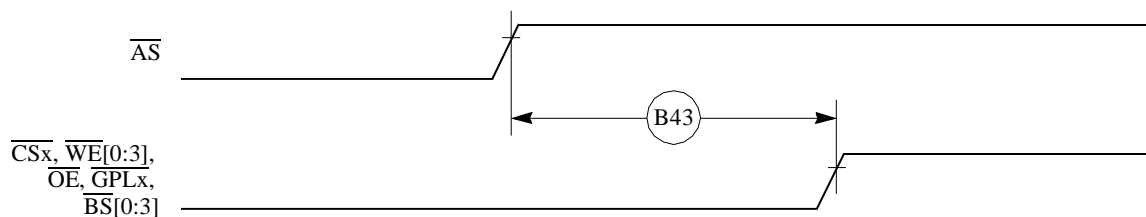
**Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)**

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.



**Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)**

Figure 21 provides the timing for the asynchronous external master control signals negation.



**Figure 21. Asynchronous External Master—Control Signals Negation Timing**

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

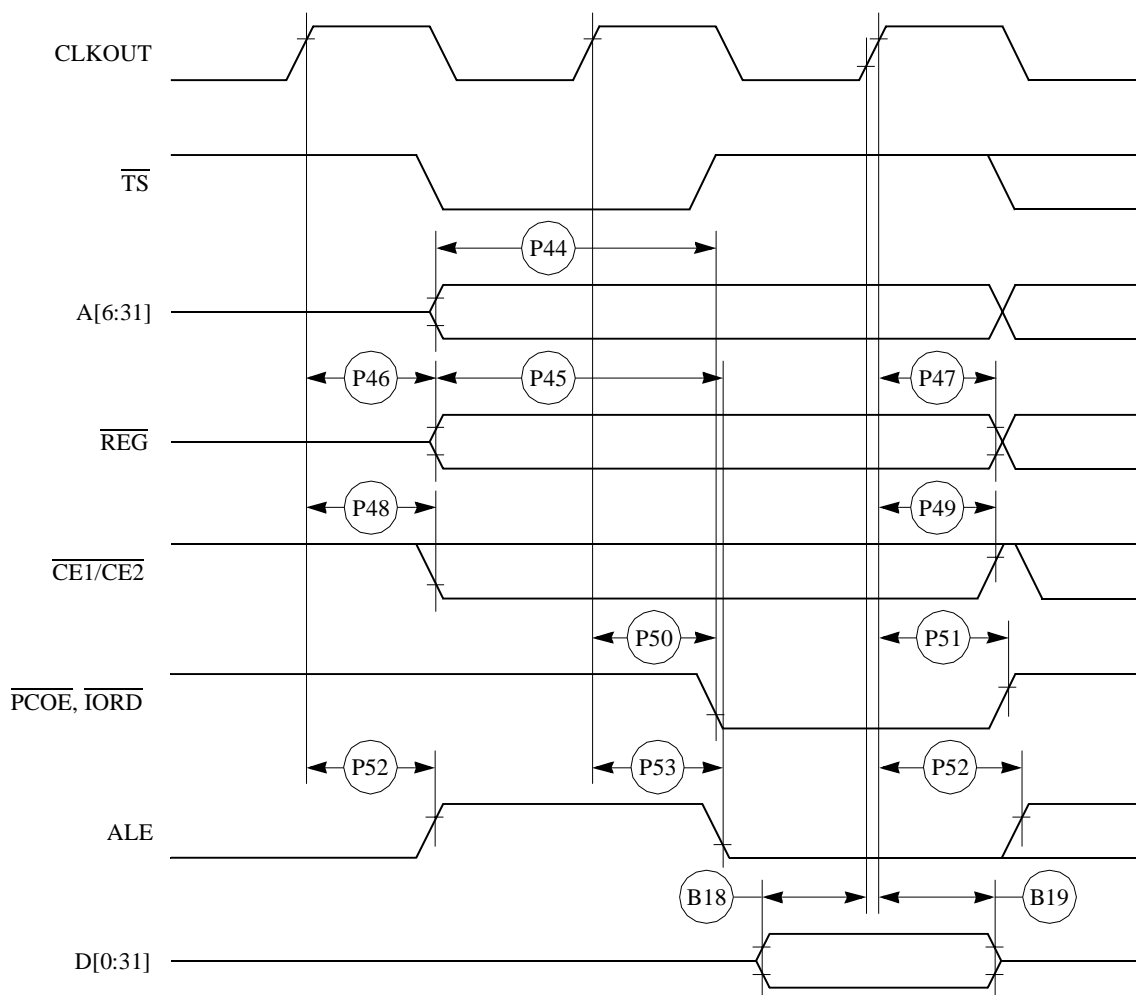


Figure 24. PCMCIA Access Cycles Timing External Bus Read

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

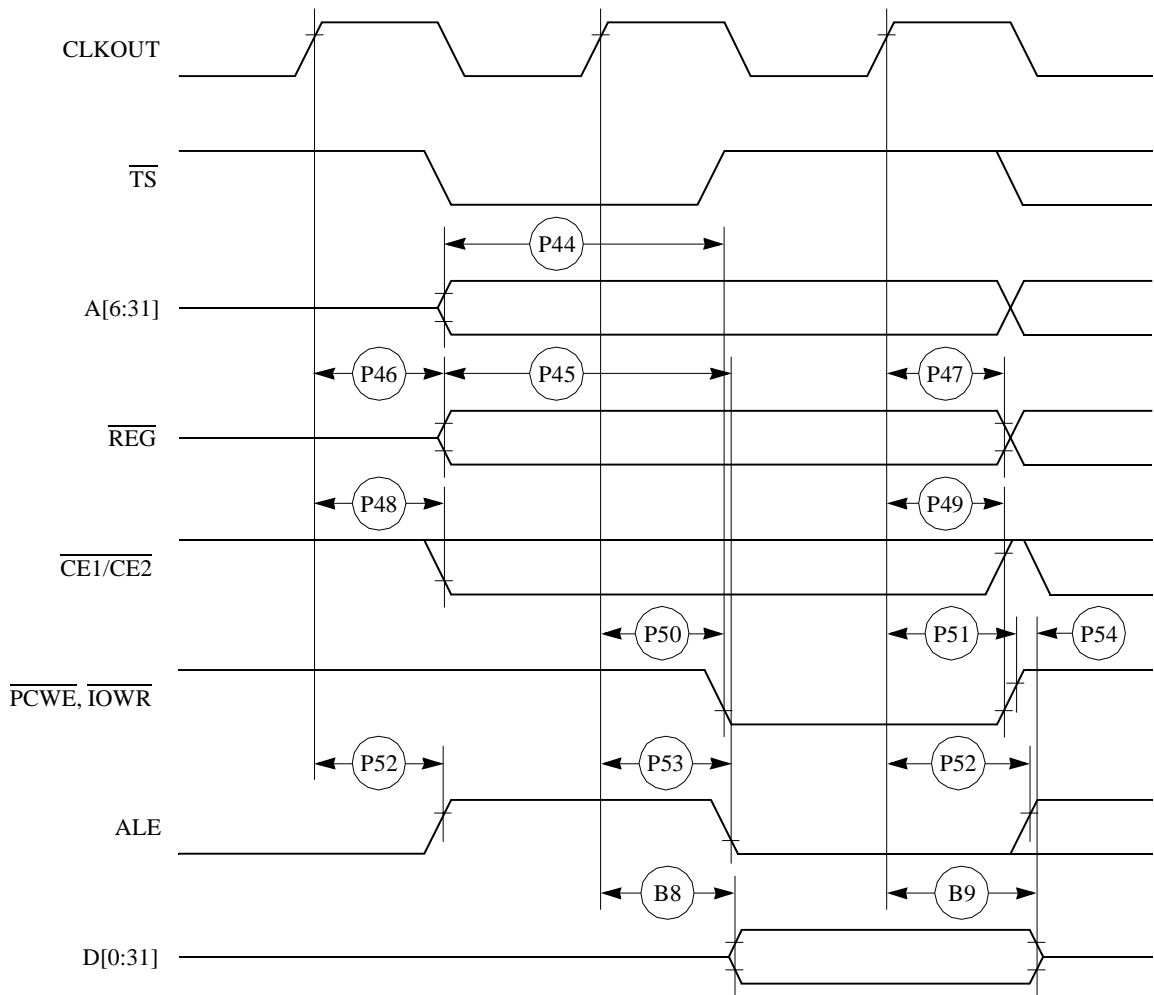


Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.

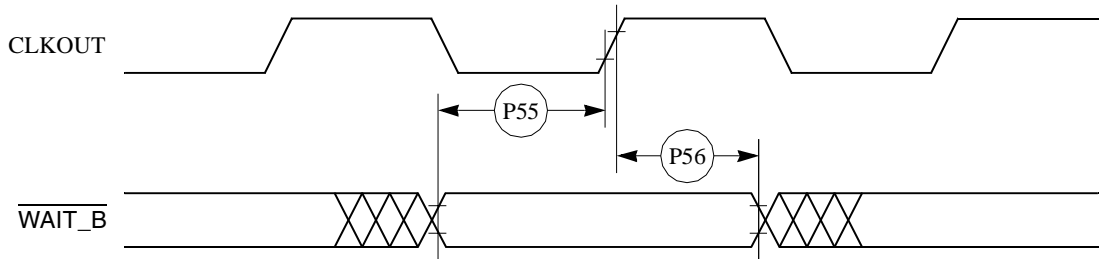


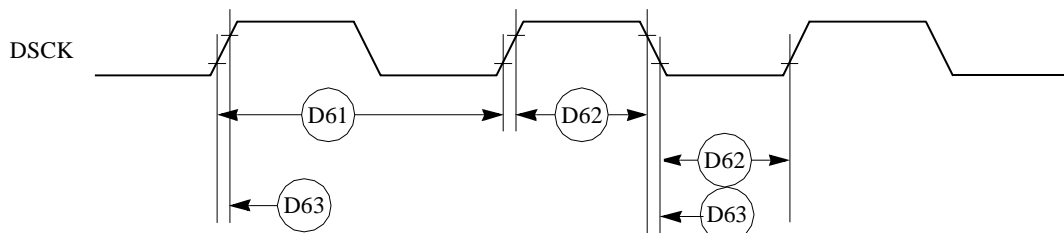
Figure 26. PCMCIA  $\overline{\text{WAIT}}$  Signal Detection Timing

Table 10 shows the debug port timing for the MPC850.

**Table 10. Debug Port Timing**

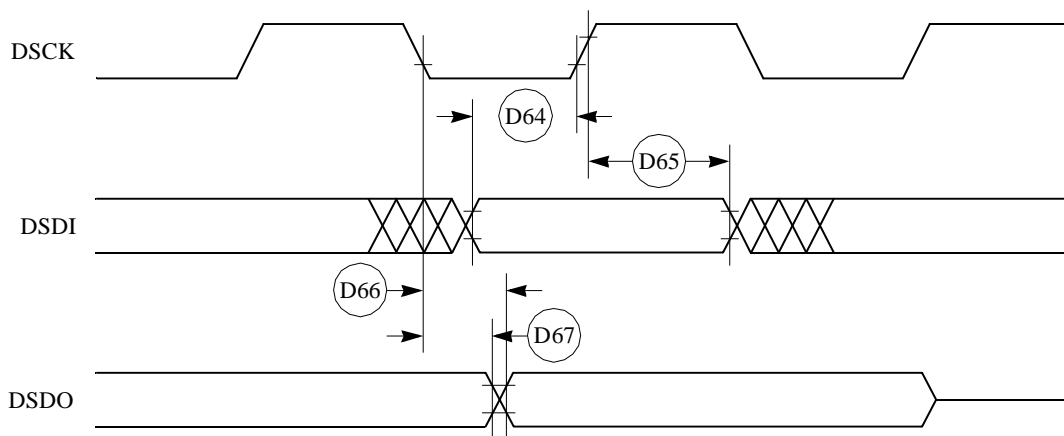
Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
D61	DSCK cycle time	60.00	—	91.00	—	75.00	—	ns
D62	DSCK clock pulse width	25.00	—	38.00	—	31.00	—	ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	8.00	—	8.00	—	ns
D65	DSDI data hold time	5.00	—	5.00	—	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	0.00	2.00	ns

Figure 29 provides the input timing for the debug port clock.



**Figure 29. Debug Port Clock Input Timing**

Figure 30 provides the timing for the debug port.



**Figure 30. Debug Port Timings**

Figure 31 shows the reset timing for the data bus configuration.

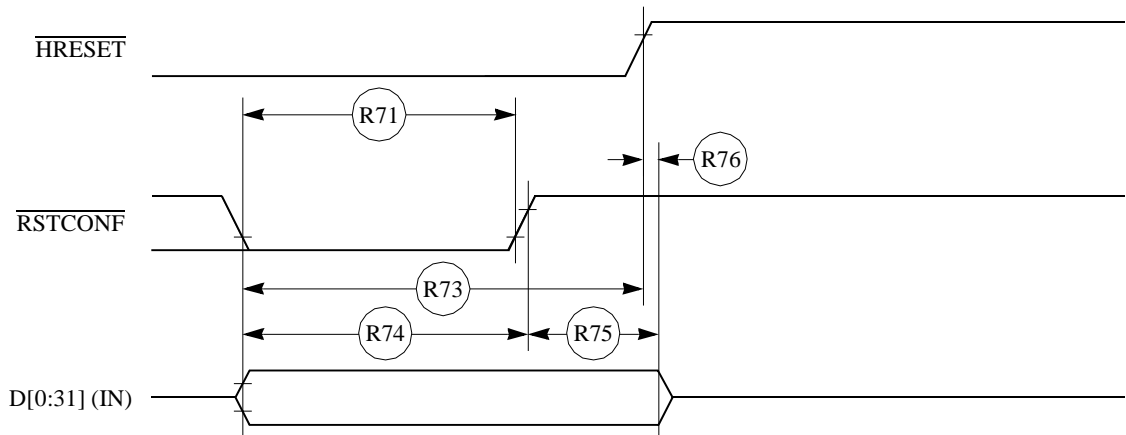


Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

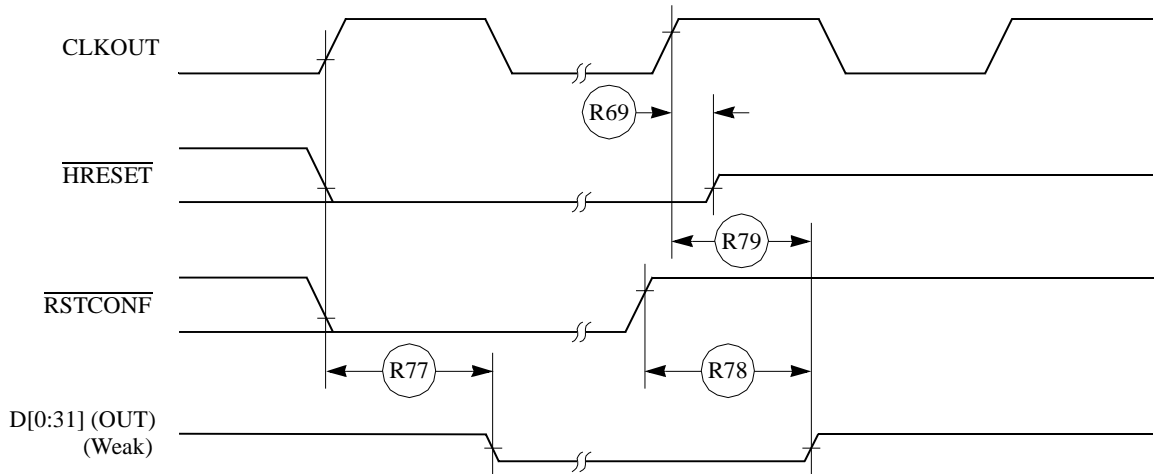


Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

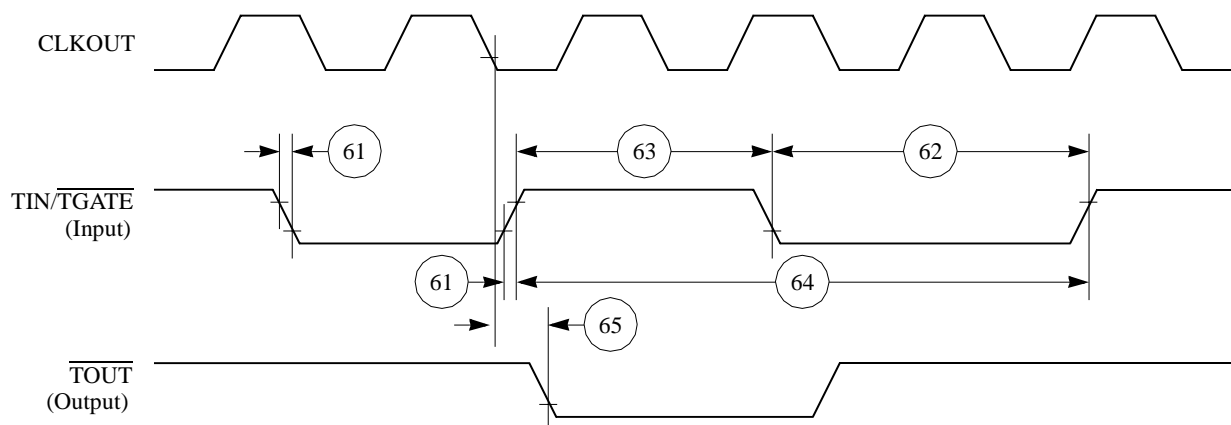


Figure 44. CPM General-Purpose Timers Timing Diagram

## 8.5 Serial Interface AC Electrical Specifications

Table 17 provides the serial interface timings as shown in Figure 45 to Figure 49.

Table 17. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) <sup>1, 2</sup>	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) <sup>2</sup>	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) <sup>3</sup>	P + 10	—	ns
72	L1TXD, L1ST <sub>n</sub> , L1RQ, L1xCLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1xCLK edge Edge (SYNC setup time)	20.00	—	ns
74	L1xCLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1xCLK edge (L1RXD setup time)	17.00	—	ns
77	L1xCLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1xCLK edge to L1ST <sub>n</sub> valid <sup>4</sup>	10.00	45.00	ns
78A	L1SYNC valid to L1ST <sub>n</sub> valid	10.00	45.00	ns
79	L1xCLK edge to L1ST <sub>n</sub> invalid	10.00	45.00	ns
80	L1xCLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid <sup>4</sup>	10.00	55.00	ns
81	L1xCLK edge to L1TXD high impedance	0.00	42.00	ns

Figure 50 through Figure 52 show the NMSI timings.

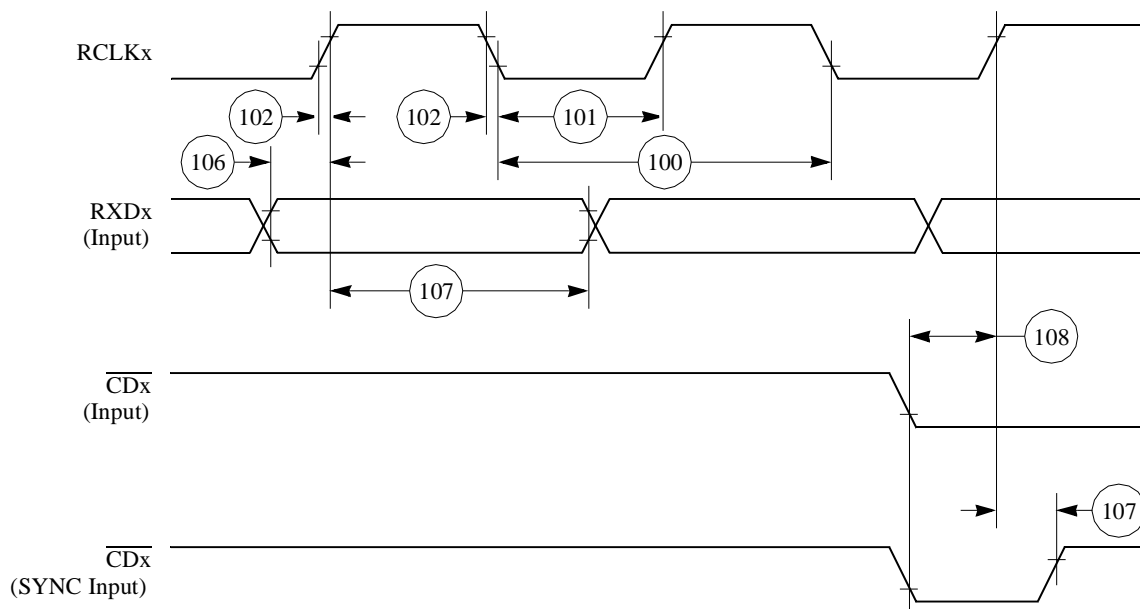


Figure 50. SCC NMSI Receive Timing Diagram

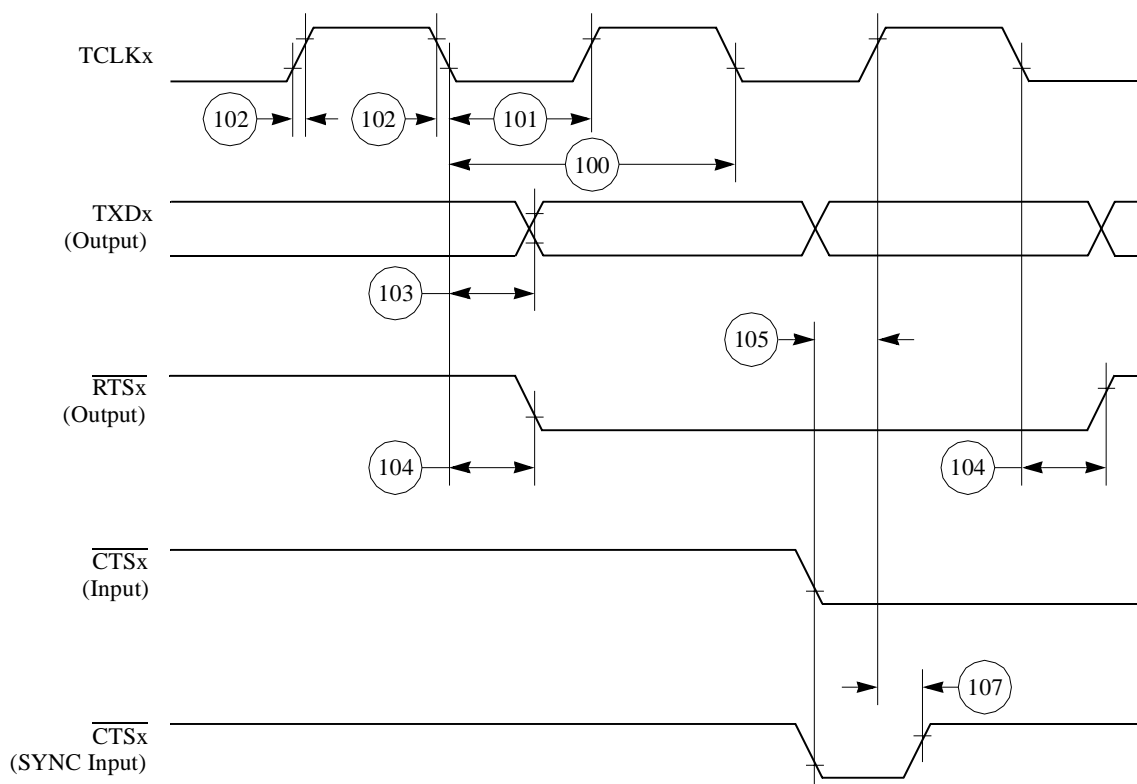
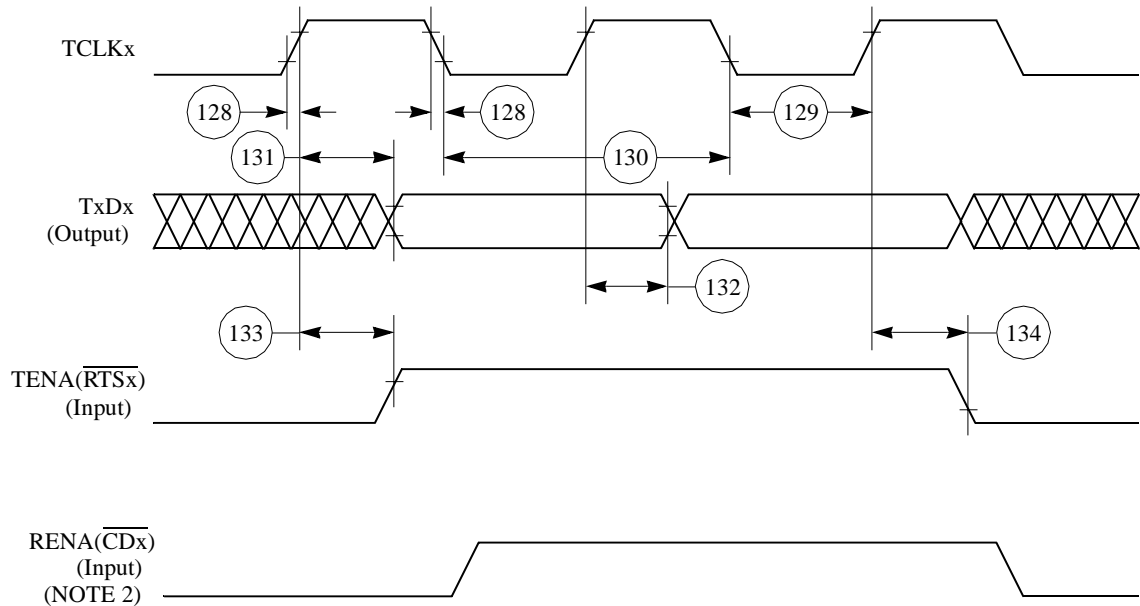


Figure 51. SCC NMSI Transmit Timing Diagram



- NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
  2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 55. Ethernet Transmit Timing Diagram

## 8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

Table 21. Serial Management Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLKx clock period <sup>1</sup>	100.00	—	ns
151	SMCLKx width low	50.00	—	ns
151a	SMCLKx width high	50.00	—	ns
152	SMCLKx rise/fall time	—	15.00	ns
153	SMTXDx active delay (from SMCLKx falling edge)	10.00	50.00	ns
154	SMRXDx/SMSYNx setup time	20.00	—	ns
155	SMRXDx/SMSYNx hold time	5.00	—	ns

<sup>1</sup> The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.



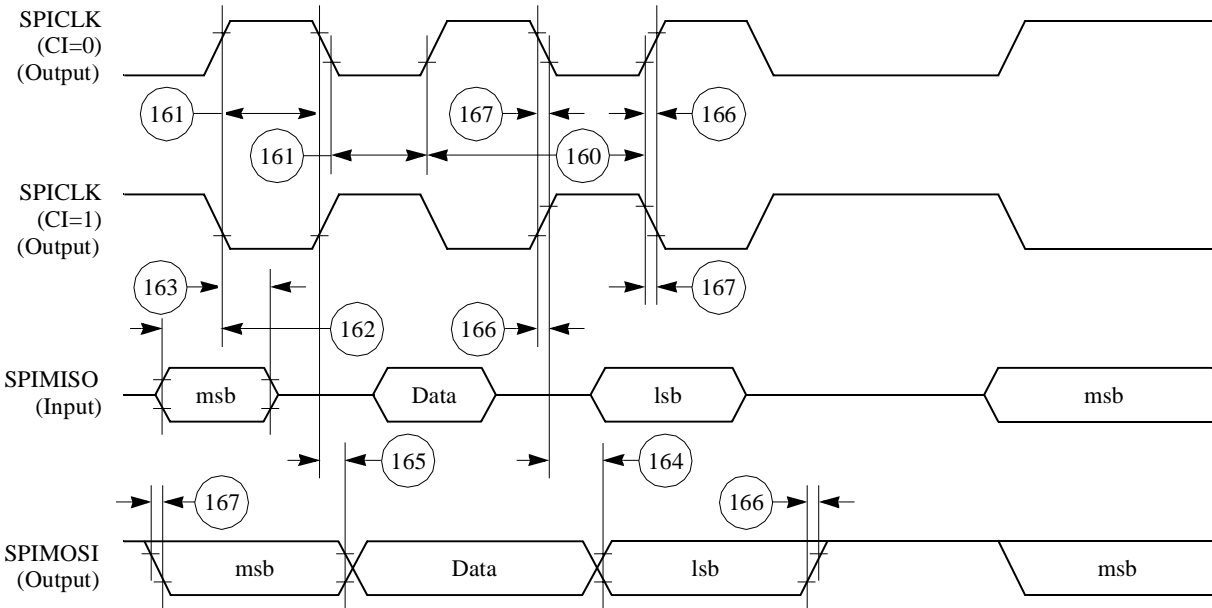


Figure 57. SPI Master (CP = 0) Timing Diagram

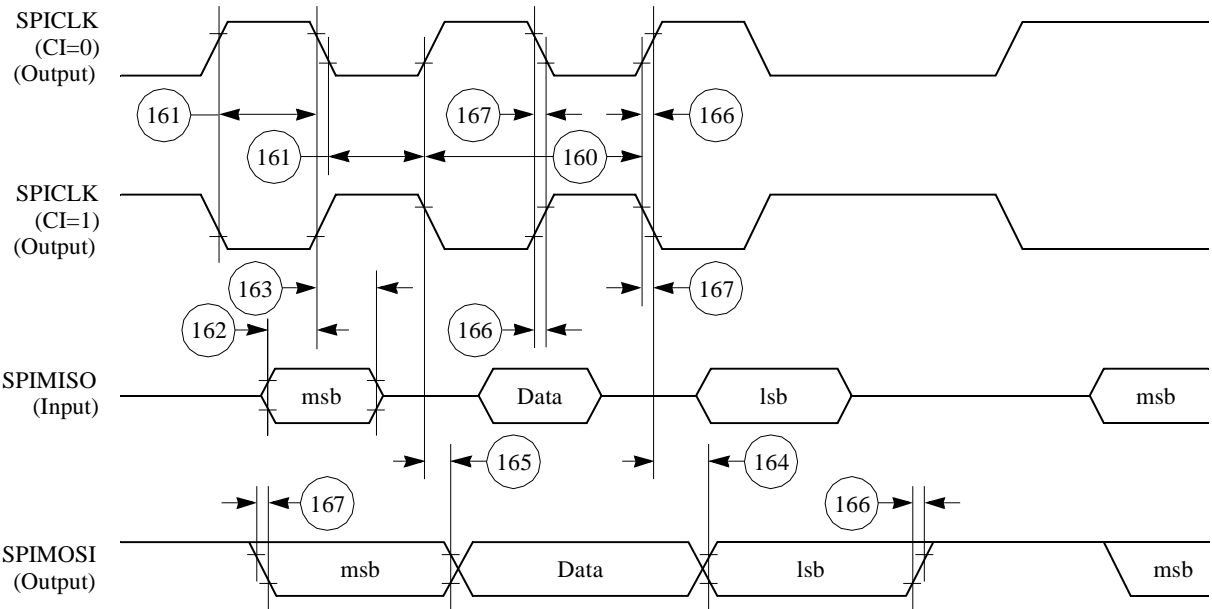


Figure 58. SPI Master (CP = 1) Timing Diagram

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

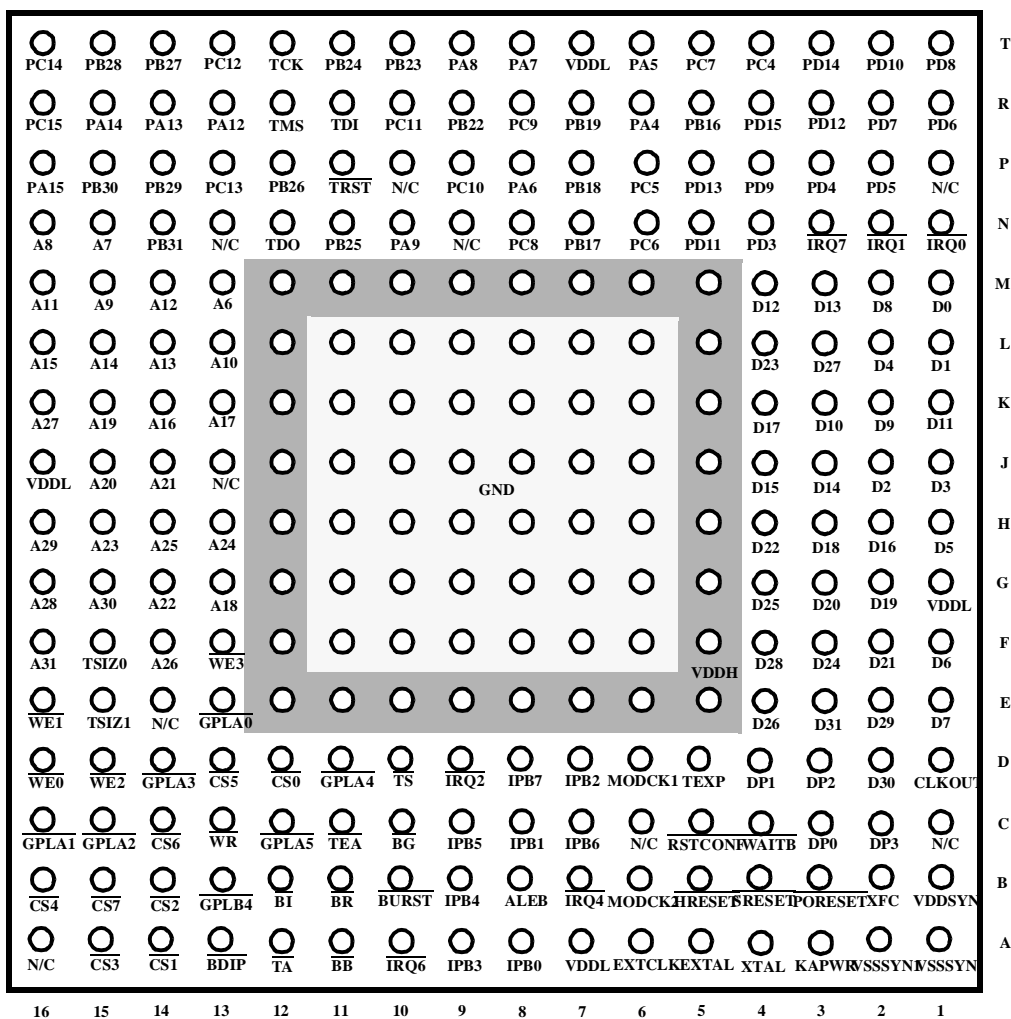


Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

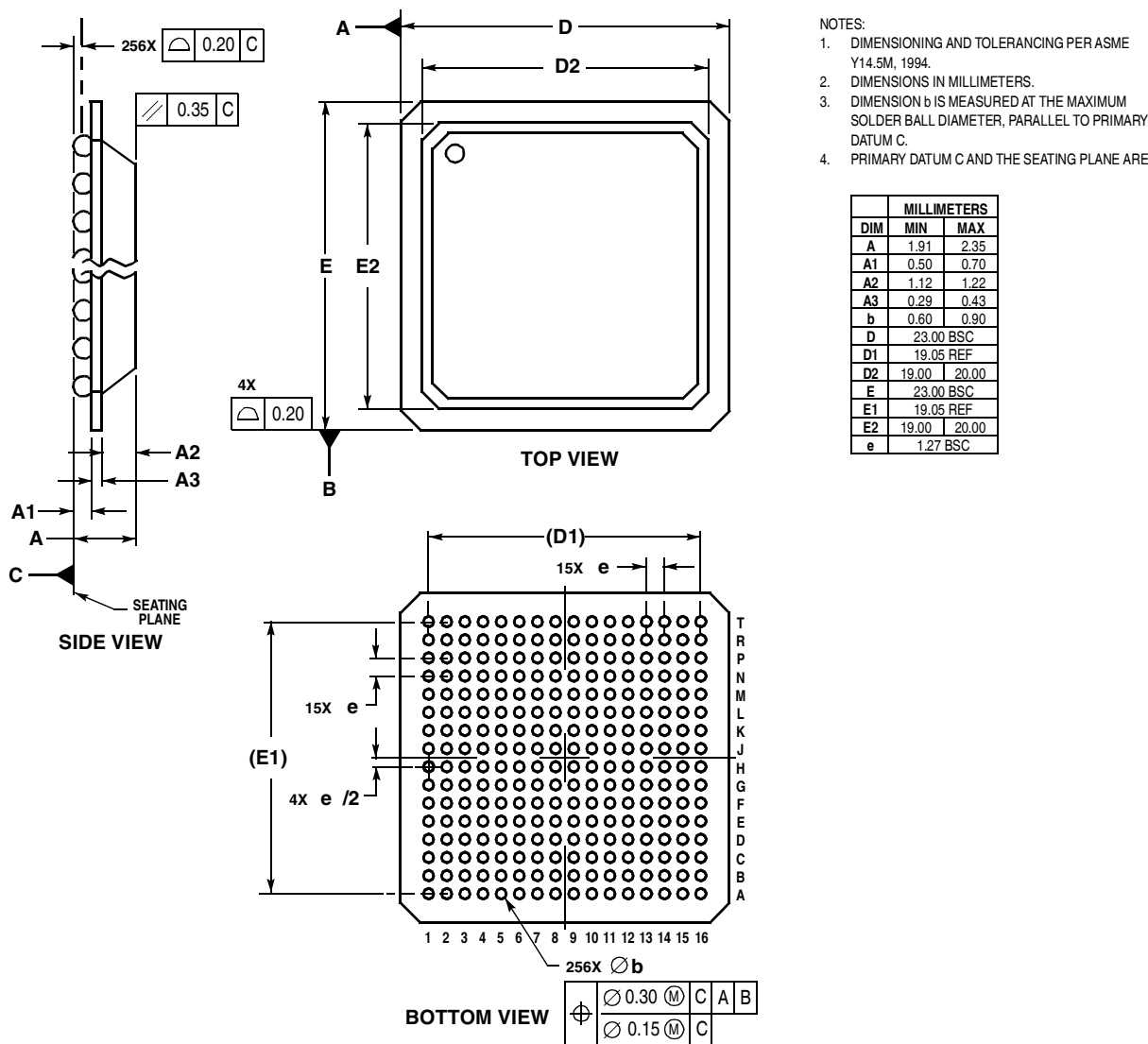


Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard

# 10 Document Revision History

Table 28 lists significant changes between revisions of this document.

**Table 28. Document Revision History**

Revision	Date	Change
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.
0.2	04/2002	Updated power numbers and added Rev. C
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.



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