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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	·
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850devr50bur2

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



NP,

2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:



Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
 - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution



Num	Characteristic	50 I	MHz	66 I	MHz	80 MHz		FFACT	FFACT	Cap Load	Unit
Num	Characteristic	Min	Max	Min	Мах	Min	Мах		50 pF)	Omt	
B42	CLKOUT rising edge to \overline{TS} valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns	
B43	AS negation to memory controller signals negation	—	TBD	—	TBD	TBD	—	—	50.00	ns	

 Table 6. Bus Operation Timing ¹ (continued)

The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters: For minima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR)$$

For maxima:

$$D = \frac{FFACTOR \times 1000}{F} + \frac{(D_{50} - 20 \times FFACTOR)}{F} + \frac{1ns(CAP \text{ LOAD} - 50) / 10}{F}$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

D₅₀ is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

- ² Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.
- ³ If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.
- ⁴ The timing for BR output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for BG output is relevant when the MPC850 is selected to work with internal bus arbiter.
- ⁵ The setup times required for TA, TEA, and BI are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).
- ⁶ The timing required for BR input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for BG input is relevant when the MPC850 is selected to work with the external bus arbiter.
- ⁷ The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the TA input signal is asserted.
- ⁸ The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.
- ⁹ The timing B30 refers to \overline{CS} when ACS = '00' and to $\overline{WE[0:3]}$ when CSNT = '0'.
- ¹⁰ The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.
- ¹¹ The $\overline{\text{AS}}$ signal is considered asynchronous to CLKOUT.



Bus Signal Timing

Figure 4 provides the timing for the synchronous output signals.



Figure 4. Synchronous Output Signals Timing

Figure 5 provides the timing for the synchronous active pull-up and open-drain output signals.



Figure 5. Synchronous Active Pullup and Open-Drain Outputs Signals Timing



Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.



Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)



Bus Signal Timing



Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)







Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)



Bus Signal Timing



Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.





Figure 21 provides the timing for the asynchronous external master control signals negation.



Figure 21. Asynchronous External Master—Control Signals Negation Timing



Table 7 provides interrupt timing for the MPC850.

Num	Characteristic ¹		50 MHz		66MHz		80 MHz	
Num			Max	Min	Max	Min	Max	Unit
139	IRQx valid to CLKOUT rising edge (set up time)	6.00		6.00		6.00		ns
140	IRQx hold time after CLKOUT.	2.00	_	2.00	_	2.00	_	ns
141	IRQx pulse width low	3.00	_	3.00	_	3.00	_	ns
142	IRQx pulse width high	3.00	_	3.00	_	3.00	_	ns
143	IRQx edge-to-edge time	80.00	_	121.0	_	100.0	_	ns

 Table 7. Interrupt Timing

¹ The timings I39 and I40 describe the testing conditions under which the IRQ lines are tested when being defined as level sensitive. The IRQ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the IRQ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.



Figure 22. Interrupt Detection Timing for External Level Sensitive Lines

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.



Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines





Figure 24 provides the PCMCIA access cycle timing for the external bus read.

Figure 24. PCMCIA Access Cycles Timing External Bus Read



IEEE 1149.1 Electrical Specifications



Figure 34. JTAG Test Clock Input Timing



Figure 35. JTAG Test Access Port Timing Diagram



Figure 36. JTAG TRST Timing Diagram



CPM Electrical Characteristics



Figure 41. SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock







8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequ	Unit	
		Min	Мах	onne
50	BRGO rise and fall time	_	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns



Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Num	Charactoristic	All Frequ	Unit		
Num	Characteristic	Min	Мах	onit	
61	TIN/TGATE rise and fall time	10.00	_	ns	
62	TIN/TGATE low time	1.00	_	clk	
63	TIN/TGATE high time	2.00	—	clk	
64	TIN/TGATE cycle time	3.00	—	clk	
65	CLKO high to TOUT valid	3.00	25.00	ns	

Table 16. Timer Timing



CPM Electrical Characteristics



Figure 44. CPM General-Purpose Timers Timing Diagram

8.5 Serial Interface AC Electrical Specifications

Table 17 provides the serial interface timings as shown in Figure 45 to Figure 49.

Num	Characteristic	All Free	Unit	
Nulli	Characteristic	Min	Мах	Unit
70	L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2}	—	SYNCCLK/2. 5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) 2	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) 3	P + 10	—	ns
72	L1TXD, L1ST <i>n</i> , L1RQ, L1xCLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1xCLK edge Edge (SYNC setup time)	20.00	_	ns
74	L1xCLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	_	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1xCLK edge (L1RXD setup time)	17.00	—	ns
77	L1xCLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1xCLK edge to L1ST <i>n</i> valid ⁴	10.00	45.00	ns
78A	L1SYNC valid to L1ST <i>n</i> valid	10.00	45.00	ns
79	L1xCLK edge to L1ST <i>n</i> invalid	10.00	45.00	ns
80	L1xCLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid ⁴	10.00	55.00	ns
81	L1xCLK edge to L1TXD high impedance	0.00	42.00	ns

Table 17. SI Timing

Table 17. SI Timing (continued)						
	All Frequencies					
NUM	Characteristic	Min	Мах	Unit		
82	L1RCLK, L1TCLK frequency (DSC =1)	_	16.00 or SYNCCLK/2	MHz		
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns		
83A	L1RCLK, L1TCLK width high (DSC = 1) ³	P + 10	—	ns		
84	L1CLK edge to L1CLKO valid (DSC = 1)		30.00	ns		
85	L1RQ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCLK		
86	L1GR setup time ²	42.00	—	ns		
87	L1GR hold time	42.00	—	ns		
88	L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	_	0.00	ns		

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

- 2 These specs are valid for IDL mode only.
- ³ Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.







CPM Electrical Characteristics

Figure 50 through Figure 52 show the NMSI timings.





CPM Electrical Characteristics



Figure 60. SPI Slave (CP = 1) Timing Diagram

8.11 I²C AC Electrical Specifications

Table 24 provides the I^2C (SCL < 100 KHz) timings.

Table 24.	I ² C Timing	(SCL < 100 KHz)
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Num	Characteristic	All Frequ	Unit	
Num		Min	Max	onit
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) ¹	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	_	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	_	ns
209	SDL/SCL rise time	_	1.00	μs



9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivativ

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

 Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support



Figure 65 shows the JEDEC package dimensions of the PBGA.



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. DIMENSIONS IN MILLIMETERS.
- DIMENSION & IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
- 4. PRIMARY DATUM C AND THE SEATING PLANE ARE

	MILLIMETERS	
DIM	MIN	MAX
Α	1.91	2.35
A1	0.50	0.70
A2	1.12	1.22
A3	0.29	0.43
b	0.60	0.90
D	23.00 BSC	
D1	19.05 REF	
D2	19.00	20.00
Е	23.00 BSC	
E1	19.05 REF	
E2	19.00	20.00
е	1.27 BSC	

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Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard



Document Revision History

10 Document Revision History

Table 28 lists significant changes between revisions of this document.

Table 28. Document Revision History

Revision	Date	Change	
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.	
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.	
0.2	04/2002	Updated power numbers and added Rev. C	
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.	



Document Revision History

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