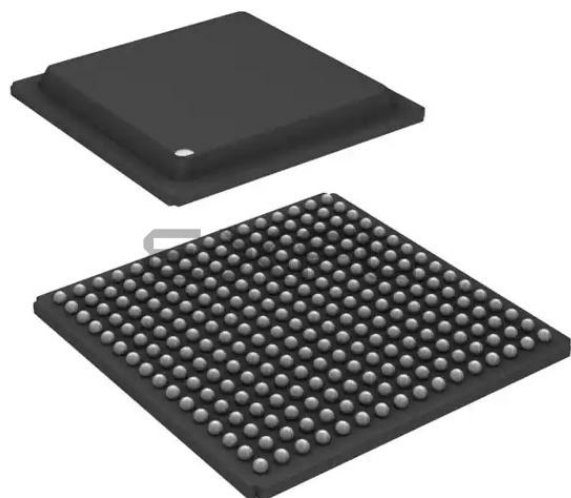




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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850devr66bu

- QUICC multichannel controller (QMC) microcode features
 - Up to 64 independent communication channels on a single SCC
 - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
 - Supports either transparent or HDLC protocols for each channel
 - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
 - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
 - UART
 - Transparent
 - General circuit interface (GCI) controller
 - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C[®] (interprocessor-integrated circuit) port
 - Supports master and slave modes
 - Supports multimaster environment
- Time slot assigner
 - Allows SCCs and SMCs to run in multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame syncs, clocking
 - Allows dynamic changes
 - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
 - Full high: all units fully powered at high clock frequency
 - Full low: all units fully powered at low clock frequency
 - Doze: core functional units disabled except time base, decremter, PLL, memory controller, real-time clock, and CPM in low-power standby
 - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
 - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
 - Low-power stop: to provide lower power dissipation

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA ¹	θ_{JA}	40 ²	°C/W
	θ_{JA}	31 ³	°C/W
	θ_{JA}	24 ⁴	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

¹ For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

² Assumes natural convection and a single layer board (no thermal vias).

³ Assumes natural convection, a multilayer board with thermal vias⁴, 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

⁴ Assumes natural convection, a multilayer board with thermal vias⁴, 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

$$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical ¹	Maximum ²	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

¹ Typical power dissipation is measured at 3.3V

² Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

Table 6. Bus Operation Timing ¹

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B1	CLKOUT period	20	—	30.30	—	25	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	—	50.00	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	—	50.00	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) ²	-0.60	0.60	-0.60	0.60	-0.60	0.60	—	50.00	ns
B1d	CLKOUT phase jitter ²	-2.00	2.00	-2.00	2.00	-2.00	2.00	—	50.00	ns
B1e	CLKOUT frequency jitter (MF < 10) ²	—	0.50	—	0.50	—	0.50	—	50.00	%
B1f	CLKOUT frequency jitter (10 < MF < 500) ²	—	2.00	—	2.00	—	2.00	—	50.00	%
B1g	CLKOUT frequency jitter (MF > 500) ²	—	3.00	—	3.00	—	3.00	—	50.00	%
B1h	Frequency jitter on EXTCLK ³	—	0.50	—	0.50	—	0.50	—	50.00	%
B2	CLKOUT pulse width low	8.00	—	12.12	—	10.00	—	—	50.00	ns
B3	CLKOUT width high	8.00	—	12.12	—	10.00	—	—	50.00	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	50.00	ns
B7	CLKOUT to A[6–31], RD $\overline{\text{WR}}$, BURST, D[0–31], DP[0–3] invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3], BDIP, PTR invalid	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS[0–1], VF[0–2] IWP[0–2], LWP[0–1], STS invalid ⁴	5.00	—	7.58	—	6.25	—	0.250	50.00	ns
B8	CLKOUT to A[6–31], RD $\overline{\text{WR}}$, BURST, D[0–31], DP[0–3] valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3] BDIP, PTR valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8b	CLKOUT to BR, BG, VFLS[0–1], VF[0–2], IWP[0–2], FRZ, LWP[0–1], STS valid ⁴	5.00	11.74	7.58	14.33	6.25	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0,1	—	8.00	—	8.00	—	8.00	—	50.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	—	50.00	ns
B24	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0.	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B24a	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B25	CLKOUT rising edge to $\overline{OE}$, WE[0–3] asserted	—	9.00	—	9.00	—	9.00	—	50.00	ns
B26	CLKOUT rising edge to $\overline{OE}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	—	50.00	ns
B27	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1	23.00	—	36.00	—	29.00	—	1.250	50.00	ns
B27a	A[6–31] to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B28	CLKOUT rising edge to WE[0–3] negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	50.00	ns
B28a	CLKOUT falling edge to WE[0–3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	—	12.00	—	14.00	—	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B33a	CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B34	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B34a	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B34b	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B35	A[6–31] to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B35a	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by BST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B35b	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B36	A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B37	UPWAIT valid to CLKOUT falling edge ¹⁰	6.00	—	6.00	—	6.00	—	—	50.00	ns
B38	CLKOUT falling edge to UPGATE valid ¹⁰	1.00	—	1.00	—	1.00	—	—	50.00	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge ¹¹	7.00	—	7.00	—	7.00	—	—	50.00	ns
B40	A[6–31], TSIZ[0–1], RD/ $\overline{WR}$, BURST, valid to CLKOUT rising edge.	7.00	—	7.00	—	7.00	—	—	50.00	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	—	50.00	ns

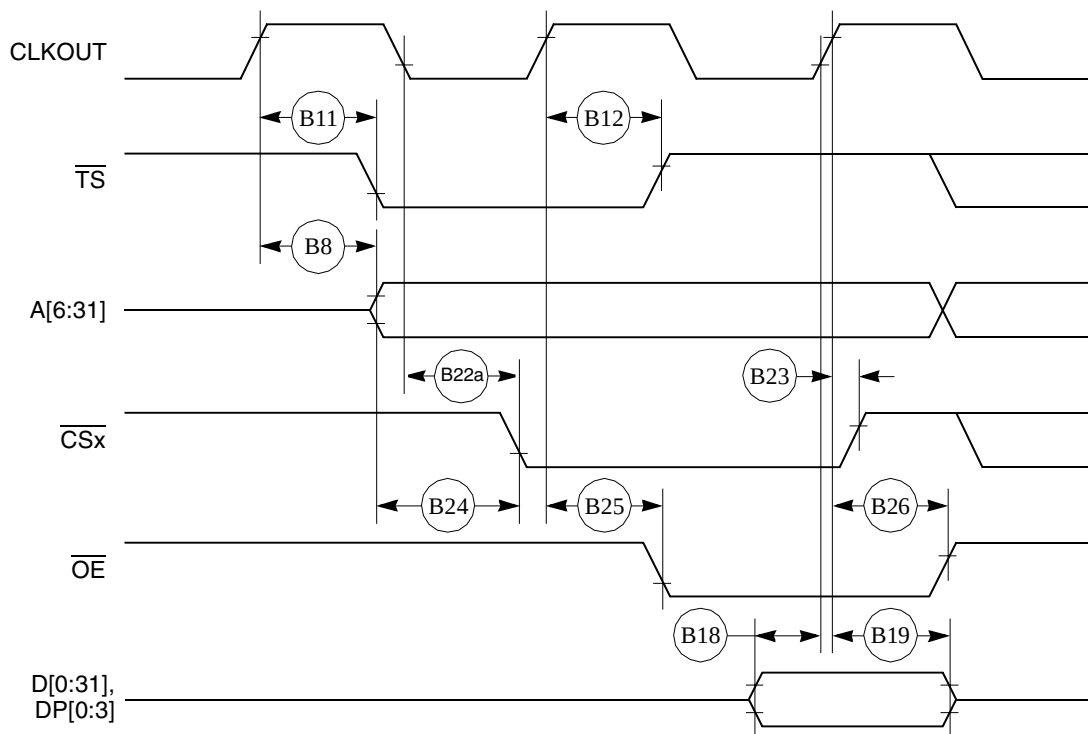


Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

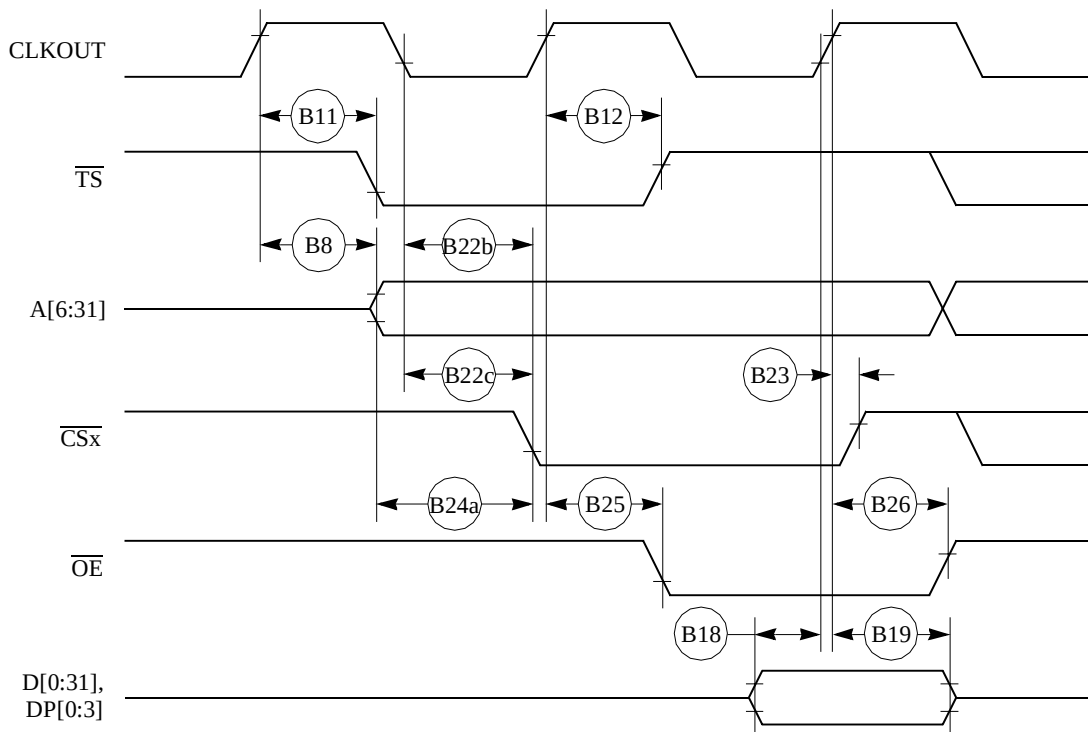


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

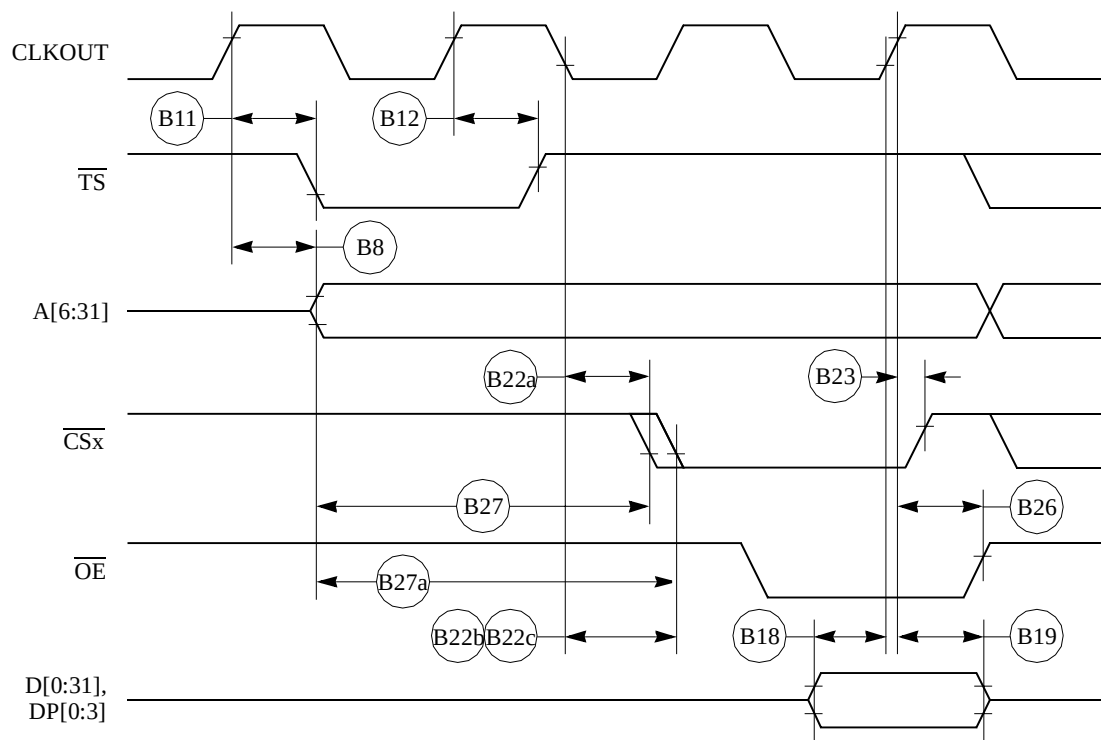


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 16 provides the timing for the external bus controlled by the UPM.

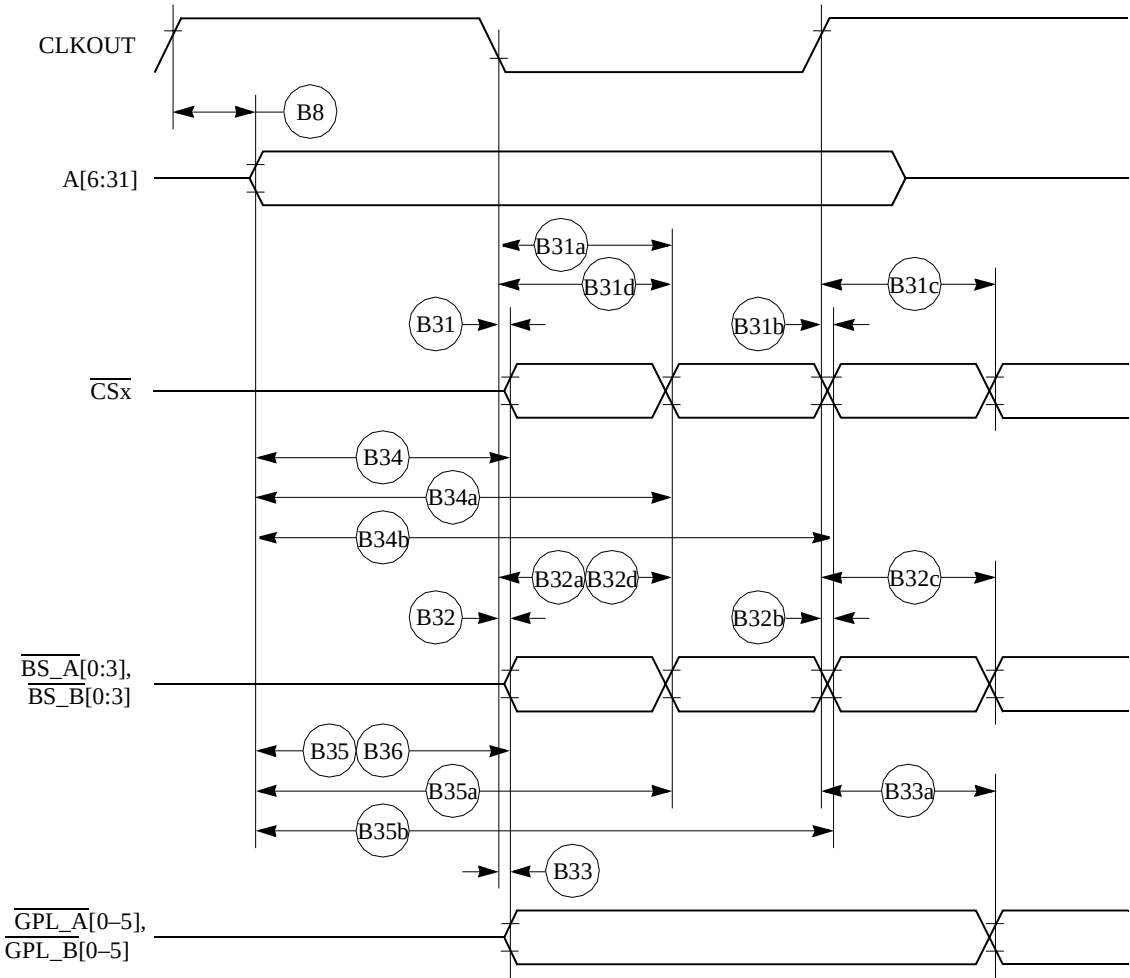


Figure 16. External Bus Timing (UPM Controlled Signals)

Table 7 provides interrupt timing for the MPC850.

Table 7. Interrupt Timing

Num	Characteristic ¹	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
I39	$\overline{\text{IRQx}}$ valid to CLKOUT rising edge (set up time)	6.00	—	6.00	—	6.00	—	ns
I40	$\overline{\text{IRQx}}$ hold time after CLKOUT.	2.00	—	2.00	—	2.00	—	ns
I41	$\overline{\text{IRQx}}$ pulse width low	3.00	—	3.00	—	3.00	—	ns
I42	$\overline{\text{IRQx}}$ pulse width high	3.00	—	3.00	—	3.00	—	ns
I43	$\overline{\text{IRQx}}$ edge-to-edge time	80.00	—	121.0	—	100.0	—	ns

¹ The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.

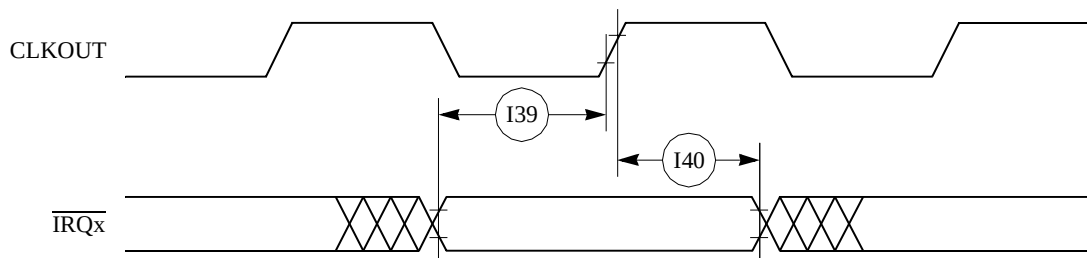


Figure 22. Interrupt Detection Timing for External Level Sensitive Lines

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.

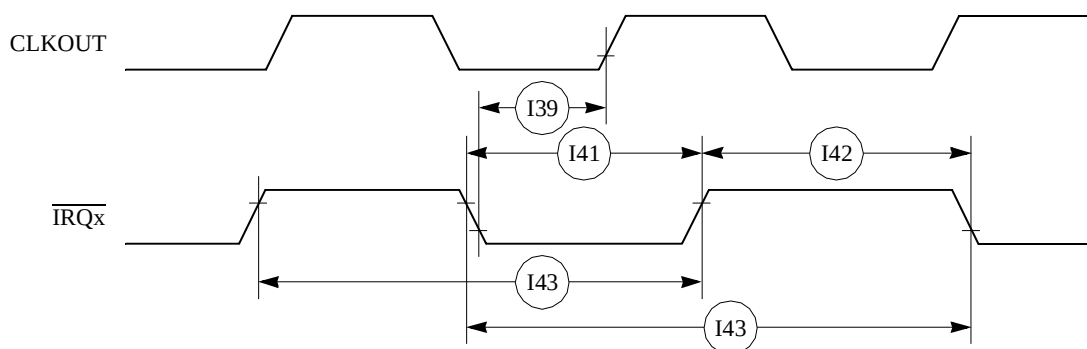


Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines

Table 8 shows the PCMCIA timing for the MPC850.

Table 8. PCMCIA Timing

Num	Characteristic	50MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
P44	A[6–31], $\overline{\text{REG}}$ valid to PCMCIA strobe asserted. ¹	13.00	—	21.00	—	17.00	—	0.750	ns
P45	A[6–31], $\overline{\text{REG}}$ valid to ALE negation. ¹	18.00	—	28.00	—	23.00	—	1.000	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid.	6.00	—	9.00	—	7.00	—	0.250	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time.	—	11.00	—	11.00	—	11.00	—	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time.	2.00	11.00	2.00	11.00	2.00	11.00	—	ns
P52	CLKOUT to ALE assert time	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P53	CLKOUT to ALE negate time	—	13.00	—	16.00	—	14.00	0.250	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D[0–31] invalid. ¹	3.00	—	6.00	—	4.00	—	0.250	ns
P55	$\overline{\text{WAIT_B}}$ valid to CLKOUT rising edge. ¹	8.00	—	8.00	—	8.00	—	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAIT_B}}$ invalid. ¹	2.00	—	2.00	—	2.00	—	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAIT_B}}$ signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAIT_B}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC850 PowerQUICC User's Manual.

Figure 31 shows the reset timing for the data bus configuration.

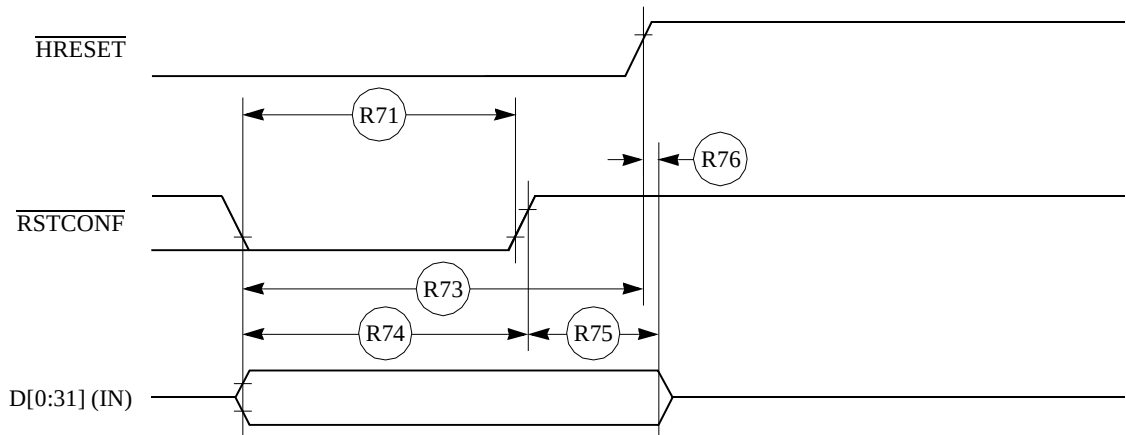


Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

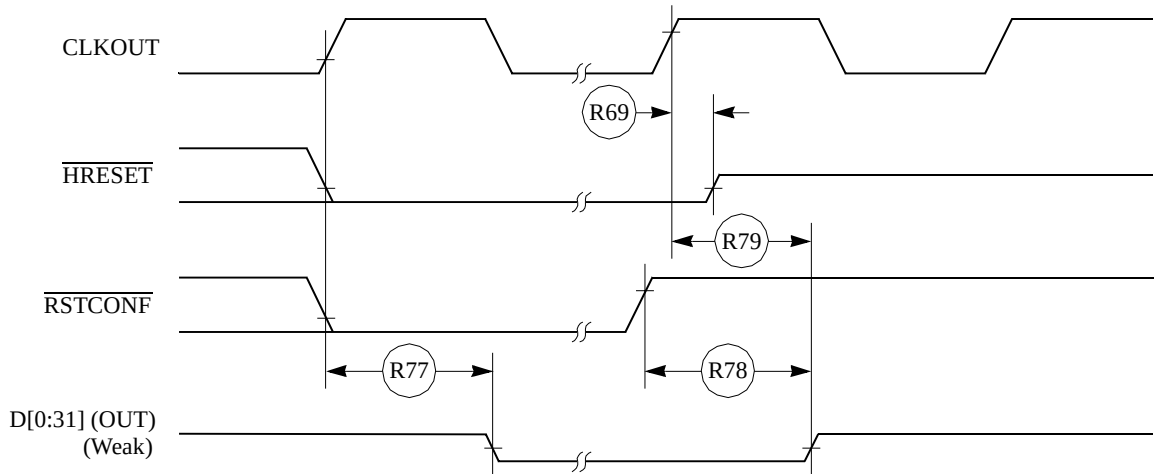


Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

Figure 33 provides the reset timing for the debug port configuration.

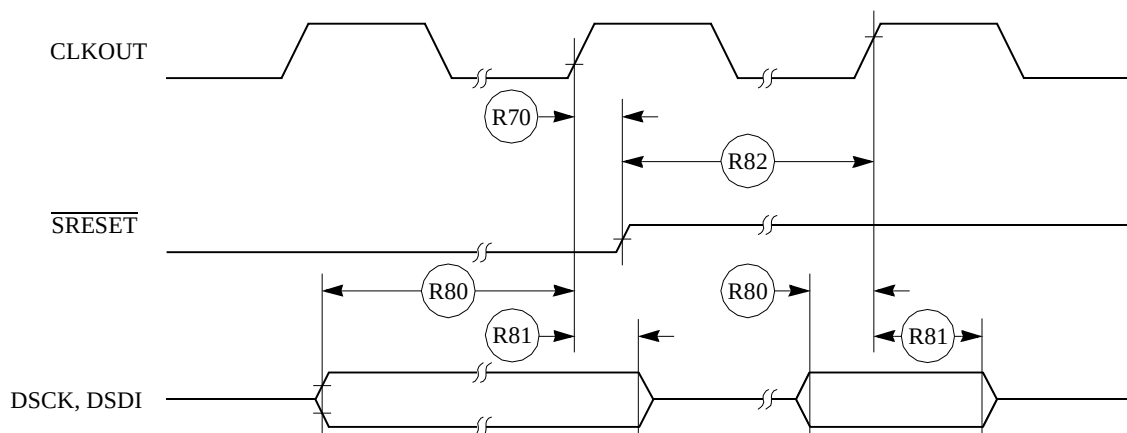


Figure 33. Reset Timing—Debug Port Configuration

7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

Table 12. JTAG Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
J82	TCK cycle time	100.00	—	100.00	—	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	40.00	—	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	5.00	—	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	25.00	—	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	—	27.00	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	0.00	—	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	—	20.00	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	100.00	—	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	40.00	—	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	—	50.00	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	—	50.00	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	—	50.00	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	50.00	—	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	50.00	—	50.00	—	ns

8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns

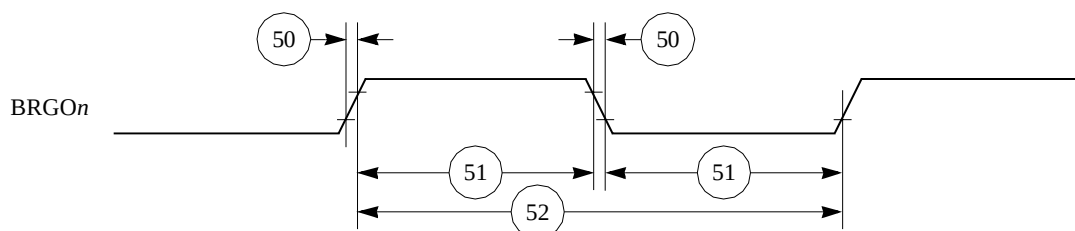


Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Table 16. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/TGATE rise and fall time	10.00	—	ns
62	TIN/TGATE low time	1.00	—	clk
63	TIN/TGATE high time	2.00	—	clk
64	TIN/TGATE cycle time	3.00	—	clk
65	CLKO high to TOUT valid	3.00	25.00	ns

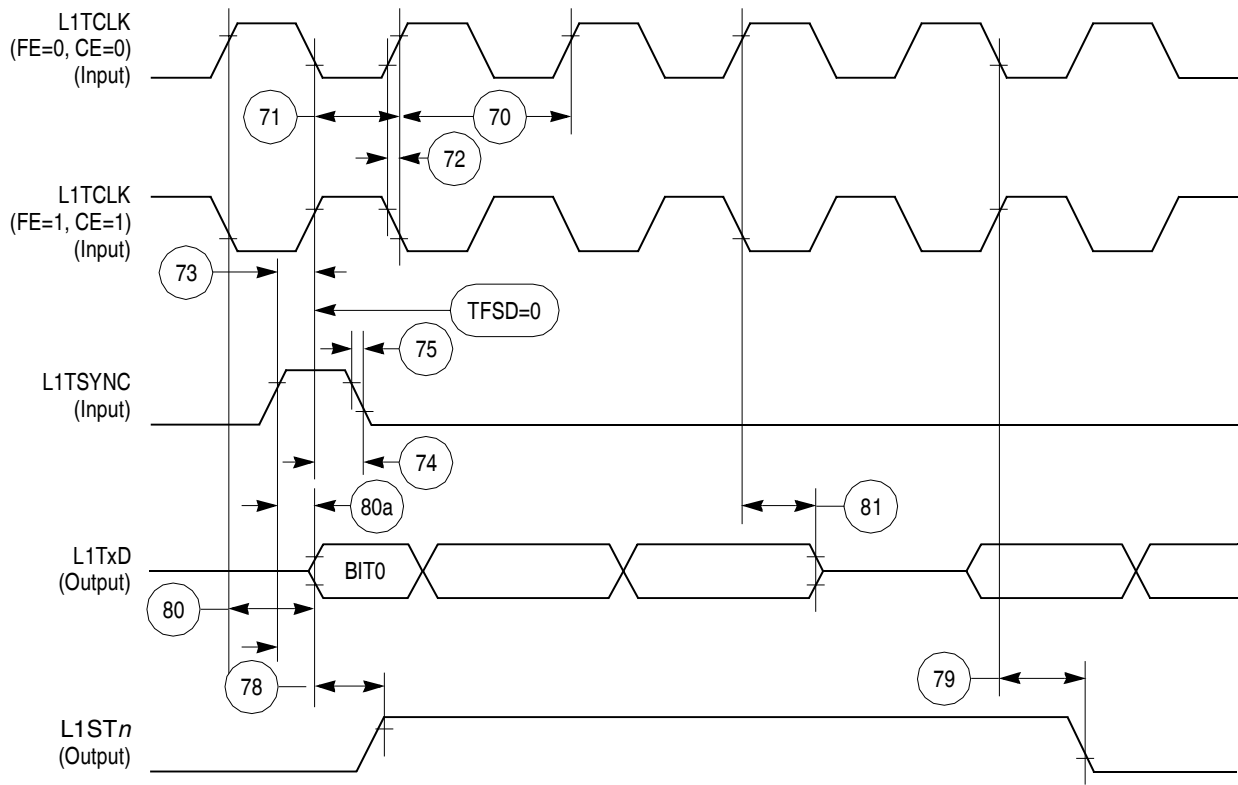


Figure 47. SI Transmit Timing Diagram

Figure 50 through Figure 52 show the NMSI timings.

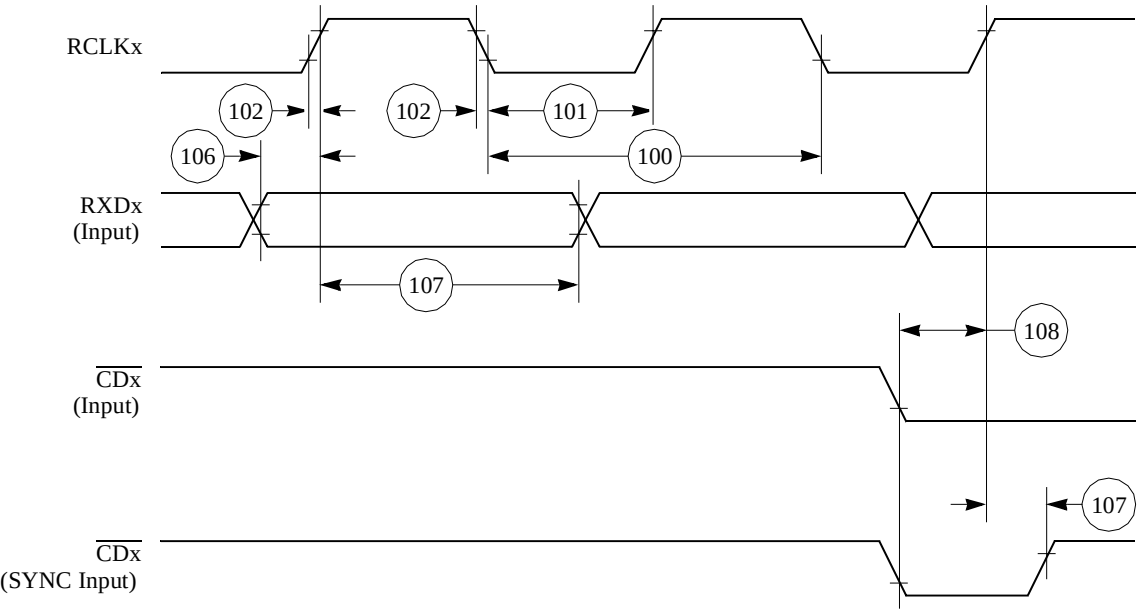


Figure 50. SCC NMSI Receive Timing Diagram

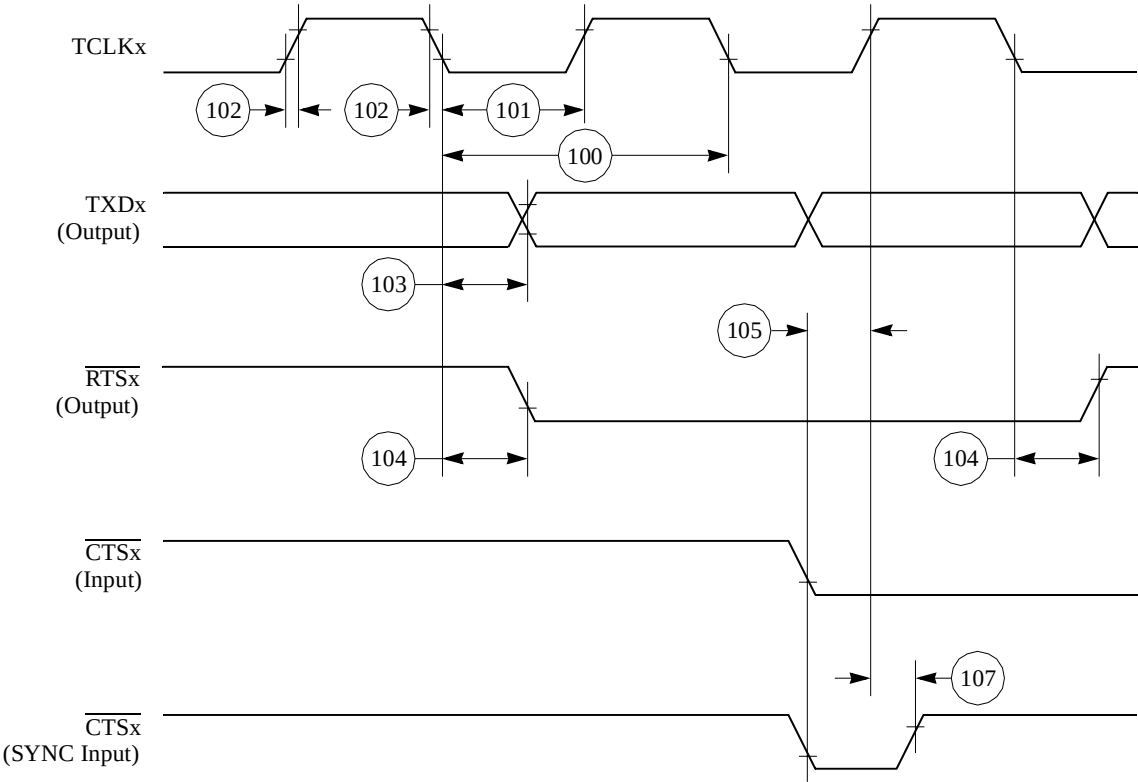


Figure 51. SCC NMSI Transmit Timing Diagram

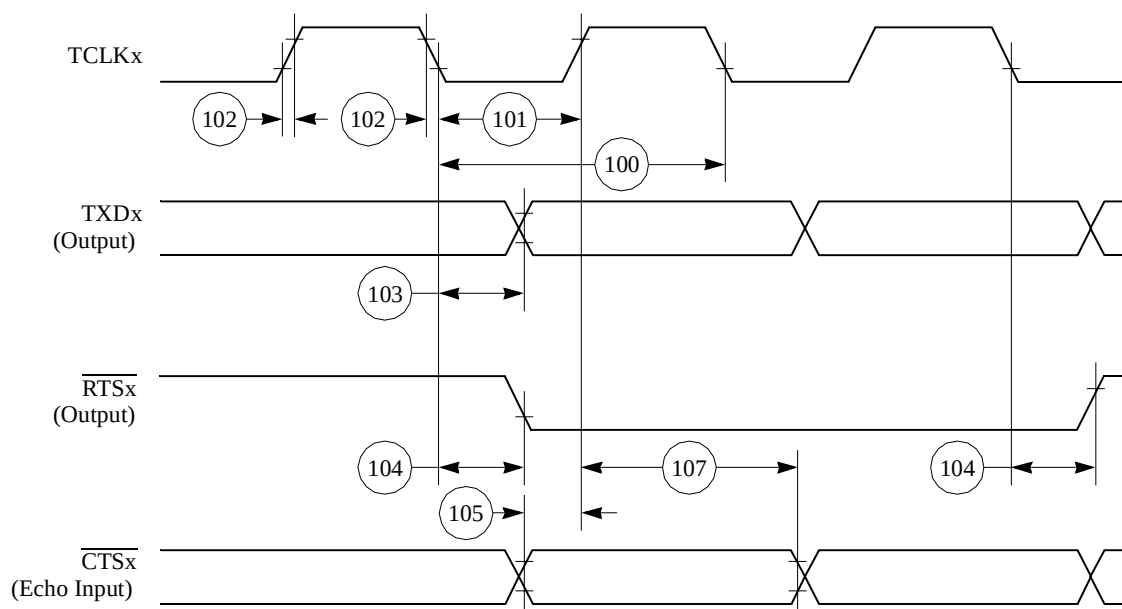


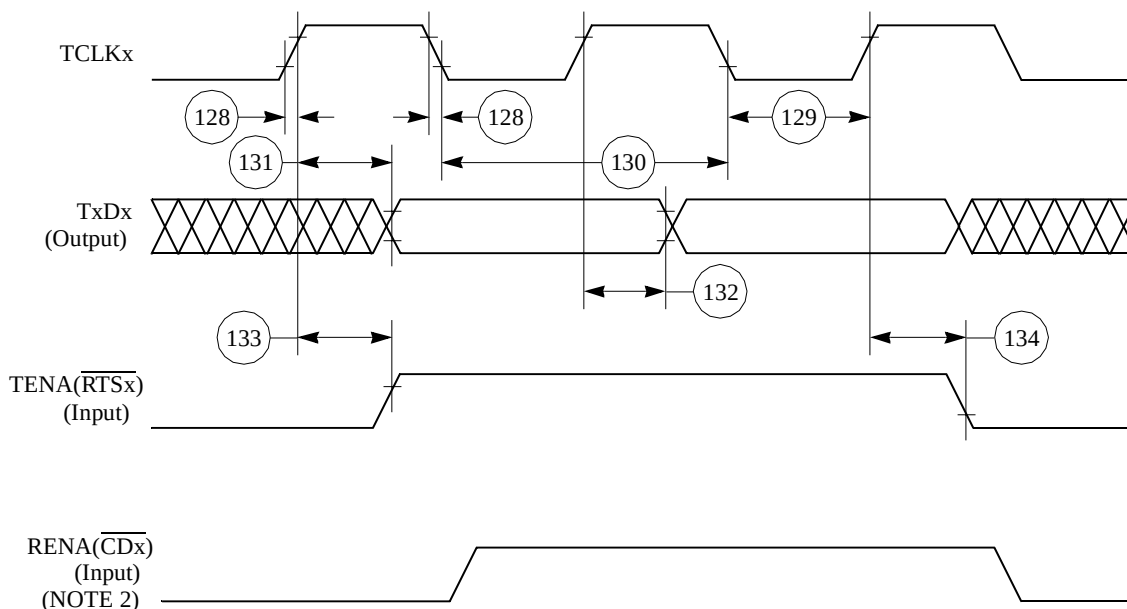
Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period ¹	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period ¹	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns



NOTES:

1. Transmit clock invert (TCI) bit in GSRM is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 55. Ethernet Transmit Timing Diagram

8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

Table 21. Serial Management Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLKx clock period ¹	100.00	—	ns
151	SMCLKx width low	50.00	—	ns
151a	SMCLKx width high	50.00	—	ns
152	SMCLKx rise/fall time	—	15.00	ns
153	SMTXDx active delay (from SMCLKx falling edge)	10.00	50.00	ns
154	SMRXDx/SMSYNx setup time	20.00	—	ns
155	SMRXDx/SMSYNx hold time	5.00	—	ns

¹ The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.

9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivatives

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.

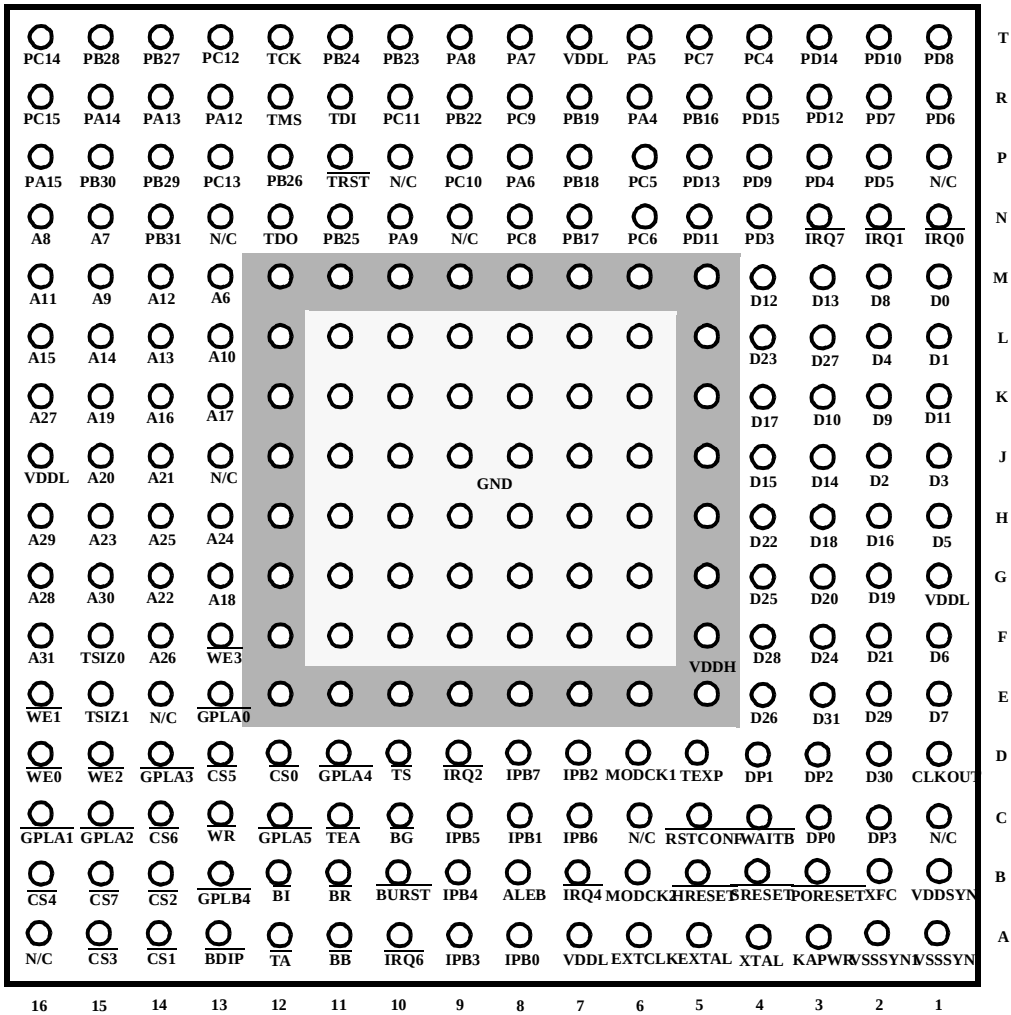


Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

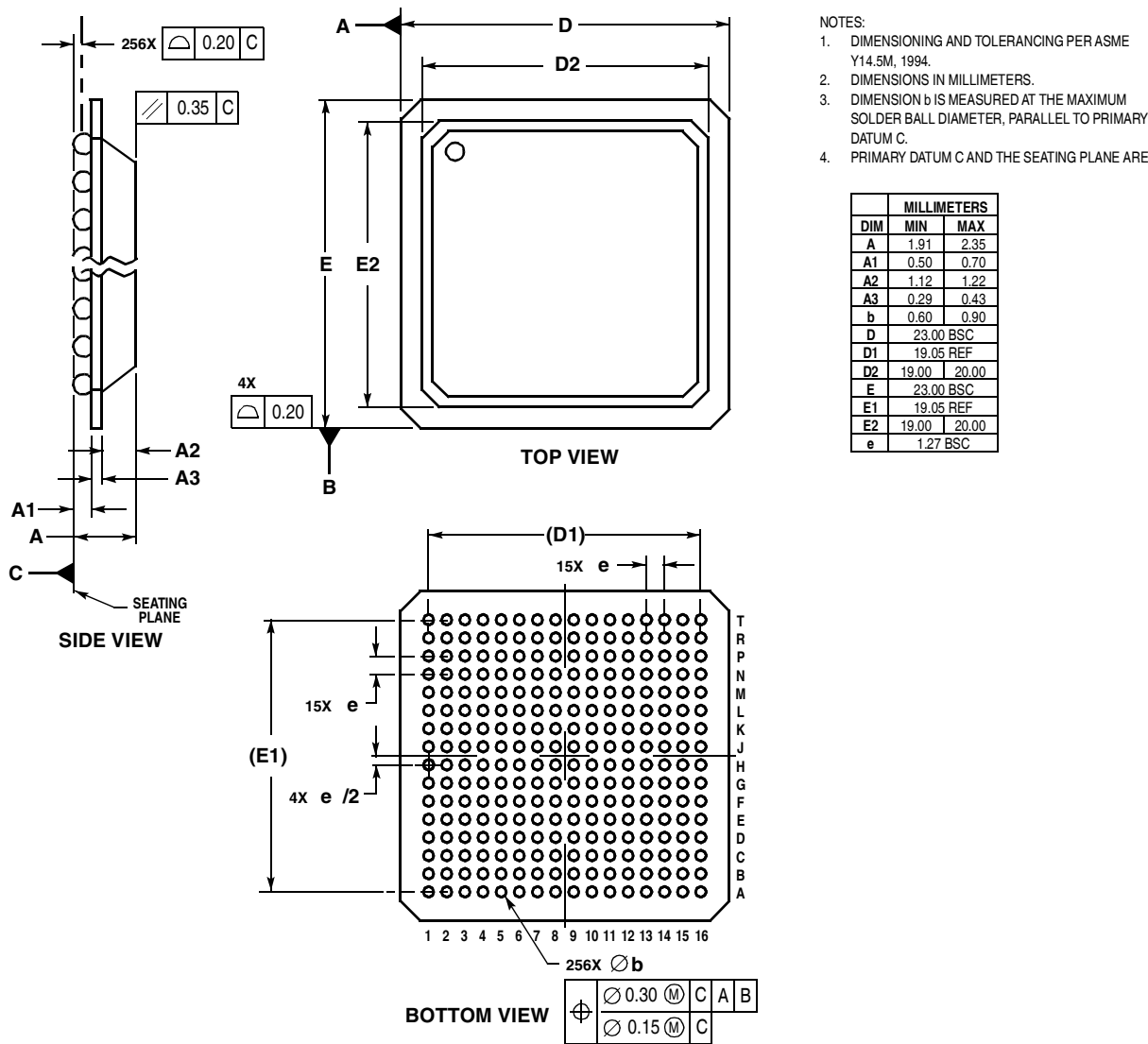


Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard