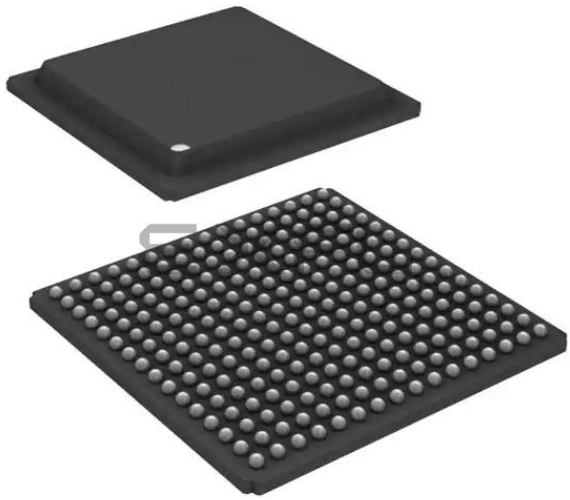

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850dezt66bu

  - 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
    - Caches are two-way, set-associative
    - Physically addressed
    - Cache blocks can be updated with a 4-word line burst
    - Least-recently used (LRU) replacement algorithm
    - Lockable one-line granularity
  - Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
  - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
  - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
  - Hardware bus monitor
  - Spurious interrupt monitor
  - Software watchdog
  - Periodic interrupt timer
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
  - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
  - Memory controller programmable to support most size and speed memory interfaces
  - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
  - Variable block sizes, 32 Kbytes to 256 Mbytes
  - Selectable write protection
  - On-chip bus arbiter supports one external bus master
  - Special features for burst mode support
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers

  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Eight external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - Fifteen internal interrupt sources
  - Programmable priority among SCCs and USB
  - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
  - Master (socket) interface, release 2.1 compliant
  - Single PCMCIA socket
  - Supports eight memory or I/O windows
- Communications processor module (CPM)
  - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
  - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8 Kbytes of dual-port RAM
  - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
  - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
  - Can be connected to any SCC, SMC, or USB
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communications controllers)
  - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
  - HDLC/SDLC™ (all channels supported at 2 Mbps)
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk®
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))

  - Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
  - Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - The MPC850 can compare using the =, ≠, <, and > conditions to generate watchpoints
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility on all general purpose I/O pins.

3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC850. Table 2 provides the maximum ratings.

Table 2. Maximum Ratings

(GND = 0V)

Rating	Symbol	Value	Unit
Supply voltage	VDDH	-0.3 to 4.0	V
	VDDL	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	VDDSYN	-0.3 to 4.0	V
Input voltage [1]	V_{in}	GND-0.3 to VDDH + 2.5 V	V
Junction temperature [2]	T_j	0 to 95 (standard) -40 to 95 (extended)	°C
Storage temperature range	T_{stg}	-55 to +150	°C

1 Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
CAUTION: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction applies to power-up and normal operation (that is, if the MPC850 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

2 The MPC850, a high-frequency device in a BGA package, does not provide a guaranteed maximum ambient temperature. Only maximum junction temperature is guaranteed. It is the responsibility of the user to consider power dissipation and thermal management. Junction temperature ratings are the same regardless of frequency rating of the device.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}). Table 3 provides the package thermal characteristics for the MPC850.

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input low voltage	VIL	GND	0.8	V
EXTAL, EXTCLK input high voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input leakage current, Vin = 5.5 V (Except TMS, TRST, DSCK and DSDI pins)	I_{in}	—	100	µA
Input leakage current, Vin = 3.6V (Except TMS, TRST, DSCK and DSDI pins)	I_{In}	—	10	µA
Input leakage current, Vin = 0V (Except TMS, TRST, DSCK and DSDI pins)	I_{In}	—	10	µA
Input capacitance	C_{in}	—	20	pF
Output high voltage, IOH = -2.0 mA, VDDH = 3.0V except XTAL, XFC, and open-drain pins	VOH	2.4	—	V
Output low voltage CLKOUT [3] IOL = 3.2 mA [1] IOL = 5.3 mA [2] IOL = 7.0 mA PA[14]/USBOE, PA[12]/TXD2 IOL = 8.9 mA TS, TA, TEA, BI, BB, HRESET, SRESET	VOL	—	0.5	V

1 A[6:31], TSIZ0/REG, TSIZ1, D[0:31], DP[0:3]/IRQ[3:6], RD/WR, BURST, RSV/IRQ2, IP_B[0:1]/IWP[0:1]/VFLS[0:1], IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, PA[15]/USBRXD, PA[13]/RXD2, PA[9]/L1TXDA/SMRXD2, PA[8]/L1RXDA/SMTXD2, PA[7]/CLK1/TIN1/L1RCLKA/BRGO1, PA[6]/CLK2/TOUT1/TIN3, PA[5]/CLK3/TIN2/L1TCLKA/BRGO2, PA[4]/CLK4/TOUT2/TIN4, PB[31]/SPISEL, PB[30]/SPICLK/TXD3, PB[29]/SPIMOSI /RXD3, PB[28]/SPIMISO/BRGO3, PB[27]/I2CSDA/BRGO1, PB[26]/I2CSCL/BRGO2, PB[25]/SMTXD1/TXD3, PB[24]/SMRXD1/RXD3, PB[23]/SMSYN1/SDACK1, PB[22]/SMSYN2/SDACK2, PB[19]/L1ST1, PB[18]/RTS2/L1ST2, PB[17]/L1ST3, PB[16]/L1RQa/L1ST4, PC[15]/DREQ0/L1ST5, PC[14]/DREQ1/RTS2/L1ST6, PC[13]/L1ST7/RTS3, PC[12]/L1RQa/L1ST8, PC[11]/USBRXP, PC[10]/TGATE1/USBRXN, PC[9]/CTS2, PC[8]/CD2/TGATE1, PC[7]/USBTXP, PC[6]/USBTXN, PC[5]/CTS3/L1TSYNCA/SDACK1, PC[4]/CD3/L1RSYNCA, PD[15], PD[14], PD[13], PD[12], PD[11], PD[10], PD[9], PD[8], PD[7], PD[6], PD[5], PD[4], PD[3]

2 BDIP/GPL_B5, BR, BG, FRZ/IRQ6, CS[0:5], CS6/CE1_B, CS7/CE2_B, WE0/BS_AB0/IORD, WE1/BS_AB1/IOWR, WE2/BS_AB2/PCOE, WE3/BS_AB3/PCWE, GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A[2:3]/GPL_B[2:3]/CS[2:3], UPWAITA/GPL_A4/AS, UPWAITB/GPL_B4, GPL_A5, ALE_B/DSCK/AT1, OP2/MODCK1/STS, OP3/MODCK2/DSDO

3 The MPC850 IBIS model must be used to accurately model the behavior of the Clkout output driver for the full and half drive setting. Due to the nature of the Clkout output buffer, IOH and IOL for Clkout should be extracted from the IBIS model at any output voltage level.

5 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the equation:

$T_J = T_A + (P_D \bullet \theta_{JA})(1)$

where

T_A = Ambient temperature, °C

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B29h	$\overline{WE}$[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B29i	$\overline{CS}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B30	$\overline{CS}$, $\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access [9]	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B30a	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A[6–31] invalid GPCM write access TRLX = 0, CSNT =1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B30b	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A[6–31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B30c	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	8.00	—	6.00	—	0.375	50.00	ns
B30d	$\overline{WE}$[0–3] negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B31	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid - as requested by control bit CST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	1.50	8.00	—	50.00	ns
B32c	CLKOUT rising edge to $\overline{BS}$ valid - as requested by control bit BST3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid - as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1	9.00	14.00	13.00	18.00	11.00	16.00	0.375	50.00	ns
B33	CLKOUT falling edge to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	1.50	6.00	—	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B33a	CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B34	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B34a	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by control bit CST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B34b	A[6–31] and D[0–31] to $\overline{CS}$ valid - as requested by CST2 in the corresponding word in UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B35	A[6–31] to $\overline{CS}$ valid - as requested by control bit BST4 in the corresponding word in UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B35a	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by BST1 in the corresponding word in the UPM	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B35b	A[6–31] and D[0–31] to $\overline{BS}$ valid - as requested by control bit BST2 in the corresponding word in the UPM	13.00	—	21.00	—	17.00	—	0.750	50.00	ns
B36	A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B37	UPWAIT valid to CLKOUT falling edge [10]	6.00	—	6.00	—	6.00	—	—	50.00	ns
B38	CLKOUT falling edge to UPWAIT valid [10]	1.00	—	1.00	—	1.00	—	—	50.00	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [11]	7.00	—	7.00	—	7.00	—	—	50.00	ns
B40	A[6–31], TSIZ[0–1], RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge.	7.00	—	7.00	—	7.00	—	—	50.00	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time)	7.00	—	7.00	—	7.00	—	—	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time)	2.00	—	2.00	—	2.00	—	—	50.00	ns
B43	$\overline{AS}$ negation to memory controller signals negation	—	TBD	—	TBD	TBD	—	—	50.00	ns

1 The minima provided assume a 0 pF load, whereas maxima assume a 50pF load. For frequencies not marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the FFactor column. AC parameters without an FFactor entry do not need to be calculated and can be taken directly from the frequency column corresponding to the frequency marked on the part. The following equations should be used in these calculations.

For a frequency F, the following equations should be applied to each one of the above parameters:

For minima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR)$$

For maxima:

$$D = \frac{FFACTOR \times 1000}{F} + (D_{50} - 20 \times FFACTOR) + 1ns(CAP\ LOAD - 50) / 10$$

where:

D is the parameter value to the frequency required in ns

F is the operation frequency in MHz

D_{50} is the parameter value defined for 50 MHz

CAP LOAD is the capacitance load on the signal in question.

FFACTOR is the one defined for each of the parameters in the table.

2 Phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed value.

3 If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2%.

4 The timing for $\overline{BR}$ output is relevant when the MPC850 is selected to work with external bus arbiter. The timing for $\overline{BG}$ output is relevant when the MPC850 is selected to work with internal bus arbiter.

5 The setup times required for $\overline{TA}$, $\overline{TEA}$, and $\overline{BI}$ are relevant only when they are supplied by an external device (and not when the memory controller or the PCMCIA interface drives them).

6 The timing required for $\overline{BR}$ input is relevant when the MPC850 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC850 is selected to work with the external bus arbiter.

7 The D[0–31] and DP[0–3] input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

8 The D[0:31] and DP[0:3] input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects controlled by the UPM in the memory controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

9 The timing B30 refers to $\overline{CS}$ when ACS = '00' and to $\overline{WE[0:3]}$ when CSNT = '0'.

10 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals.

11 The $\overline{AS}$ signal is considered asynchronous to CLKOUT.

Figure 2 is the control timing diagram.

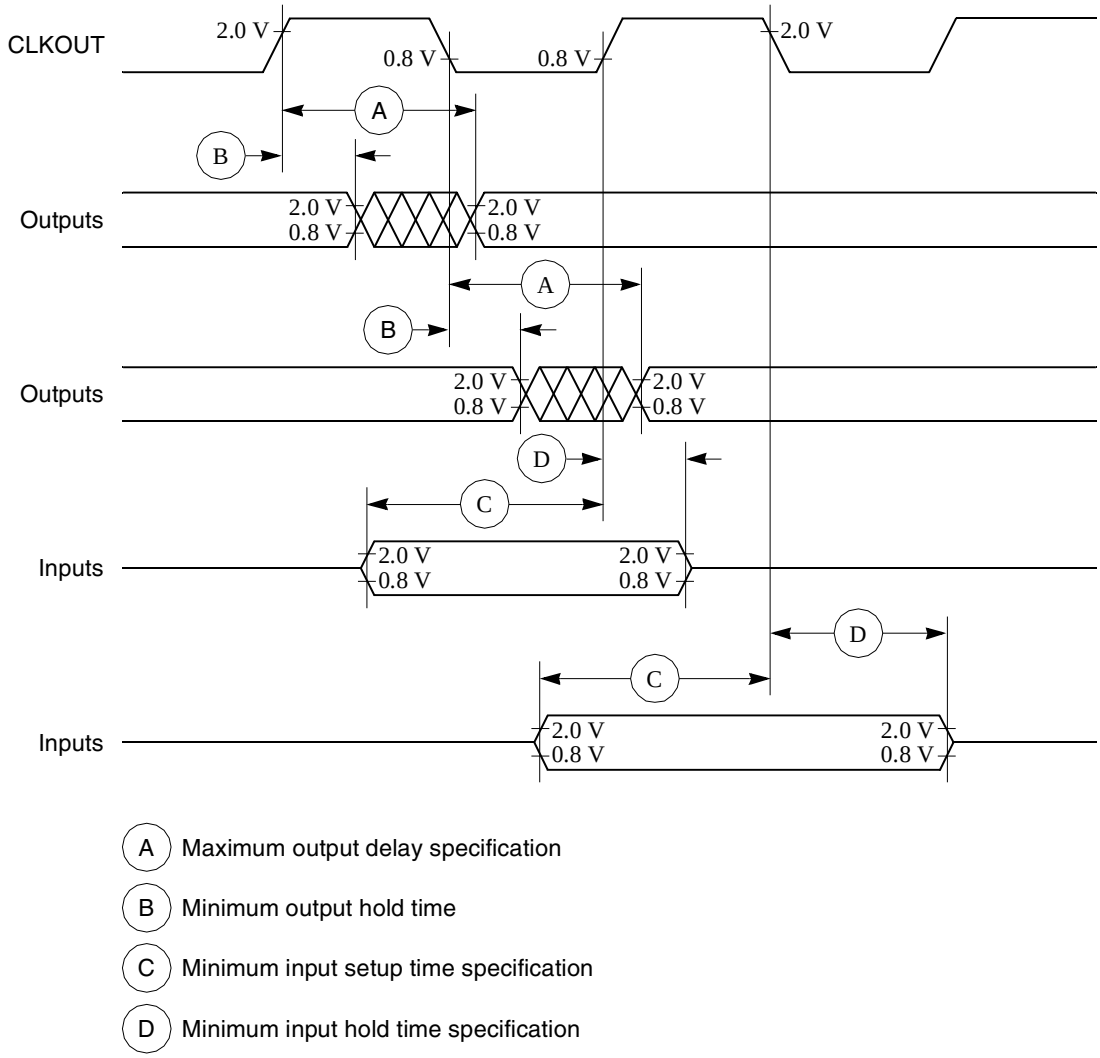

Figure 2. Control Timing

Figure 3 provides the timing for the external clock.

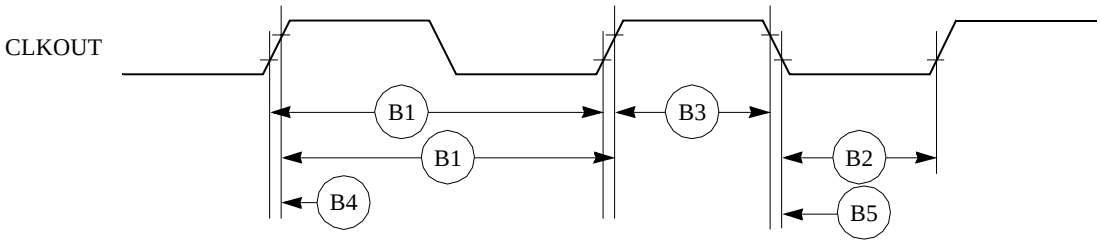

Figure 3. External Clock Timing

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

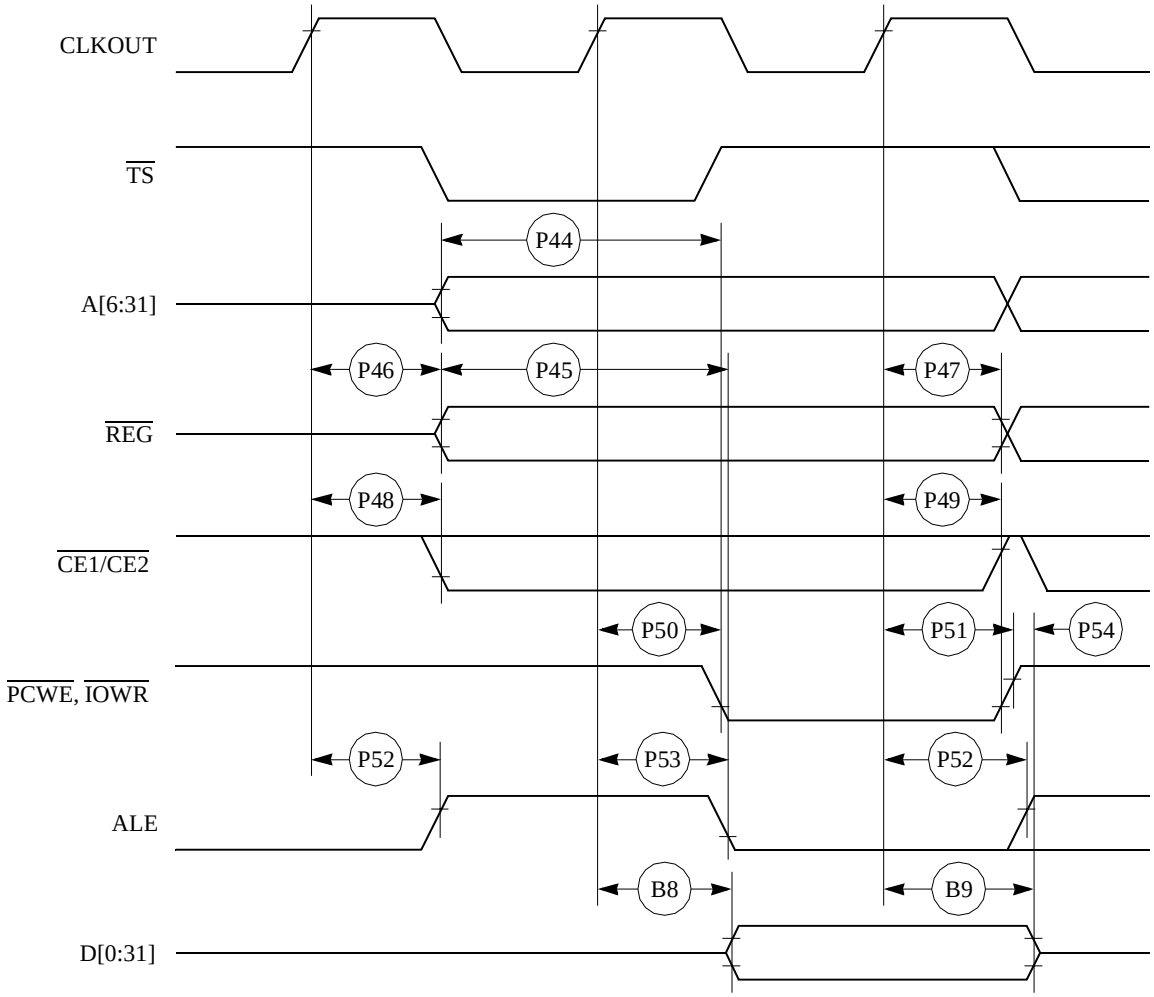

Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.

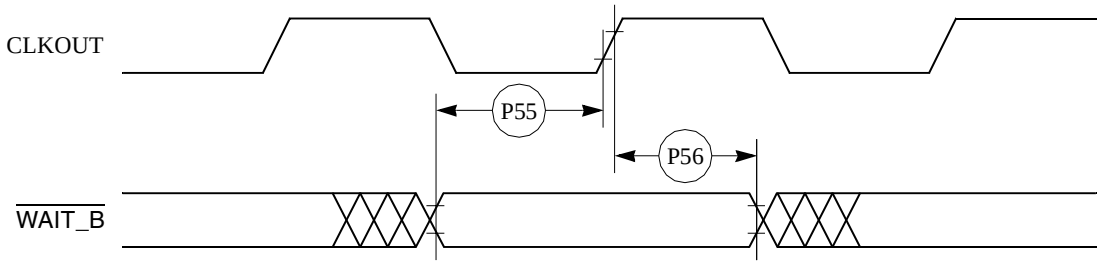

Figure 26. PCMCIA WAIT Signal Detection Timing

Table 11 shows the reset timing for the MPC850.

Table 11. Reset Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	340.00	—	515.00	—	425.00	—	17.000	ns
R72		—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R80	DSDI, DSCK set up	60.00	—	90.00	—	75.00	—	3.000	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns

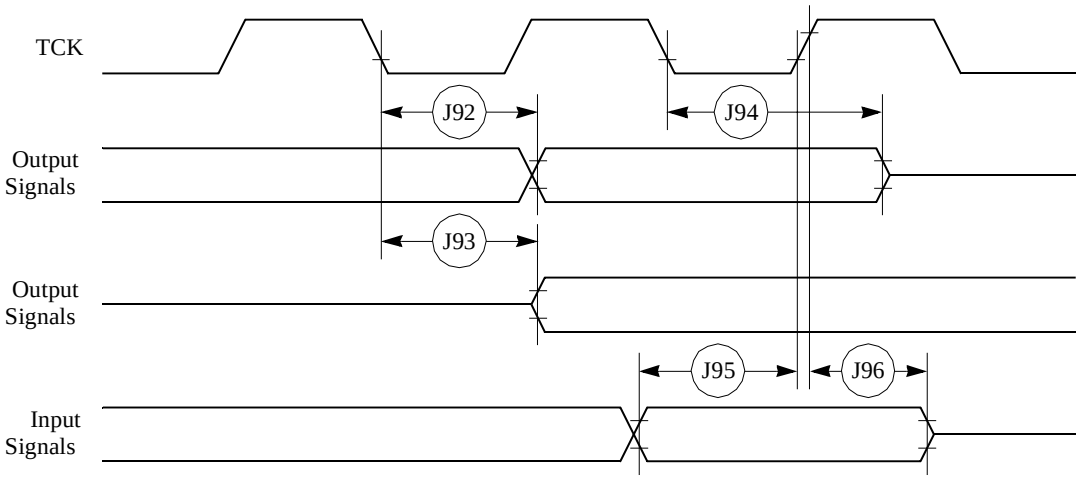

Figure 37. Boundary Scan (JTAG) Timing Diagram

8 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC850.

8.1 PIO AC Electrical Specifications

Table 13 provides the parallel I/O timings for the MPC850 as shown in Figure 38.

Table 13. Parallel I/O Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

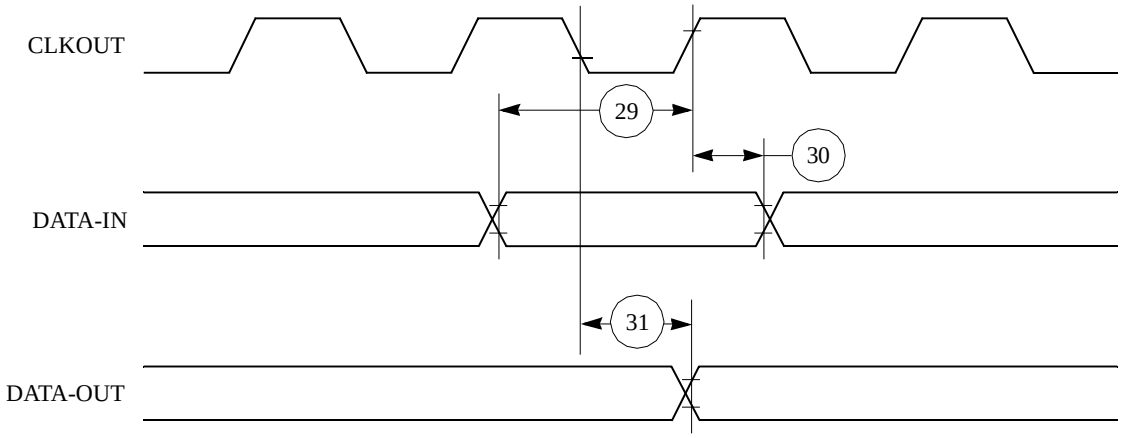

Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Table 14. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7.00	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3.00	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12.00	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12.00	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20.00	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15.00	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7.00	—	ns

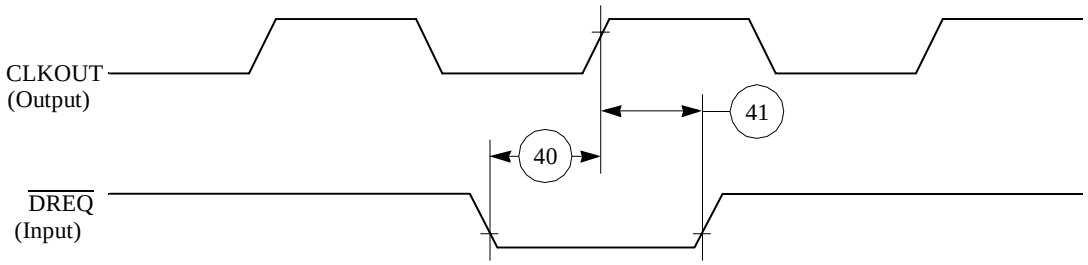

Figure 39. IDMA External Requests Timing Diagram

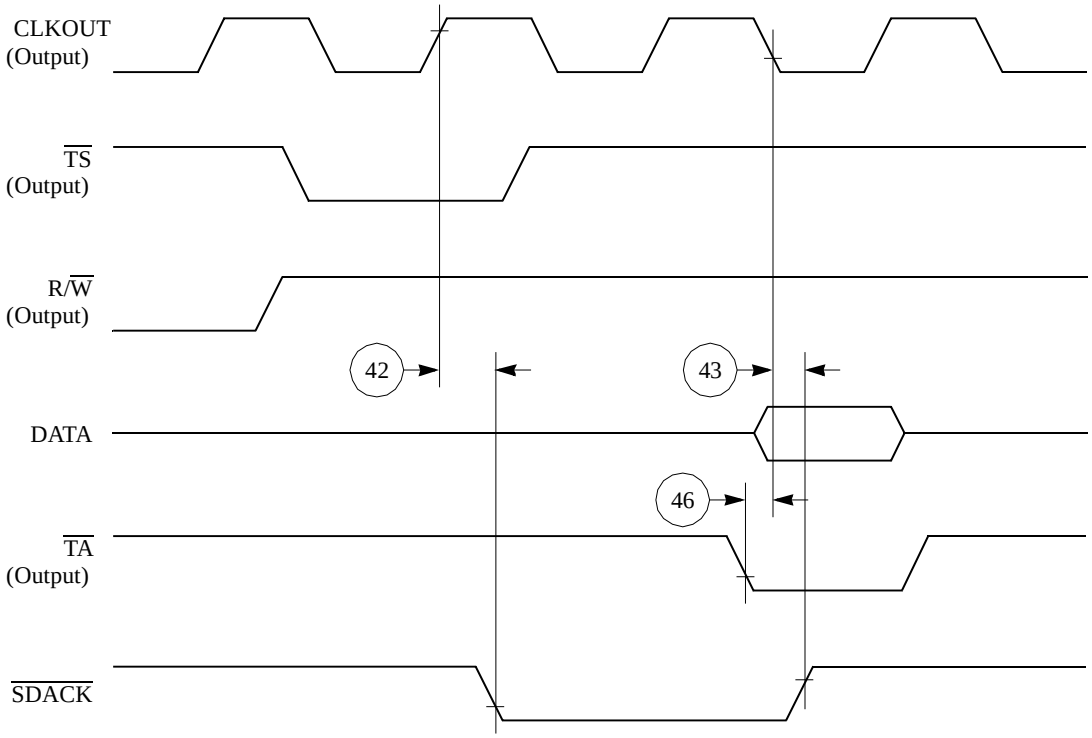

Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock

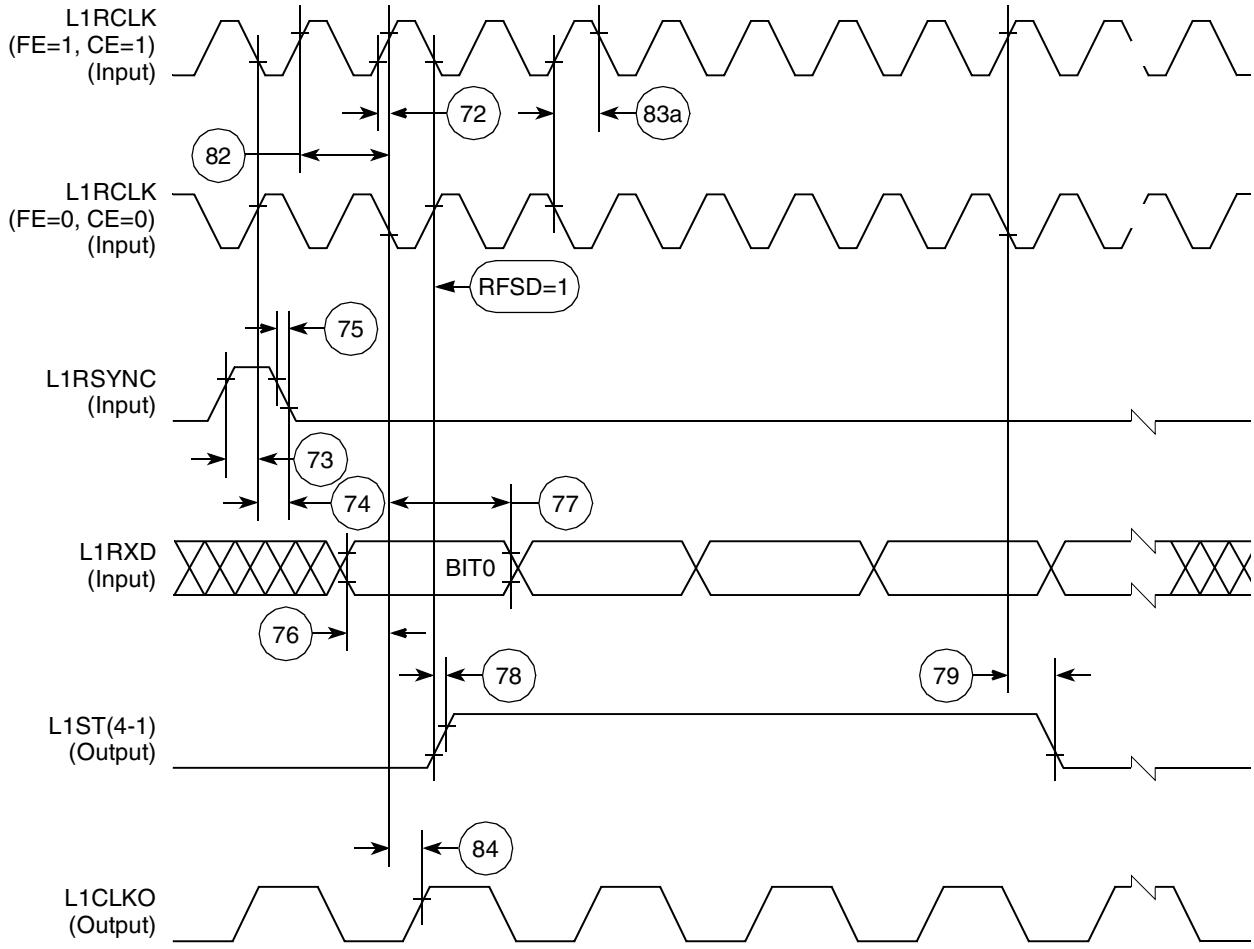

Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

Table 18. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	—	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge [2]	5.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time	—	—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	$\overline{\text{RTSx}}$ active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	$\overline{\text{CTSx}}$ setup time to TCLKx rising edge	40.00	—	ns
106	RXDx setup time to RCLKx rising edge	40.00	—	ns
107	RXDx hold time from RCLKx rising edge [2]	0.00	—	ns
108	$\overline{\text{CDx}}$ setup time to RCLKx rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

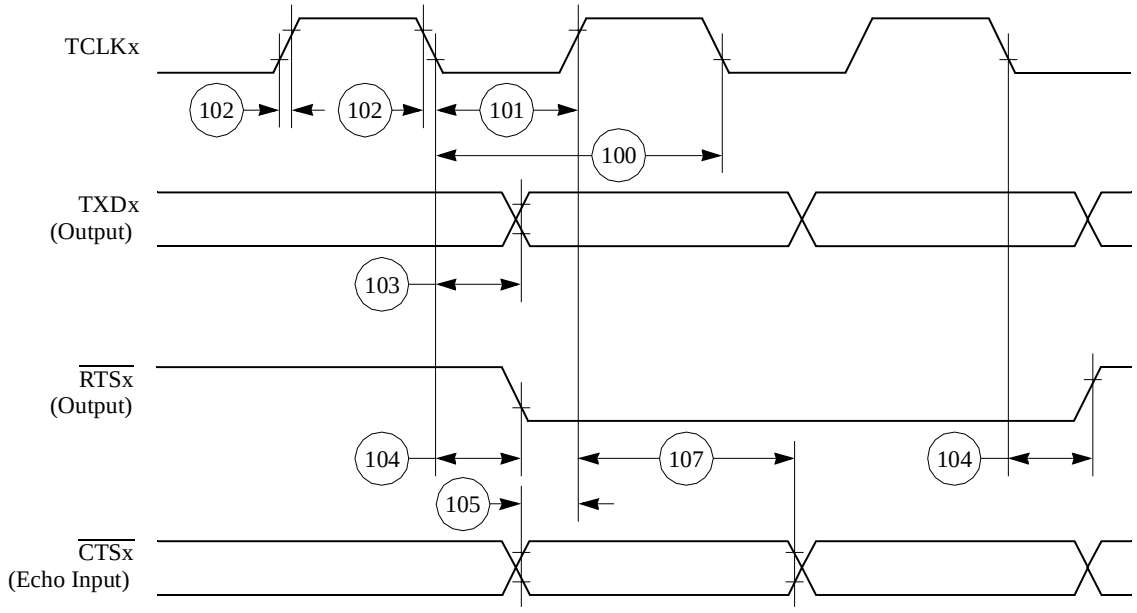

Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period [1]	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period[1]	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns

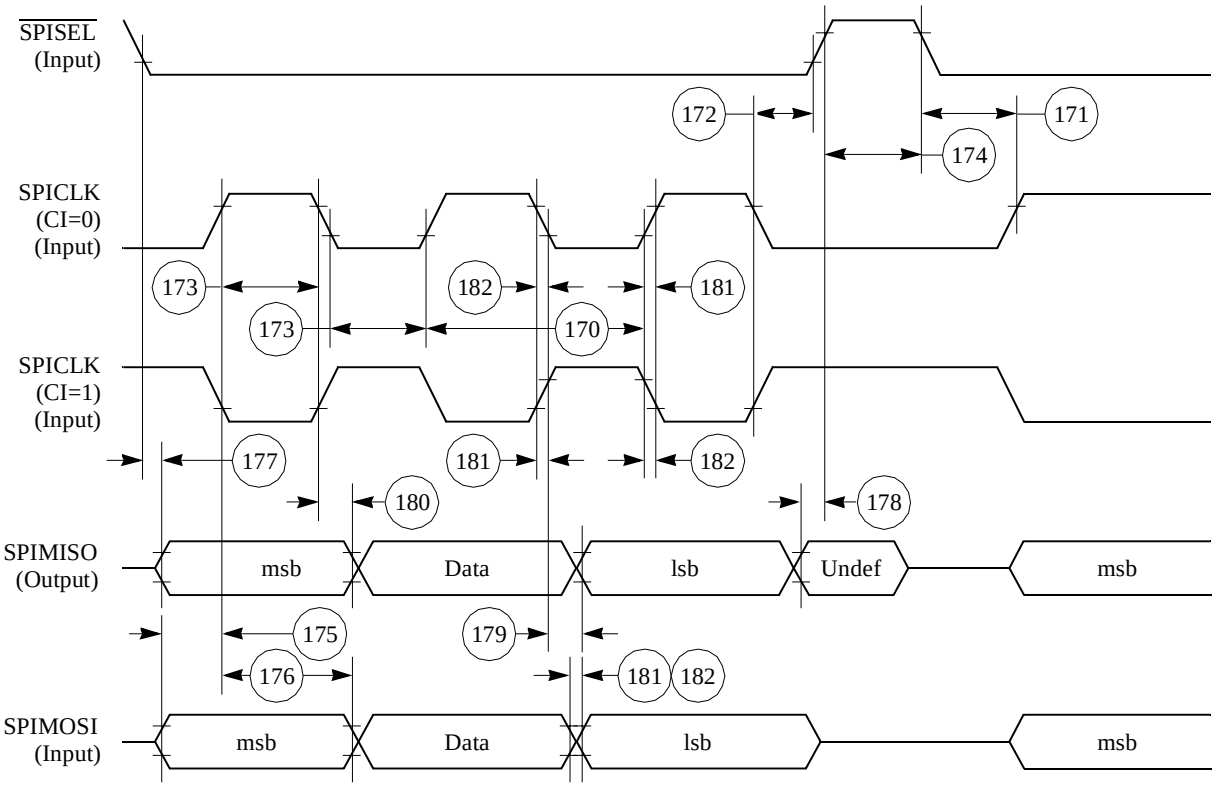

Figure 59. SPI Slave (CP = 0) Timing Diagram

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface.

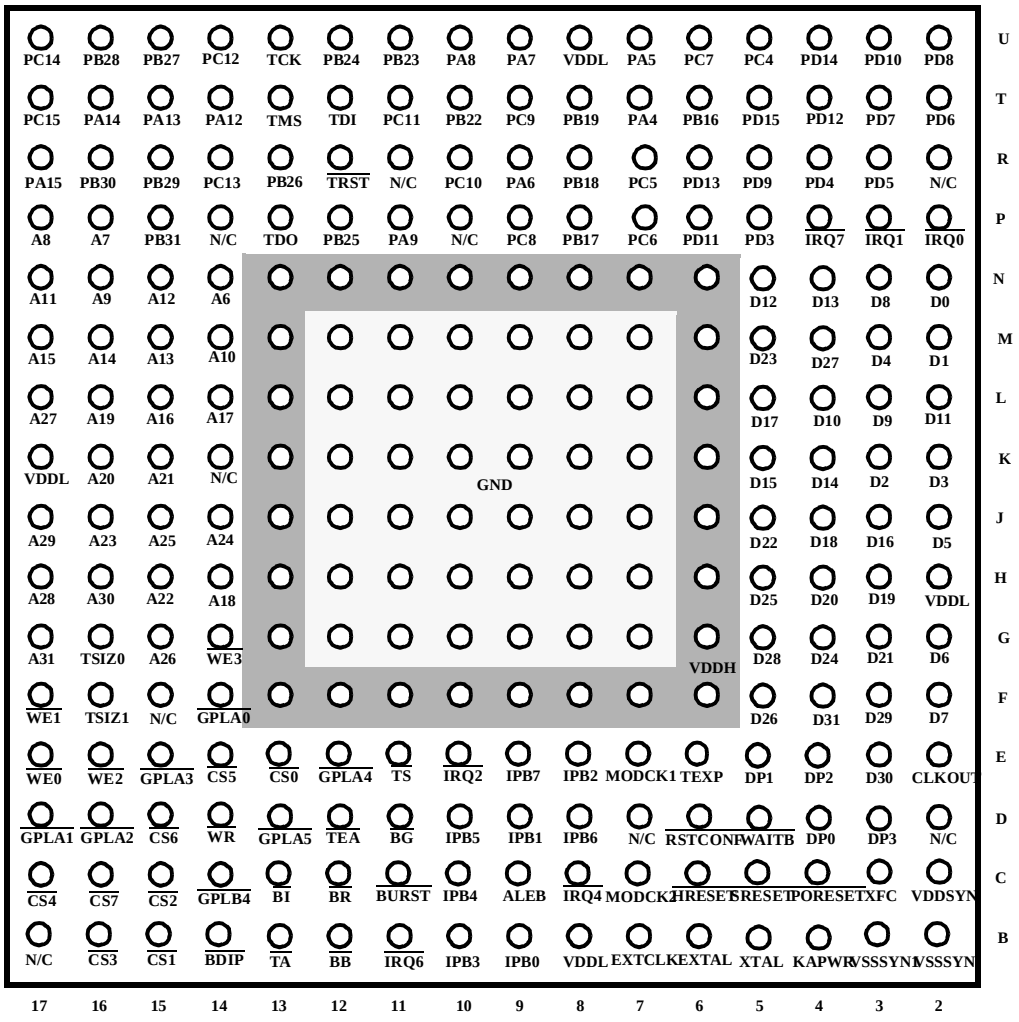

Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

THIS PAGE INTENTIONALLY LEFT BLANK