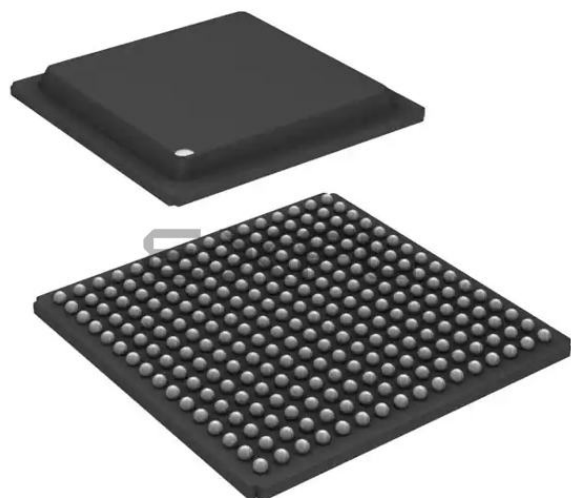




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850dezt66bur2

- Gate mode can enable/disable counting
- Interrupt can be masked on reference match and event capture
- Interrupts
 - Eight external interrupt request (IRQ) lines
 - Twelve port pins with interrupt capability
 - Fifteen internal interrupt sources
 - Programmable priority among SCCs and USB
 - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
 - Master (socket) interface, release 2.1 compliant
 - Single PCMCIA socket
 - Supports eight memory or I/O windows
- Communications processor module (CPM)
 - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
 - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 8 Kbytes of dual-port RAM
 - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
 - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
 - Can be connected to any SCC, SMC, or USB
 - Allow changes during operation
 - Autobaud support option
- Two SCCs (serial communications controllers)
 - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
 - HDLC/SDLC™ (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support PPP (point-to-point protocol)
 - AppleTalk®
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B28c	CLKOUT falling edge to $\overline{\text{WE}}[0-3]$ negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	—	14.00	—	18.00	—	16.00	0.375	50.00	ns
B29	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29a	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29b	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29c	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29d	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29e	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29f	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns
B29g	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns

Figure 13 through Figure 15 provide the timing for the external bus write controlled by various GPCM factors.

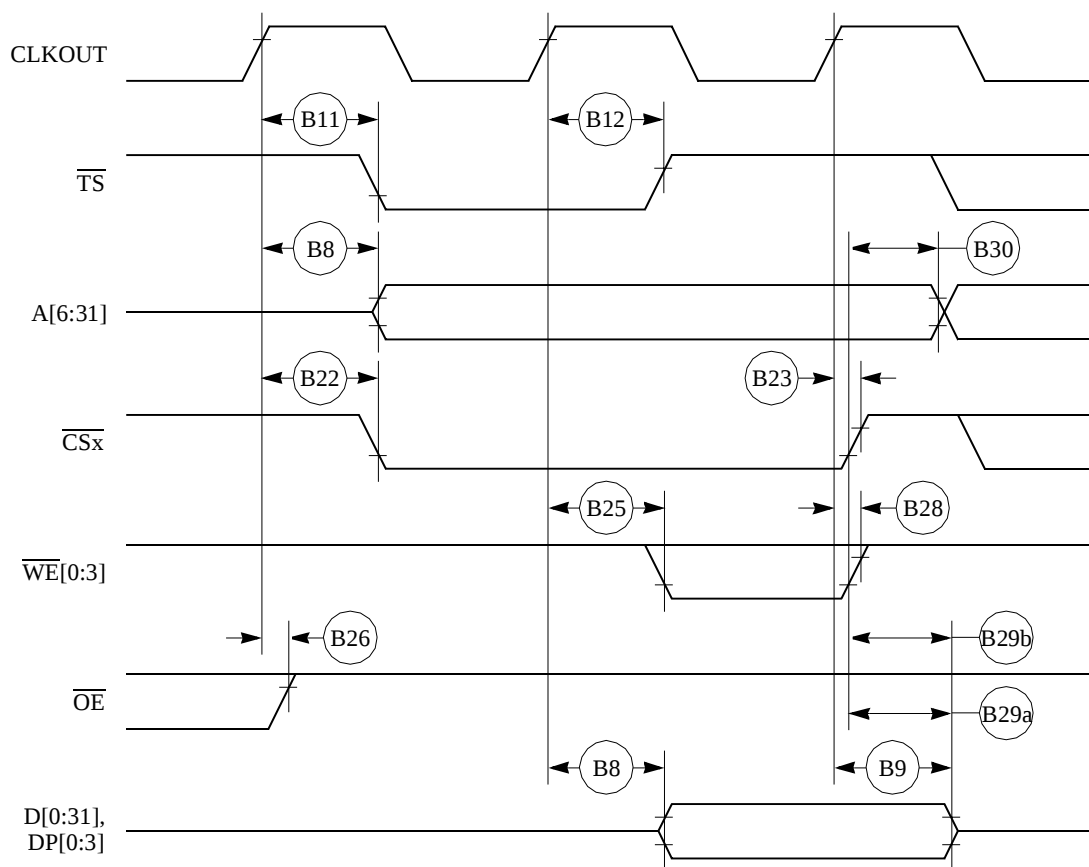


Figure 13. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

Figure 16 provides the timing for the external bus controlled by the UPM.

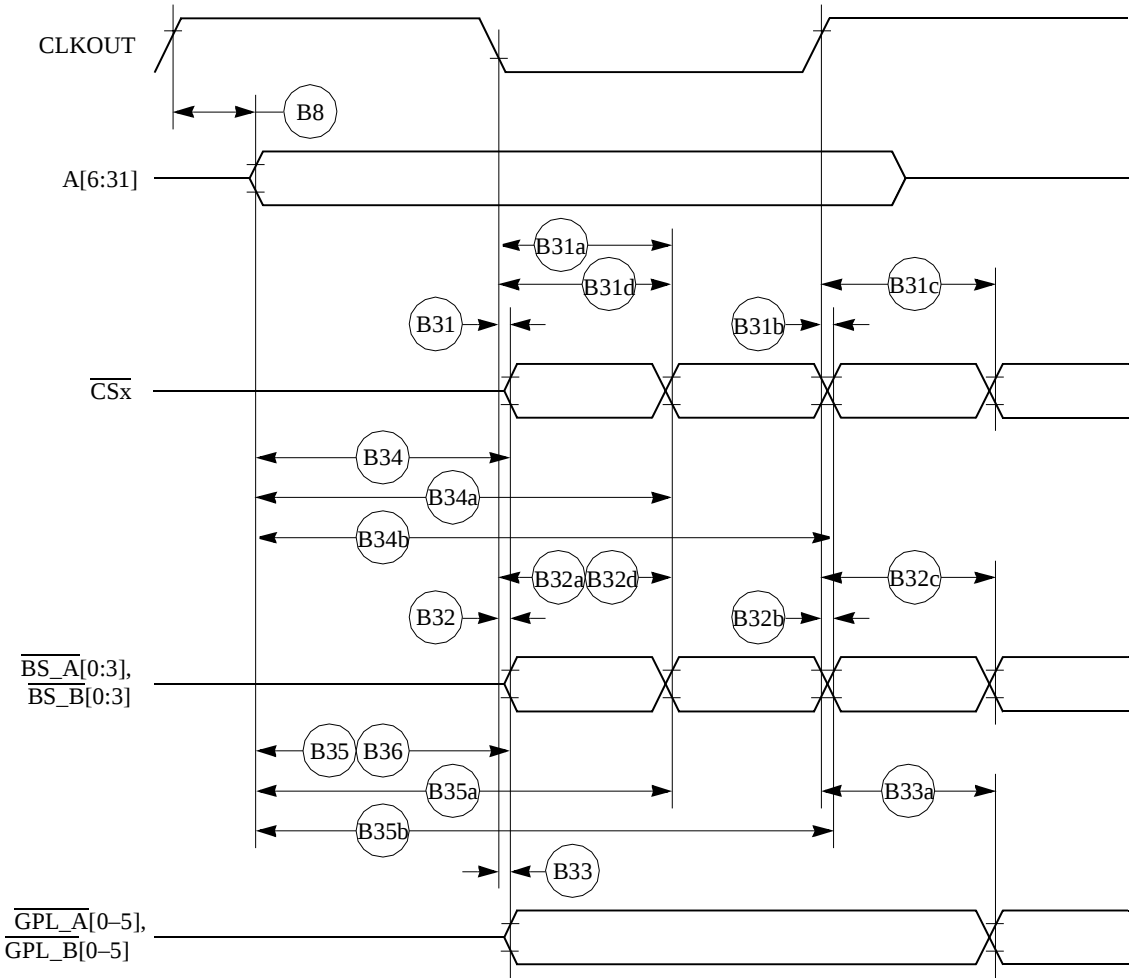


Figure 16. External Bus Timing (UPM Controlled Signals)

Table 8 shows the PCMCIA timing for the MPC850.

Table 8. PCMCIA Timing

Num	Characteristic	50MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
P44	A[6–31], $\overline{\text{REG}}$ valid to PCMCIA strobe asserted. ¹	13.00	—	21.00	—	17.00	—	0.750	ns
P45	A[6–31], $\overline{\text{REG}}$ valid to ALE negation. ¹	18.00	—	28.00	—	23.00	—	1.000	ns
P46	CLKOUT to $\overline{\text{REG}}$ valid	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P47	CLKOUT to $\overline{\text{REG}}$ Invalid.	6.00	—	9.00	—	7.00	—	0.250	ns
P48	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	
P49	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated.	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P50	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time.	—	11.00	—	11.00	—	11.00	—	ns
P51	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time.	2.00	11.00	2.00	11.00	2.00	11.00	—	ns
P52	CLKOUT to ALE assert time	5.00	13.00	8.00	16.00	6.00	14.00	0.250	ns
P53	CLKOUT to ALE negate time	—	13.00	—	16.00	—	14.00	0.250	ns
P54	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D[0–31] invalid. ¹	3.00	—	6.00	—	4.00	—	0.250	ns
P55	$\overline{\text{WAIT_B}}$ valid to CLKOUT rising edge. ¹	8.00	—	8.00	—	8.00	—	—	ns
P56	CLKOUT rising edge to $\overline{\text{WAIT_B}}$ invalid. ¹	2.00	—	2.00	—	2.00	—	—	ns

¹ PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAIT_B}}$ signal is detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAIT_B}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the MPC850 PowerQUICC User's Manual.

Table 9 shows the PCMCIA port timing for the MPC850.

Table 9. PCMCIA Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive ¹	18.00	—	26.00	—	22.00	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

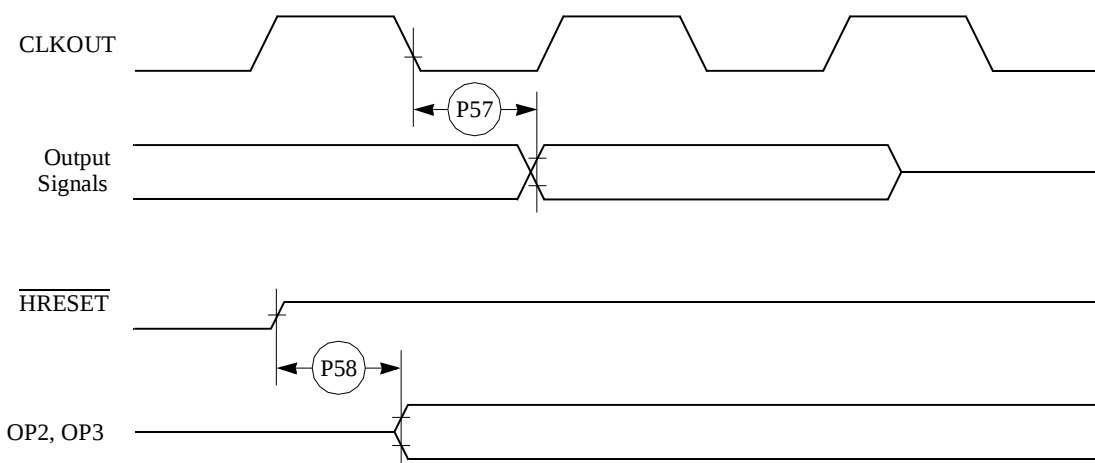


Figure 27. PCMCIA Output Port Timing

Figure 28 provides the PCMCIA output port timing for the MPC850.

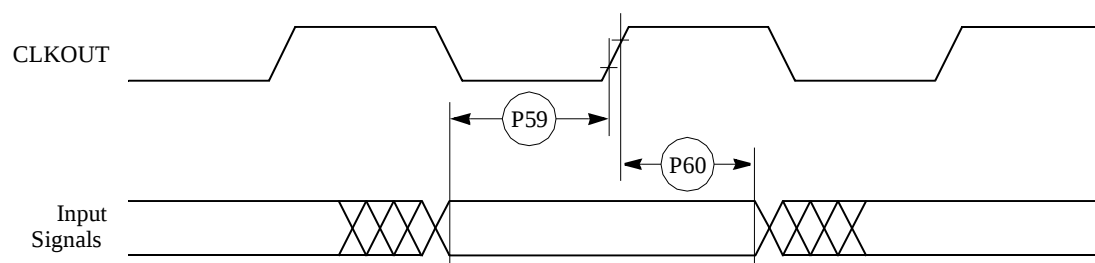


Figure 28. PCMCIA Input Port Timing

Figure 33 provides the reset timing for the debug port configuration.

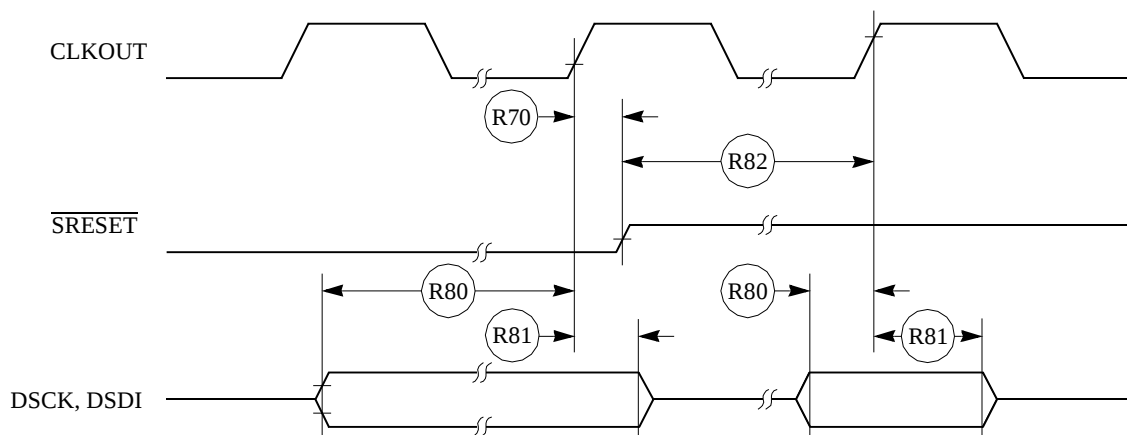


Figure 33. Reset Timing—Debug Port Configuration

7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

Table 12. JTAG Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
J82	TCK cycle time	100.00	—	100.00	—	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	40.00	—	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	5.00	—	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	25.00	—	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	—	27.00	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	0.00	—	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	—	20.00	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	100.00	—	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	40.00	—	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	—	50.00	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	—	50.00	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	—	50.00	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	50.00	—	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	50.00	—	50.00	—	ns

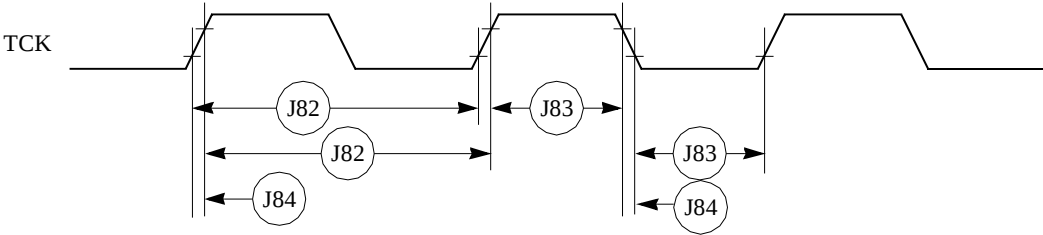


Figure 34. JTAG Test Clock Input Timing

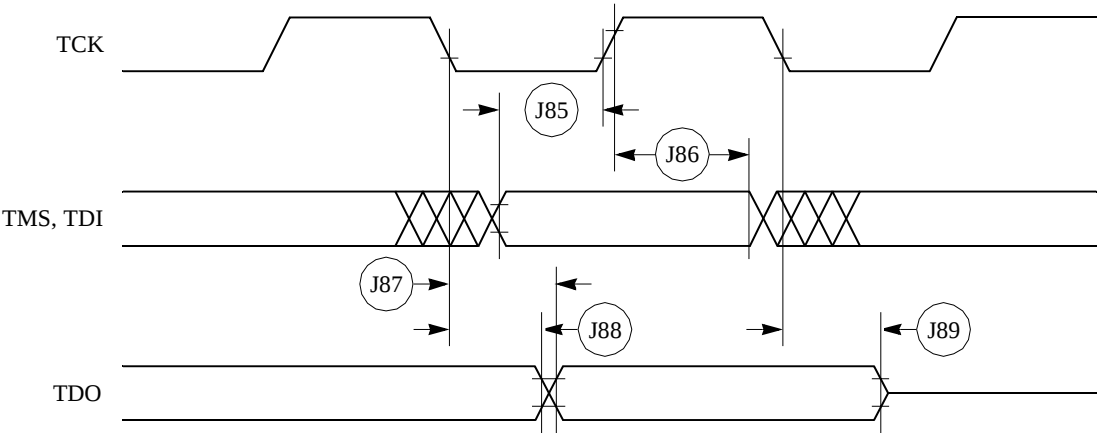


Figure 35. JTAG Test Access Port Timing Diagram

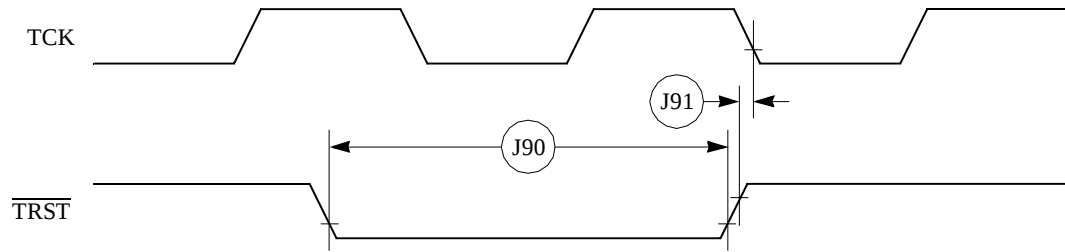


Figure 36. JTAG $\overline{\text{TRST}}$ Timing Diagram

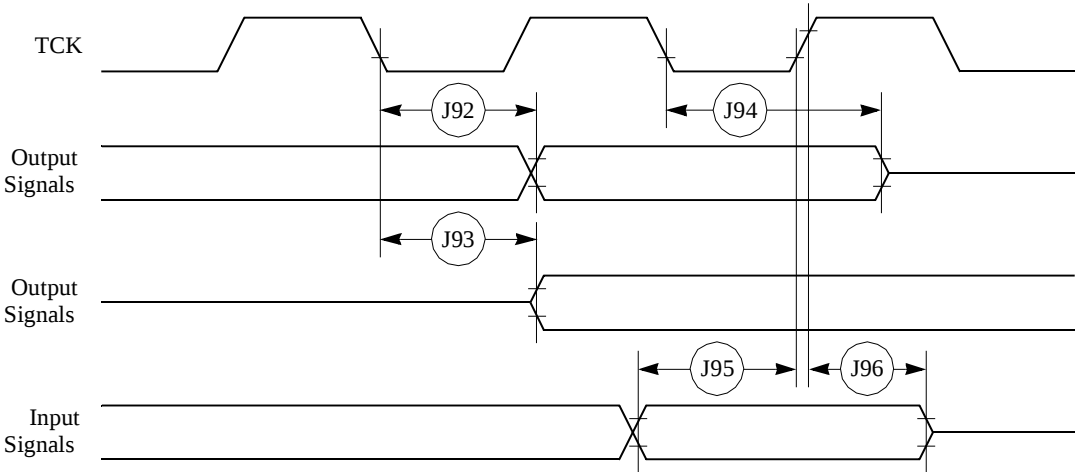


Figure 37. Boundary Scan (JTAG) Timing Diagram

8 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC850.

8.1 PIO AC Electrical Specifications

Table 13 provides the parallel I/O timings for the MPC850 as shown in Figure 38.

Table 13. Parallel I/O Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

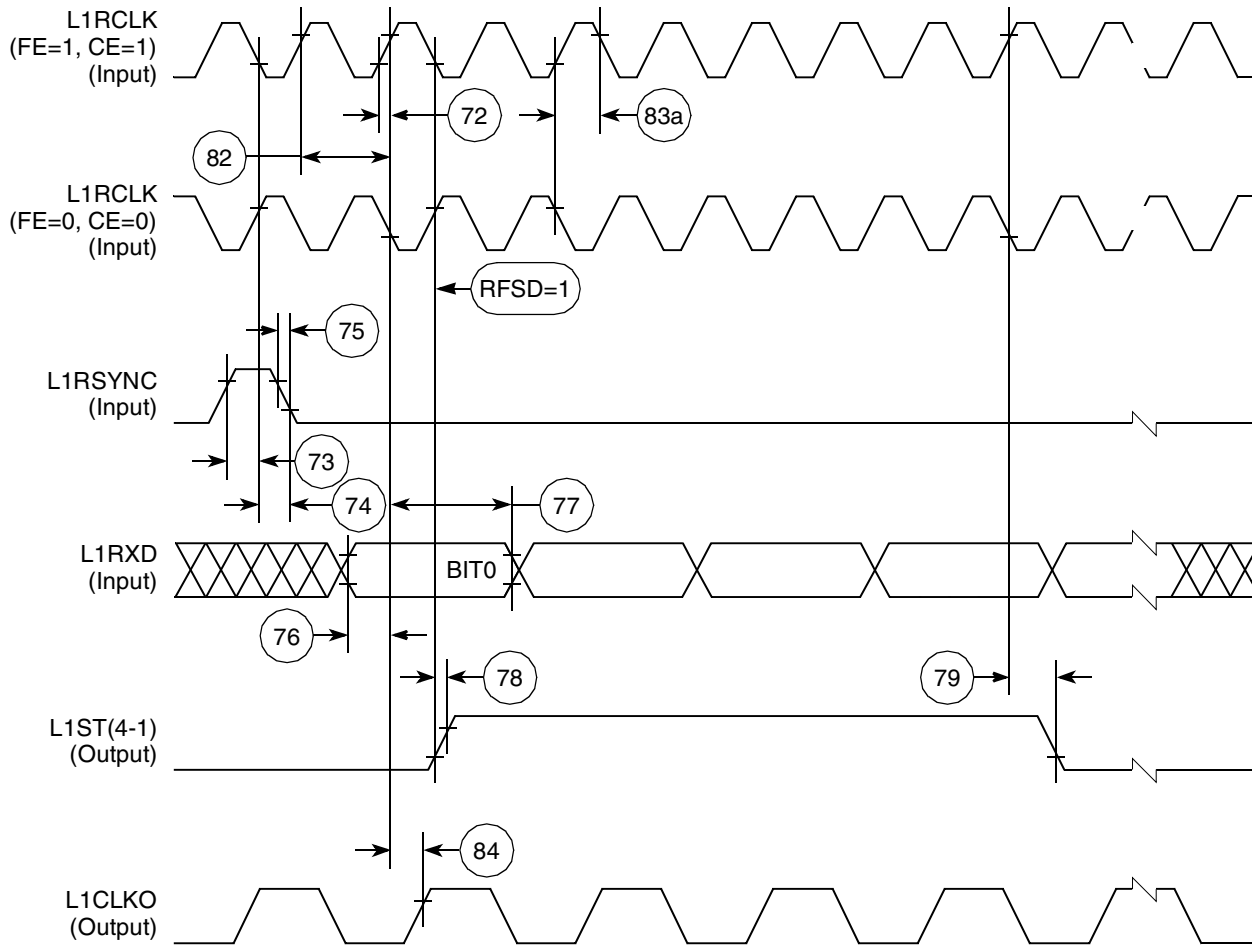


Figure 46. SI Receive Timing with Double-Speed Clocking (DSC = 1)

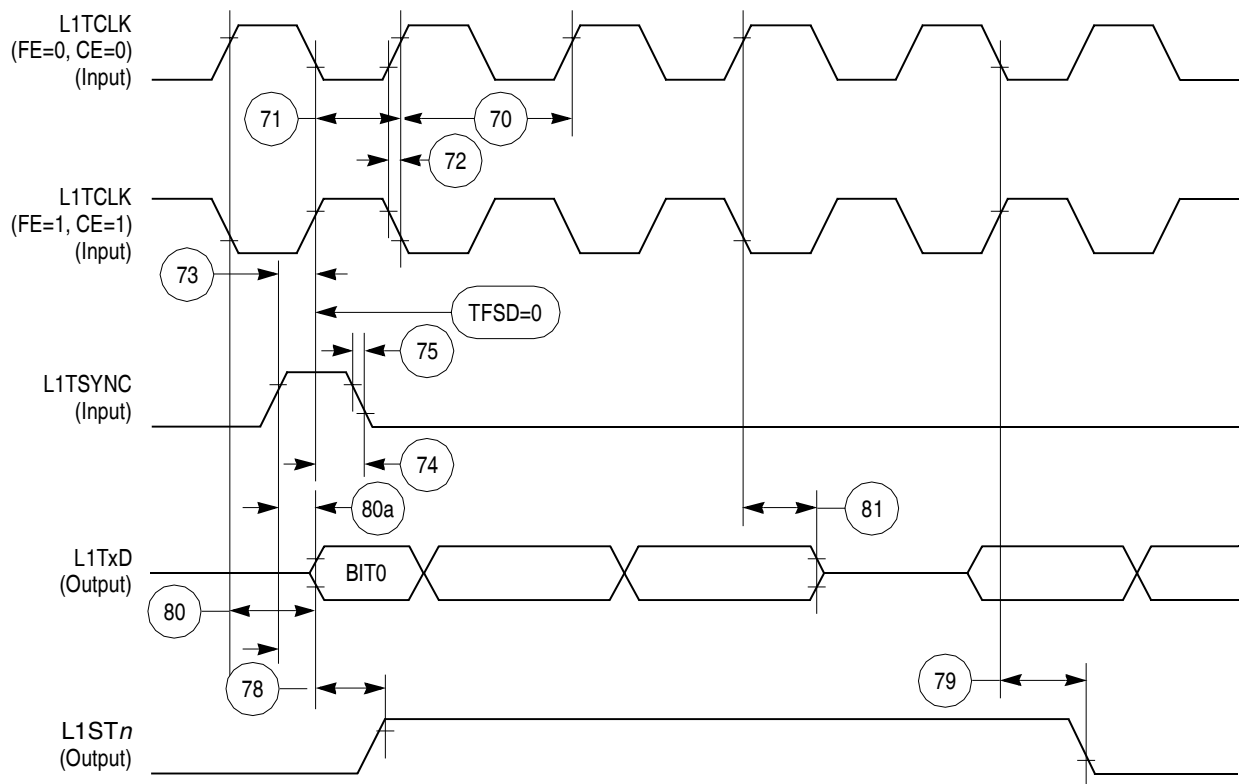


Figure 47. SI Transmit Timing Diagram

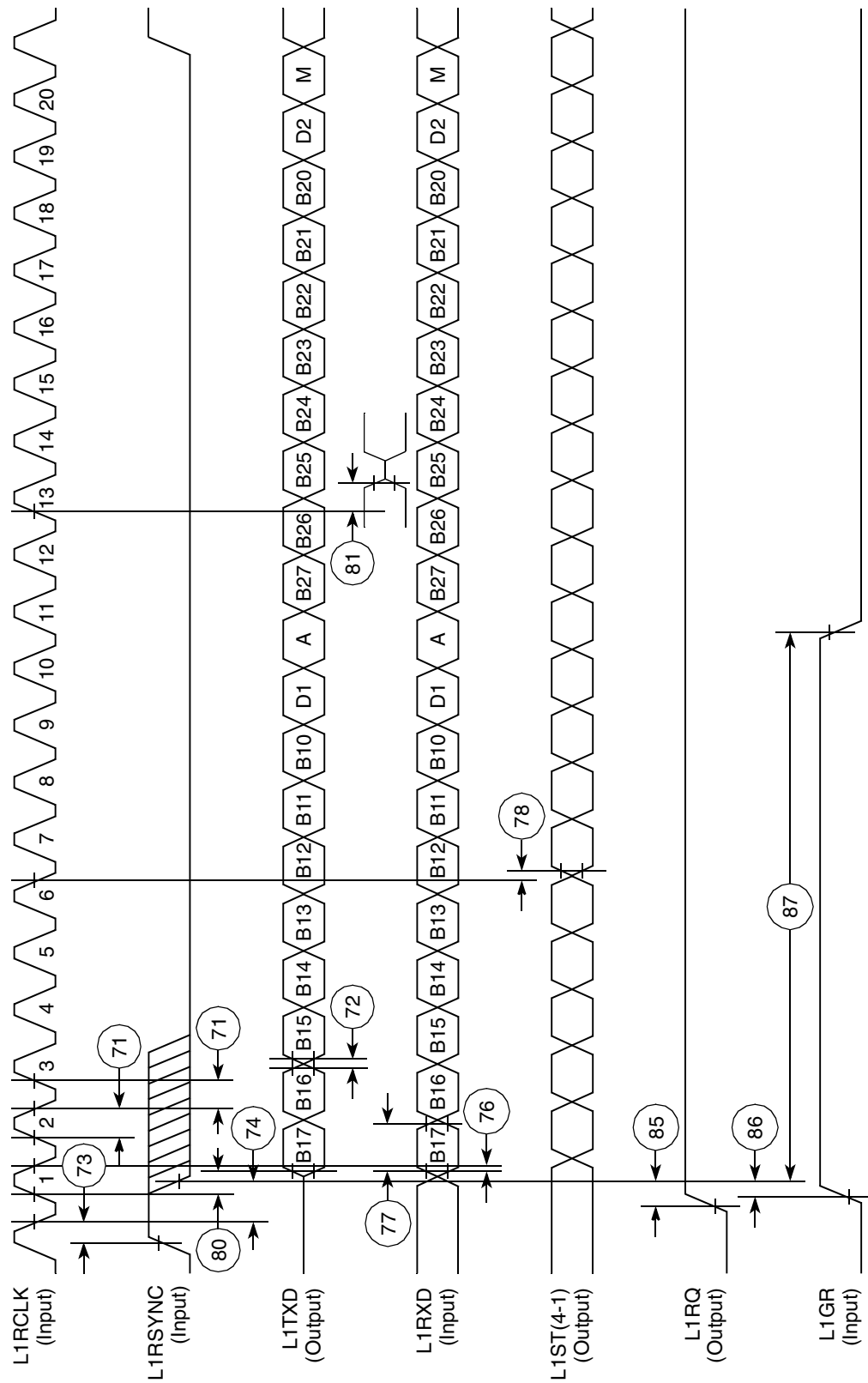


Figure 49. IDL Timing

Figure 50 through Figure 52 show the NMSI timings.

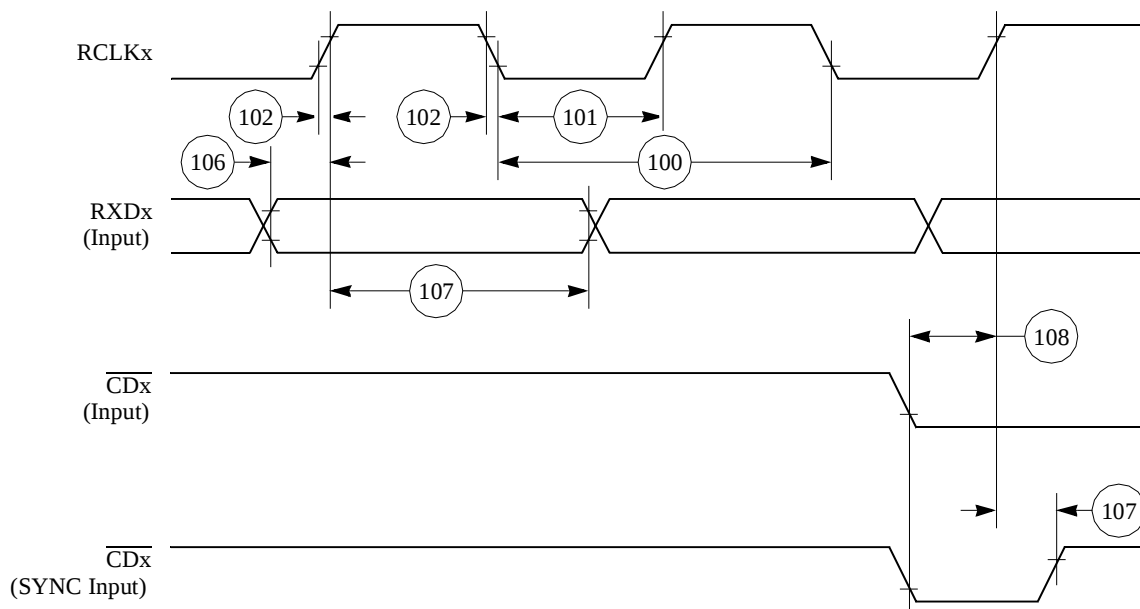


Figure 50. SCC NMSI Receive Timing Diagram

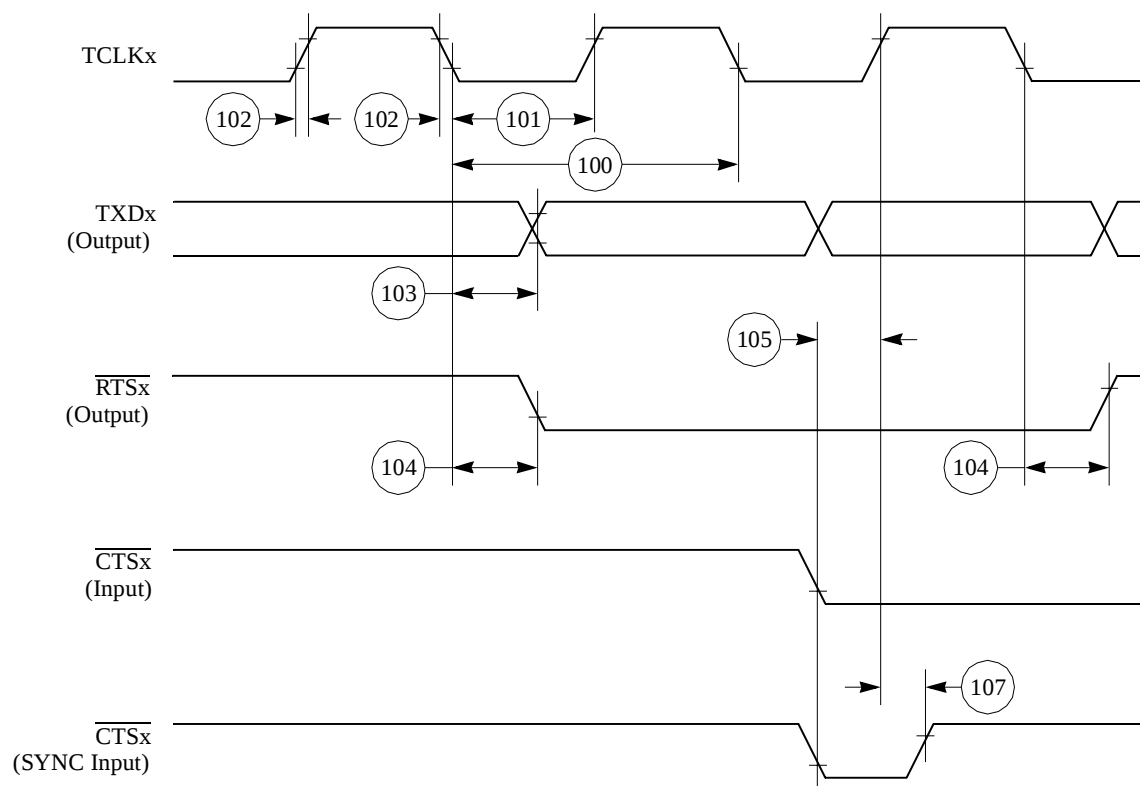


Figure 51. SCC NMSI Transmit Timing Diagram

Table 20. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to $\overline{\text{SDACK}}$ asserted ²	—	20.00	ns
139	CLKOUT low to $\overline{\text{SDACK}}$ negated ²	—	20.00	ns

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame destination address into memory.

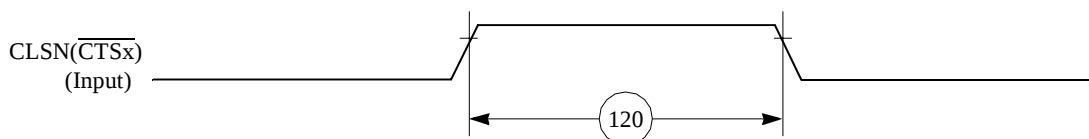


Figure 53. Ethernet Collision Timing Diagram

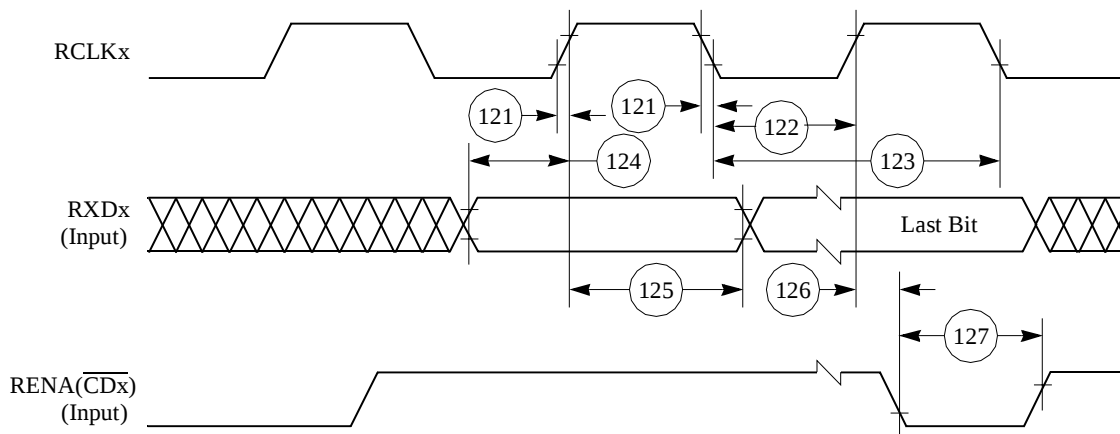
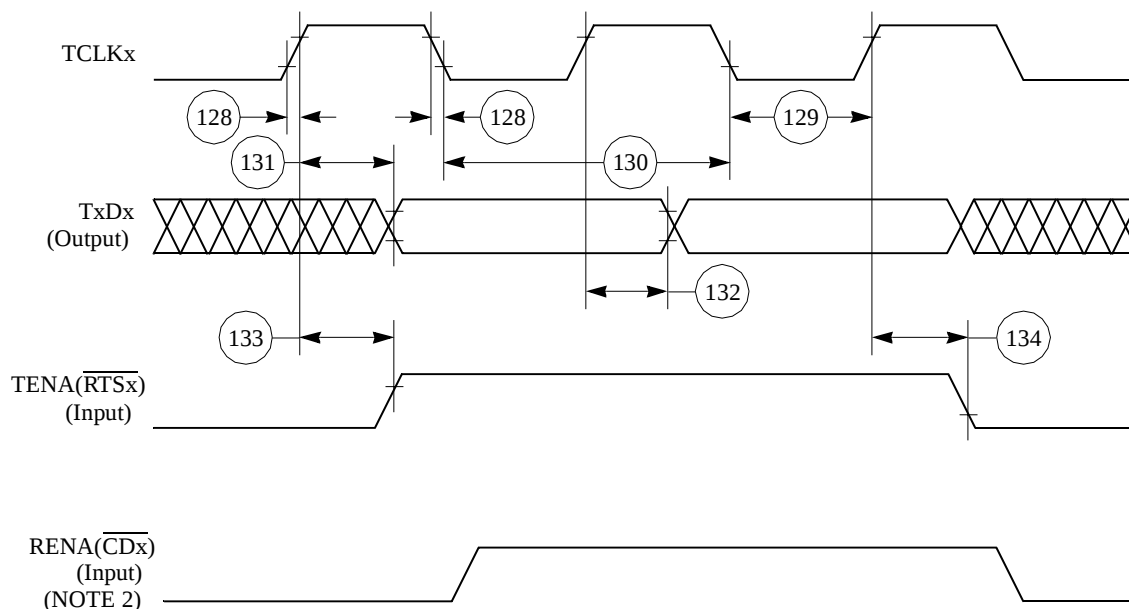


Figure 54. Ethernet Receive Timing Diagram



NOTES:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 55. Ethernet Transmit Timing Diagram

8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

Table 21. Serial Management Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLKx clock period ¹	100.00	—	ns
151	SMCLKx width low	50.00	—	ns
151a	SMCLKx width high	50.00	—	ns
152	SMCLKx rise/fall time	—	15.00	ns
153	SMTXDx active delay (from SMCLKx falling edge)	10.00	50.00	ns
154	SMRXDx/SMSYNx setup time	20.00	—	ns
155	SMRXDx/SMSYNx hold time	5.00	—	ns

¹ The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.

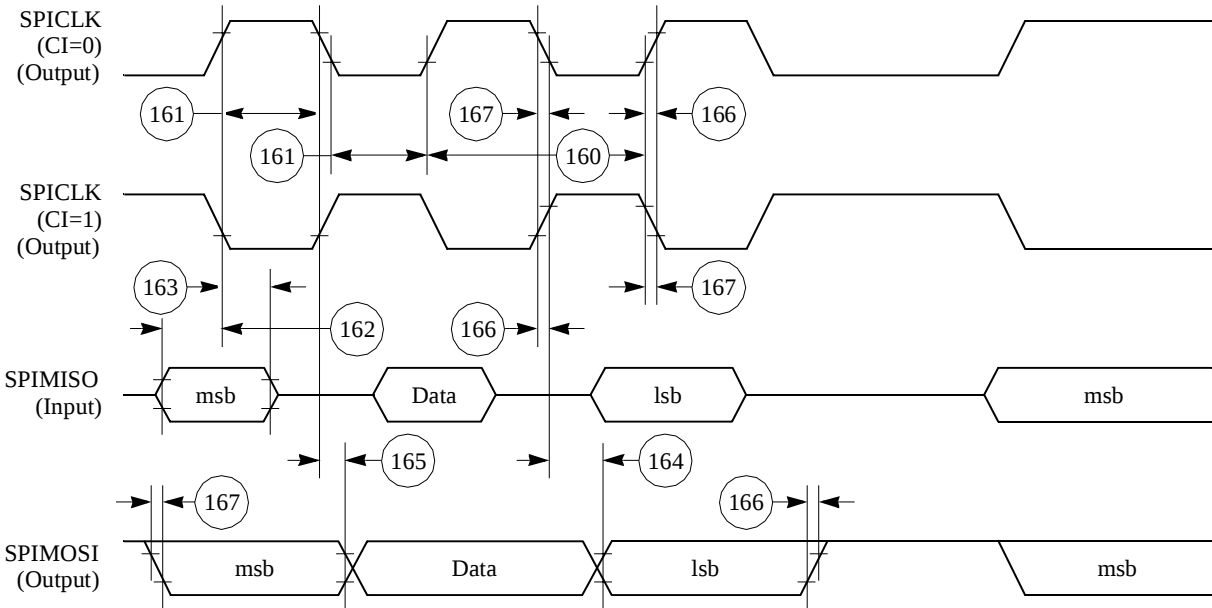


Figure 57. SPI Master (CP = 0) Timing Diagram

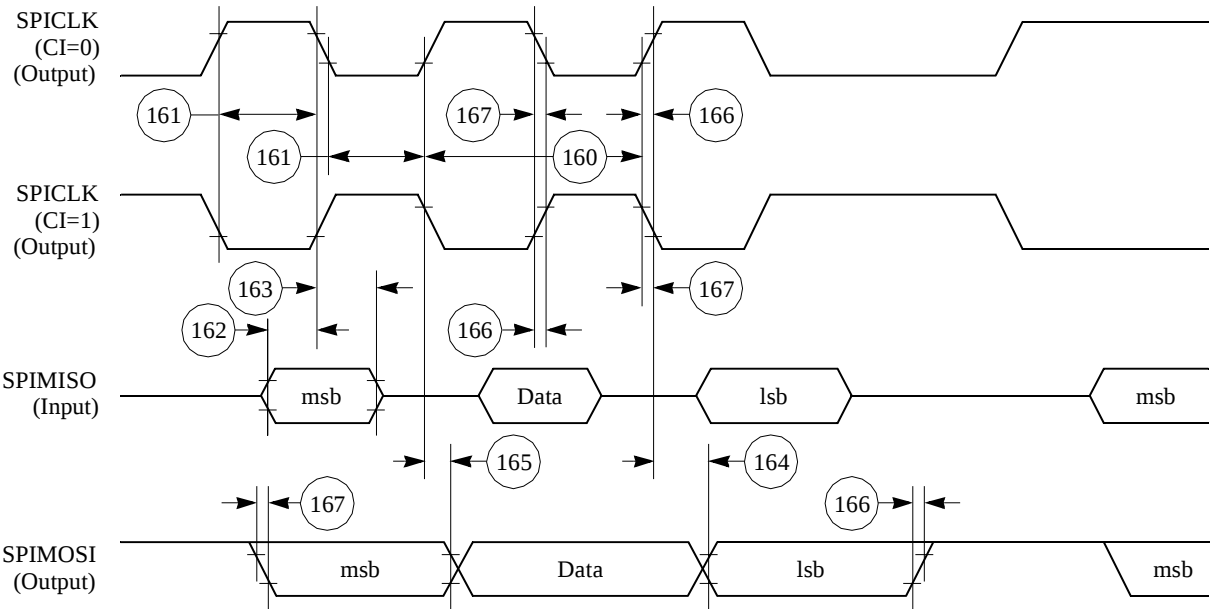


Figure 58. SPI Master (CP = 1) Timing Diagram

8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

Table 23. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t _{cyc}
171	Slave enable lead time	15.00	—	ns
172	Slave enable lag time	15.00	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t _{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t _{cyc}
175	Slave data setup time (inputs)	20.00	—	ns
176	Slave data hold time (inputs)	20.00	—	ns
177	Slave access time	—	50.00	ns
178	Slave SPI MISO disable time	—	50.00	ns
179	Slave data valid (after SPICLK edge)	—	50.00	ns
180	Slave data hold time (outputs)	0.00	—	ns
181	Rise time (input)	—	15.00	ns
182	Fall time (input)	—	15.00	ns

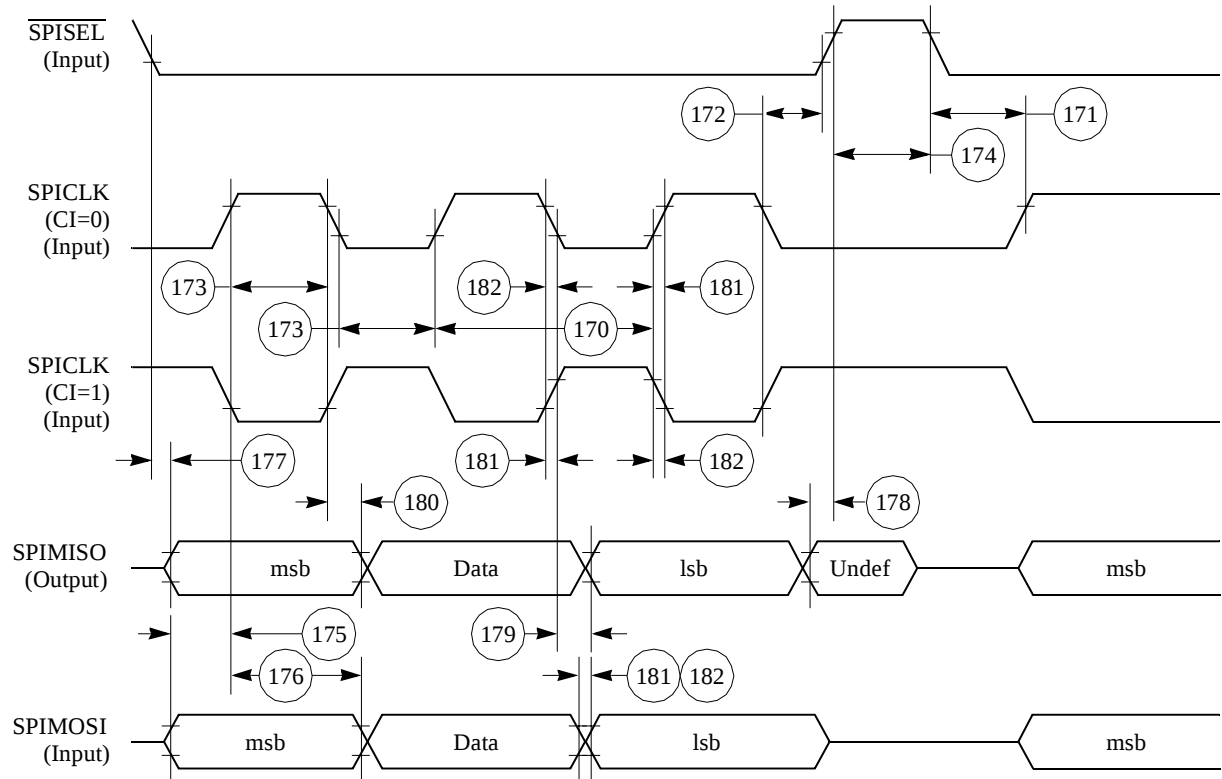


Figure 59. SPI Slave (CP = 0) Timing Diagram

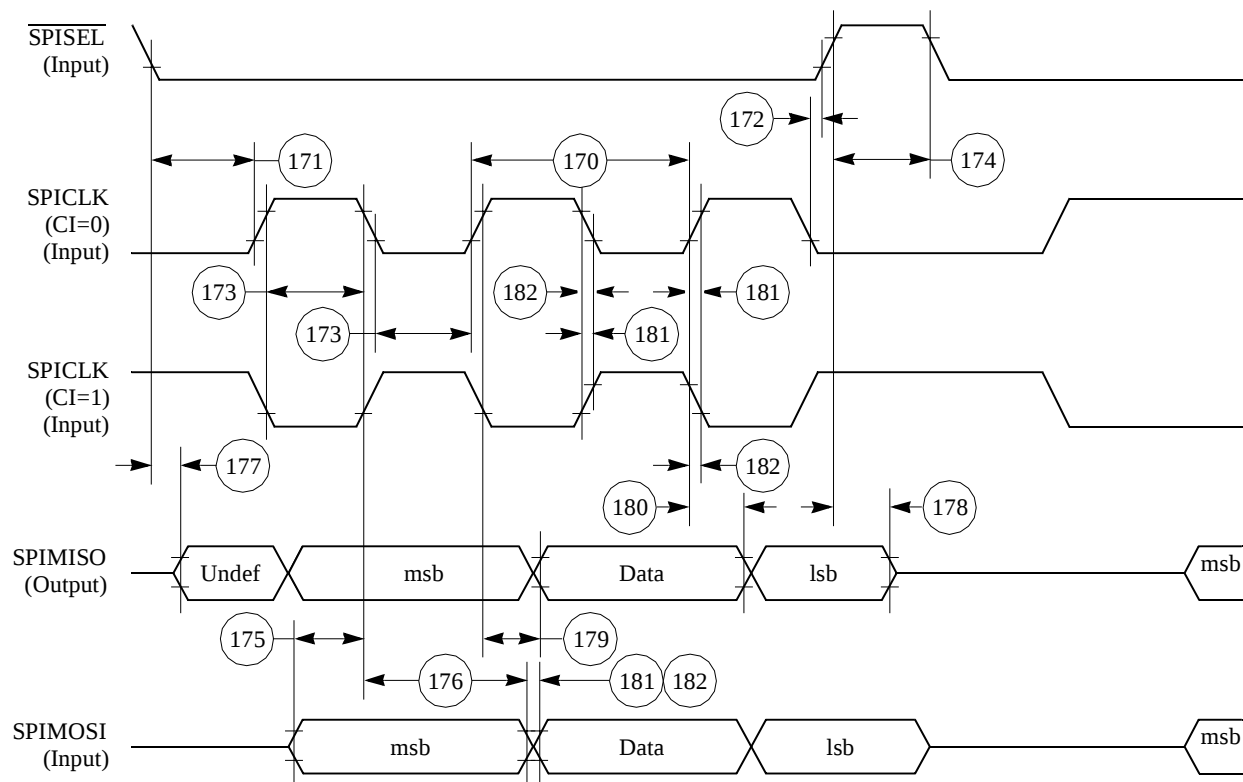


Figure 60. SPI Slave (CP = 1) Timing Diagram

8.11 I²C AC Electrical Specifications

Table 24 provides the I²C (SCL < 100 KHz) timings.

Table 24. I²C Timing (SCL < 100 KHz)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
200	SCL clock frequency (slave)	0.00	100.00	KHz
200	SCL clock frequency (master) ¹	1.50	100.00	KHz
202	Bus free time between transmissions	4.70	—	μs
203	Low period of SCL	4.70	—	μs
204	High period of SCL	4.00	—	μs
205	Start condition setup time	4.70	—	μs
206	Start condition hold time	4.00	—	μs
207	Data hold time	0.00	—	μs
208	Data setup time	250.00	—	ns
209	SDL/SCL rise time	—	1.00	μs

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

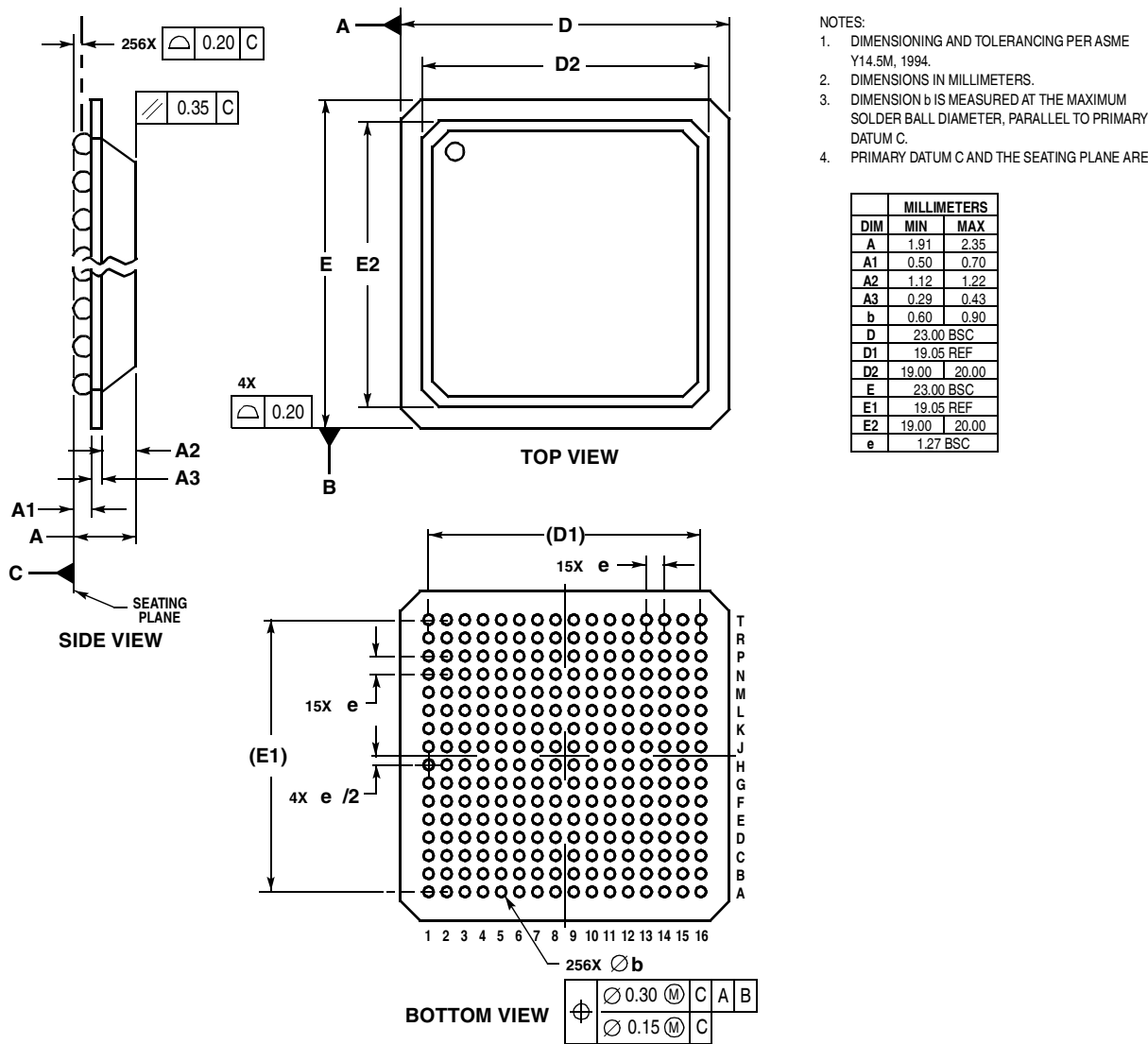


Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard