

Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850dslvr50bu

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I²C port
- One serial peripheral interface (SPI).

[Table 1](#) shows the functionality supported by the members of the MPC850 family.

Table 1. MPC850 Functionality Matrix

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Additional documentation may be provided for parts listed in [Table 1](#).

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA ¹	θ_{JA}	40 ²	°C/W
	θ_{JA}	31 ³	°C/W
	θ_{JA}	24 ⁴	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

¹ For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

² Assumes natural convection and a single layer board (no thermal vias).

³ Assumes natural convection, a multilayer board with thermal vias⁴, 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

⁴ Assumes natural convection, a multilayer board with thermal vias⁴, 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

$$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical ¹	Maximum ²	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

¹ Typical power dissipation is measured at 3.3V

² Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

θ_{JA} = Package thermal resistance, junction to ambient, °C/W

$$P_D = P_{INT} + P_{I/O}$$

$$P_{INT} = I_{DD} \times V_{DD}, \text{ watts—chip internal power}$$

$P_{I/O}$ = Power dissipation on input and output pins—user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \div (T_J + 273^\circ\text{C})(2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273^\circ\text{C}) + \theta_{JA} \bullet P_D^2(3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

5.1 Layout Practices

Each V_{CC} pin on the MPC850 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC850 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

6 Bus Signal Timing

Table 6 provides the bus operation timing for the MPC850 at 50 MHz, 66 MHz, and 80 MHz. Timing information for other bus speeds can be interpolated by equation using the MPC850 Electrical Specifications Spreadsheet found at <http://www.mot.com/netcomm>.

The maximum bus speed supported by the MPC850 is 50 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC850 used at 66 MHz must be configured for a 33 MHz bus).

The timing for the MPC850 bus shown assumes a 50-pF load. This timing can be derated by 1 ns per 10 pF. Derating calculations can also be performed using the MPC850 Electrical Specifications Spreadsheet.

Table 6. Bus Operation Timing ¹ (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B28c	CLKOUT falling edge to $\overline{\text{WE}}[0-3]$ negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	—	14.00	—	18.00	—	16.00	0.375	50.00	ns
B29	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29a	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29b	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29c	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29d	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29e	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29f	$\overline{\text{WE}}[0-3]$ negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns
B29g	$\overline{\text{CS}}$ negated to D[0-31], DP[0-3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns

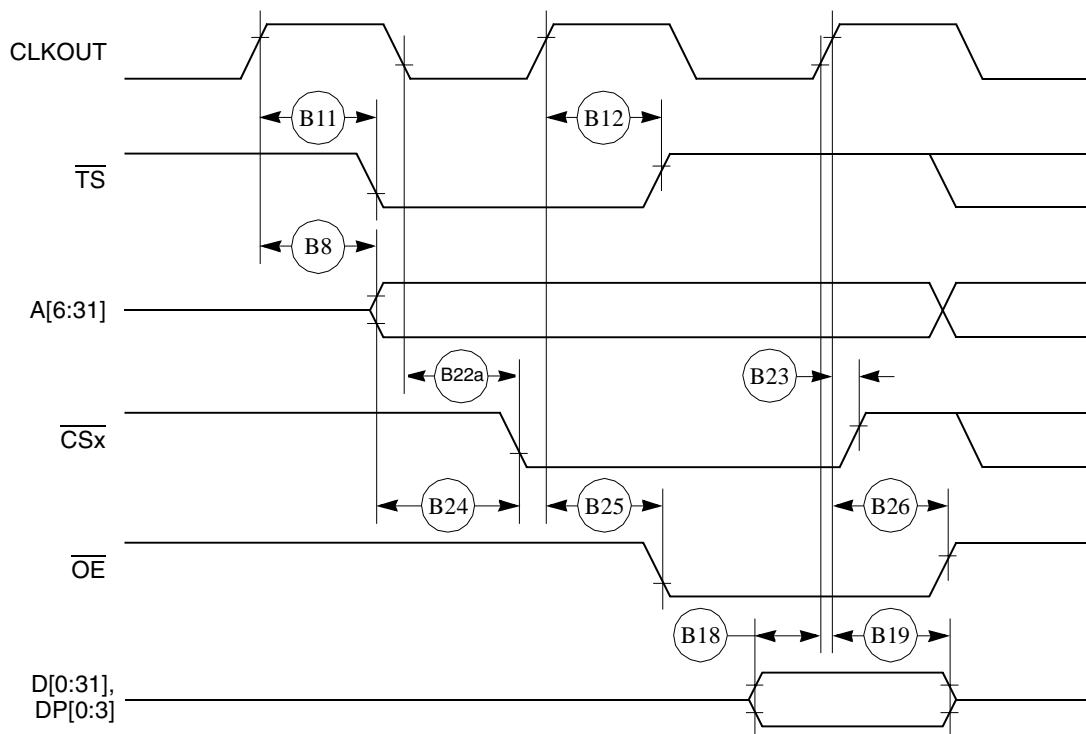


Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

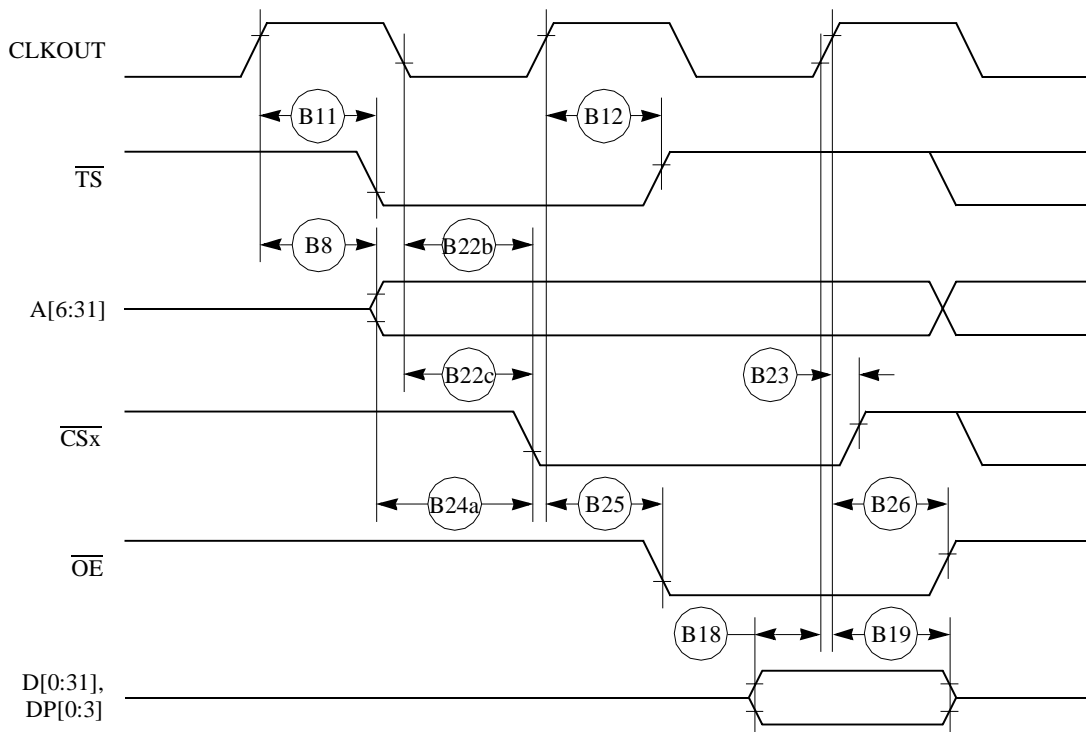


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

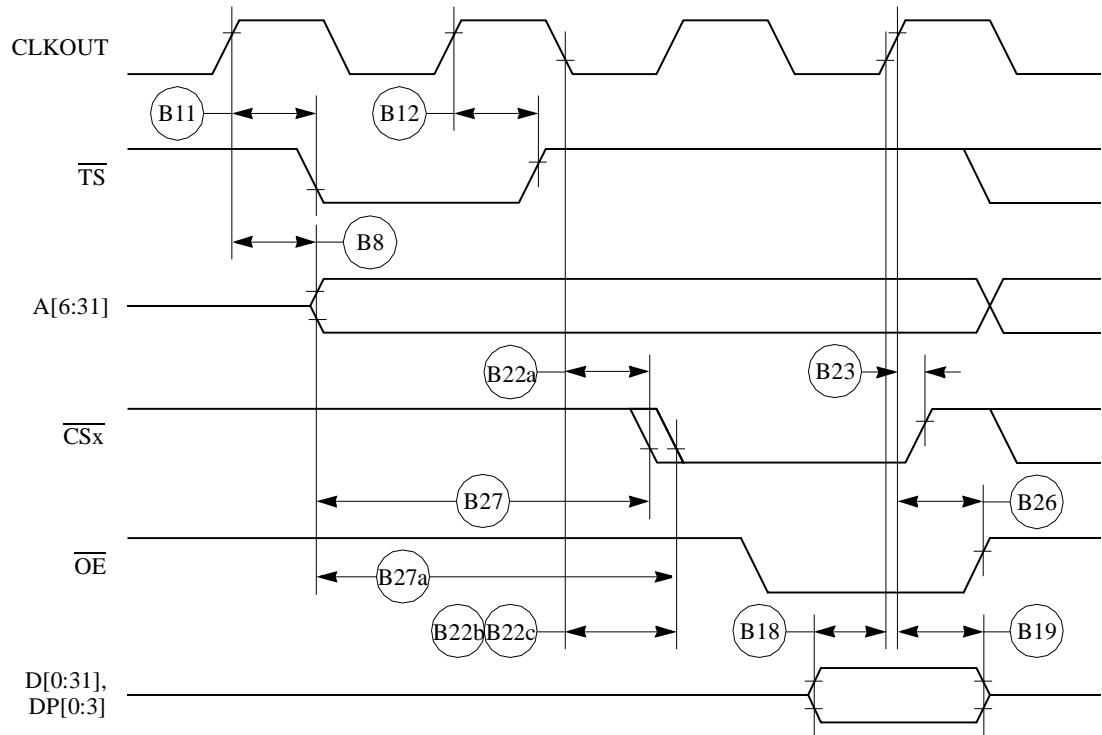


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

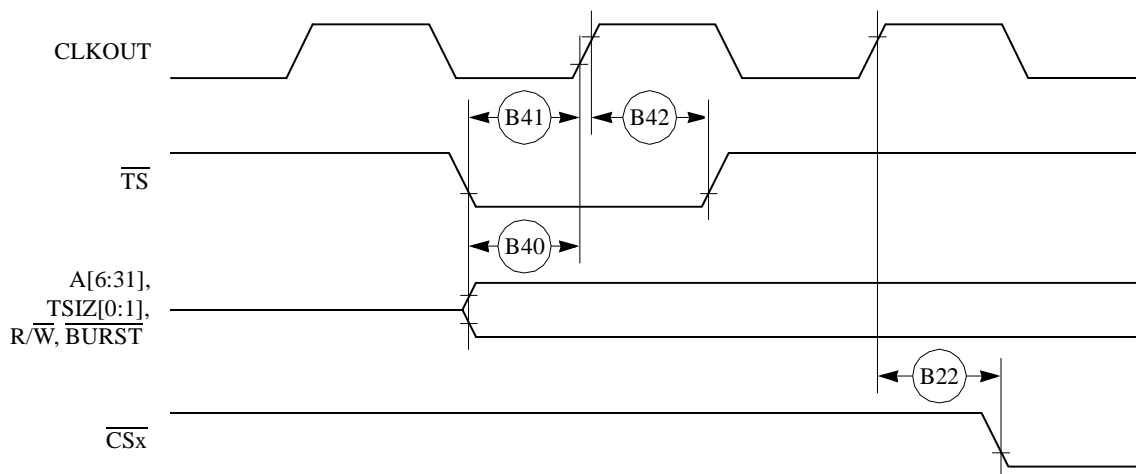


Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.

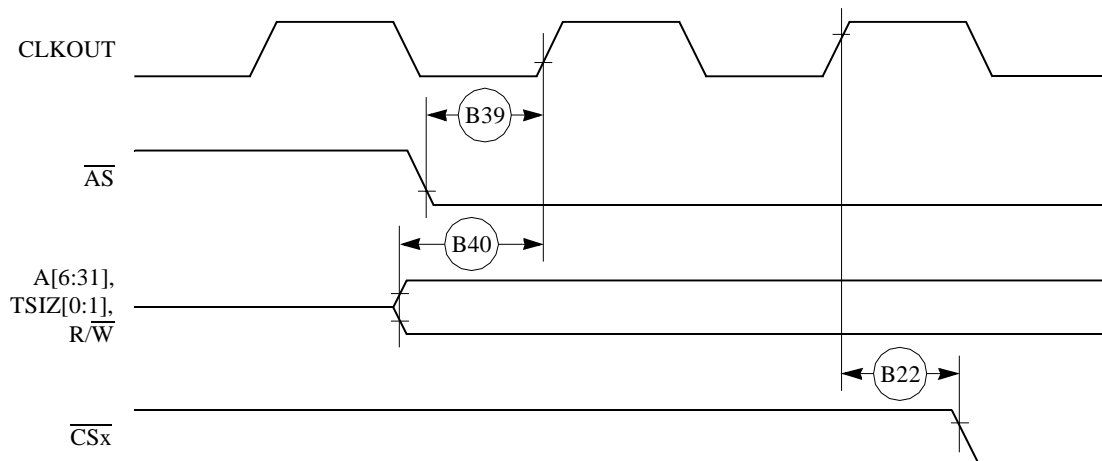


Figure 20. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 21 provides the timing for the asynchronous external master control signals negation.

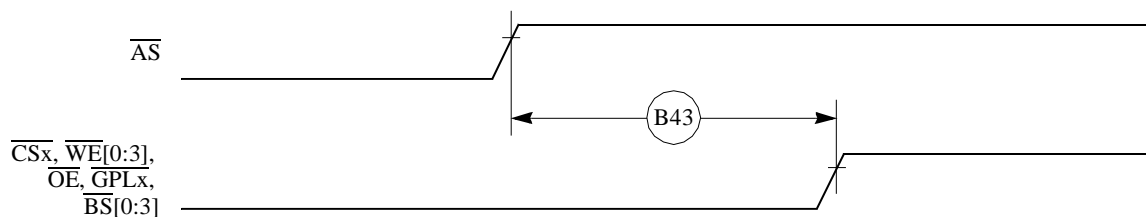


Figure 21. Asynchronous External Master—Control Signals Negation Timing

Figure 24 provides the PCMCIA access cycle timing for the external bus read.

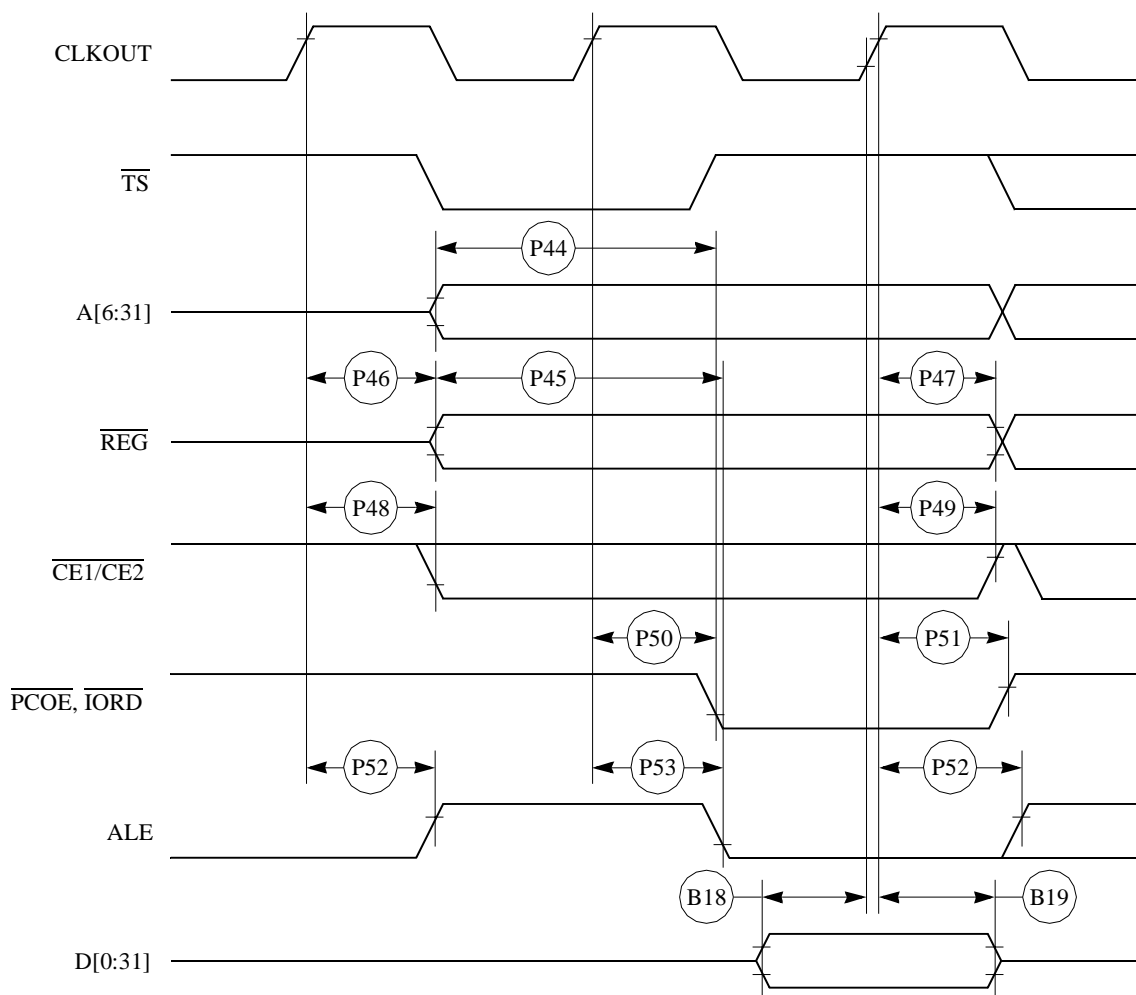


Figure 24. PCMCIA Access Cycles Timing External Bus Read

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

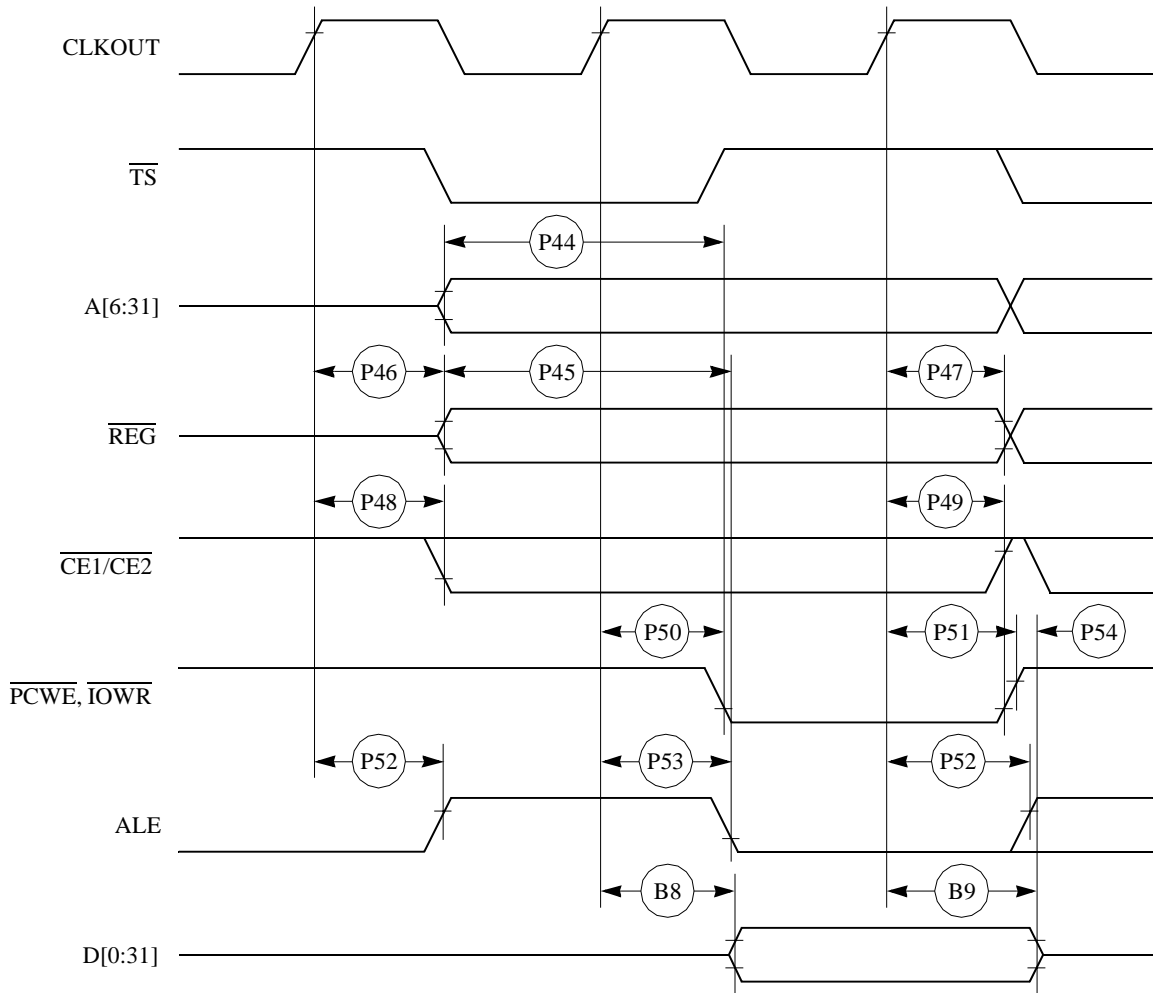


Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.

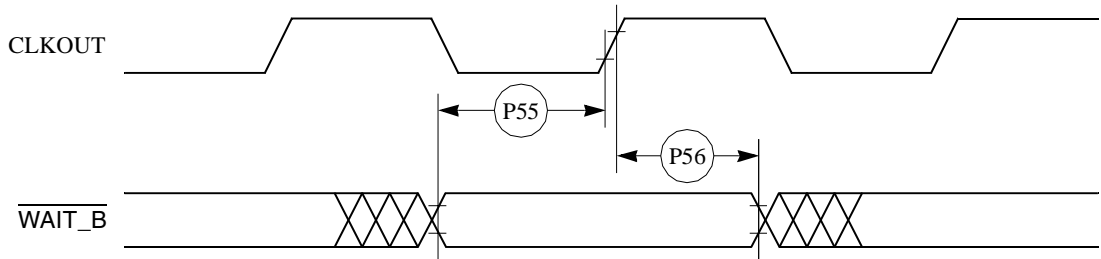


Figure 26. PCMCIA $\overline{\text{WAIT}}$ Signal Detection Timing

Table 9 shows the PCMCIA port timing for the MPC850.

Table 9. PCMCIA Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive ¹	18.00	—	26.00	—	22.00	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	ns

¹ OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

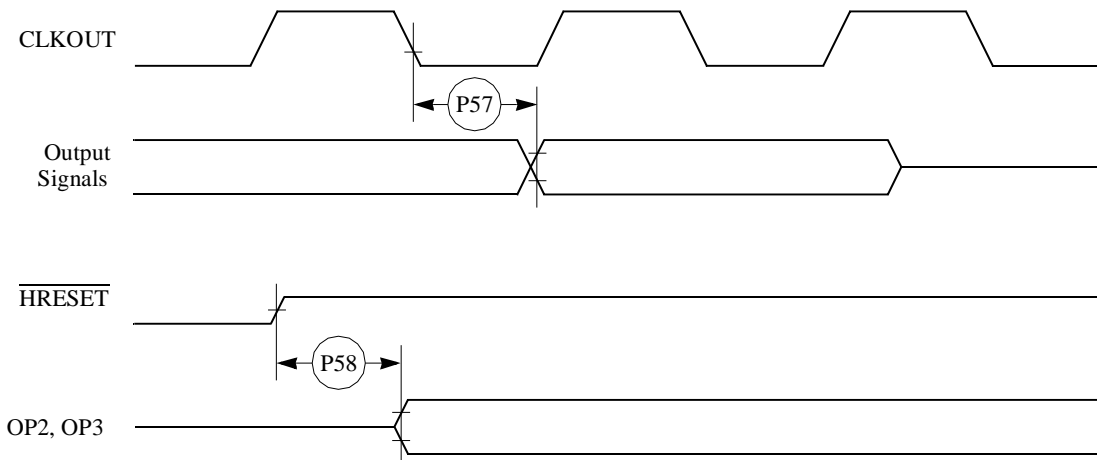


Figure 27. PCMCIA Output Port Timing

Figure 28 provides the PCMCIA output port timing for the MPC850.

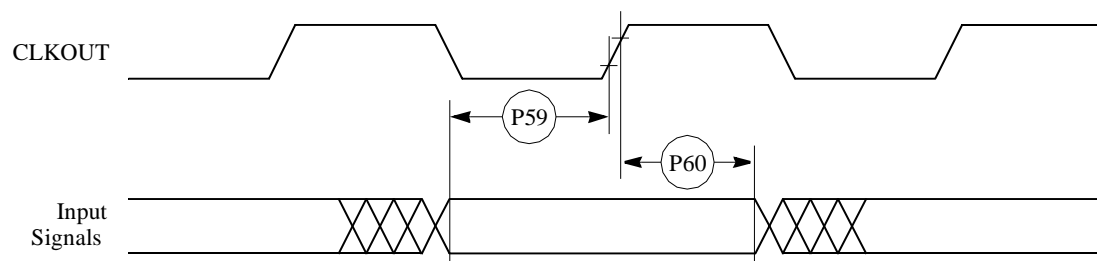


Figure 28. PCMCIA Input Port Timing

Table 10 shows the debug port timing for the MPC850.

Table 10. Debug Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
D61	DSCK cycle time	60.00	—	91.00	—	75.00	—	ns
D62	DSCK clock pulse width	25.00	—	38.00	—	31.00	—	ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	8.00	—	8.00	—	ns
D65	DSDI data hold time	5.00	—	5.00	—	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	0.00	2.00	ns

Figure 29 provides the input timing for the debug port clock.

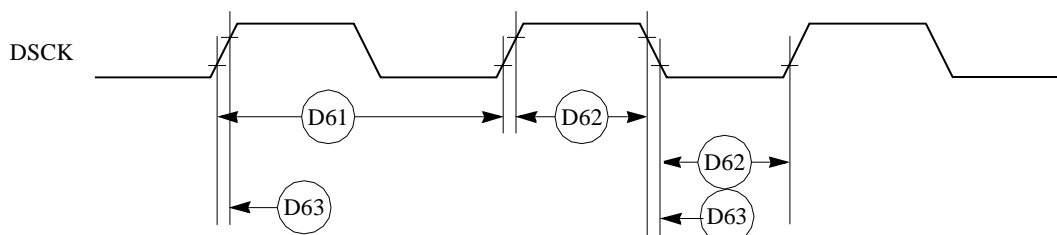


Figure 29. Debug Port Clock Input Timing

Figure 30 provides the timing for the debug port.

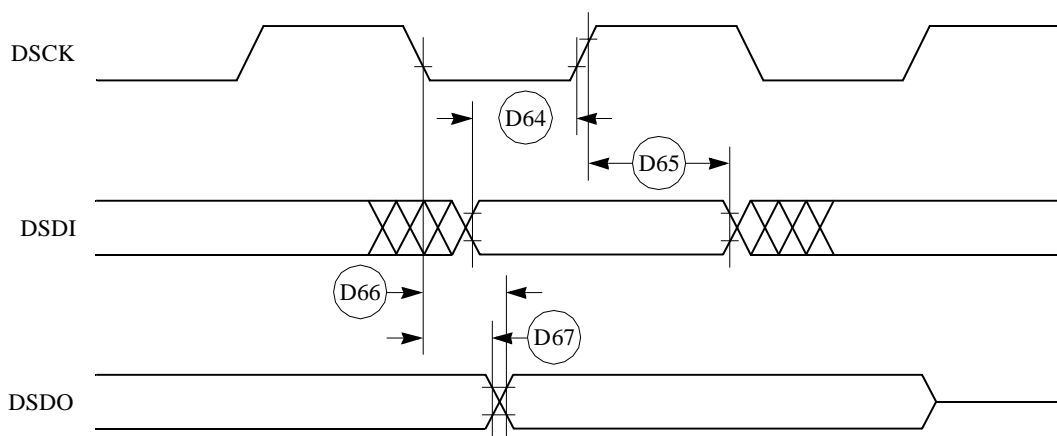


Figure 30. Debug Port Timings

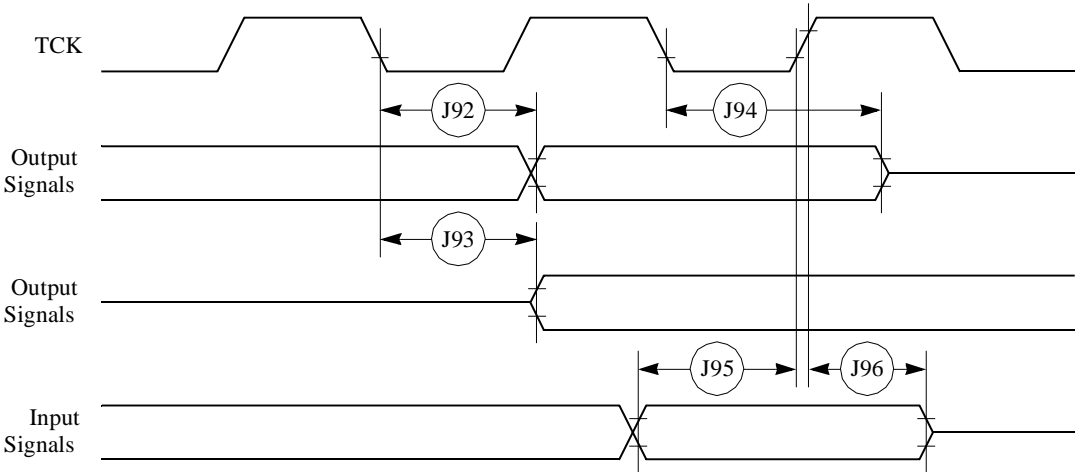


Figure 37. Boundary Scan (JTAG) Timing Diagram

8 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC850.

8.1 PIO AC Electrical Specifications

Table 13 provides the parallel I/O timings for the MPC850 as shown in Figure 38.

Table 13. Parallel I/O Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	—	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns

8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns

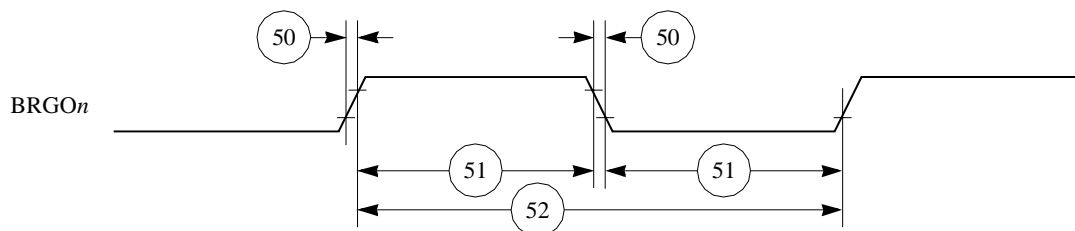


Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Table 16. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/TGATE rise and fall time	10.00	—	ns
62	TIN/TGATE low time	1.00	—	clk
63	TIN/TGATE high time	2.00	—	clk
64	TIN/TGATE cycle time	3.00	—	clk
65	CLKO high to TOUT valid	3.00	25.00	ns

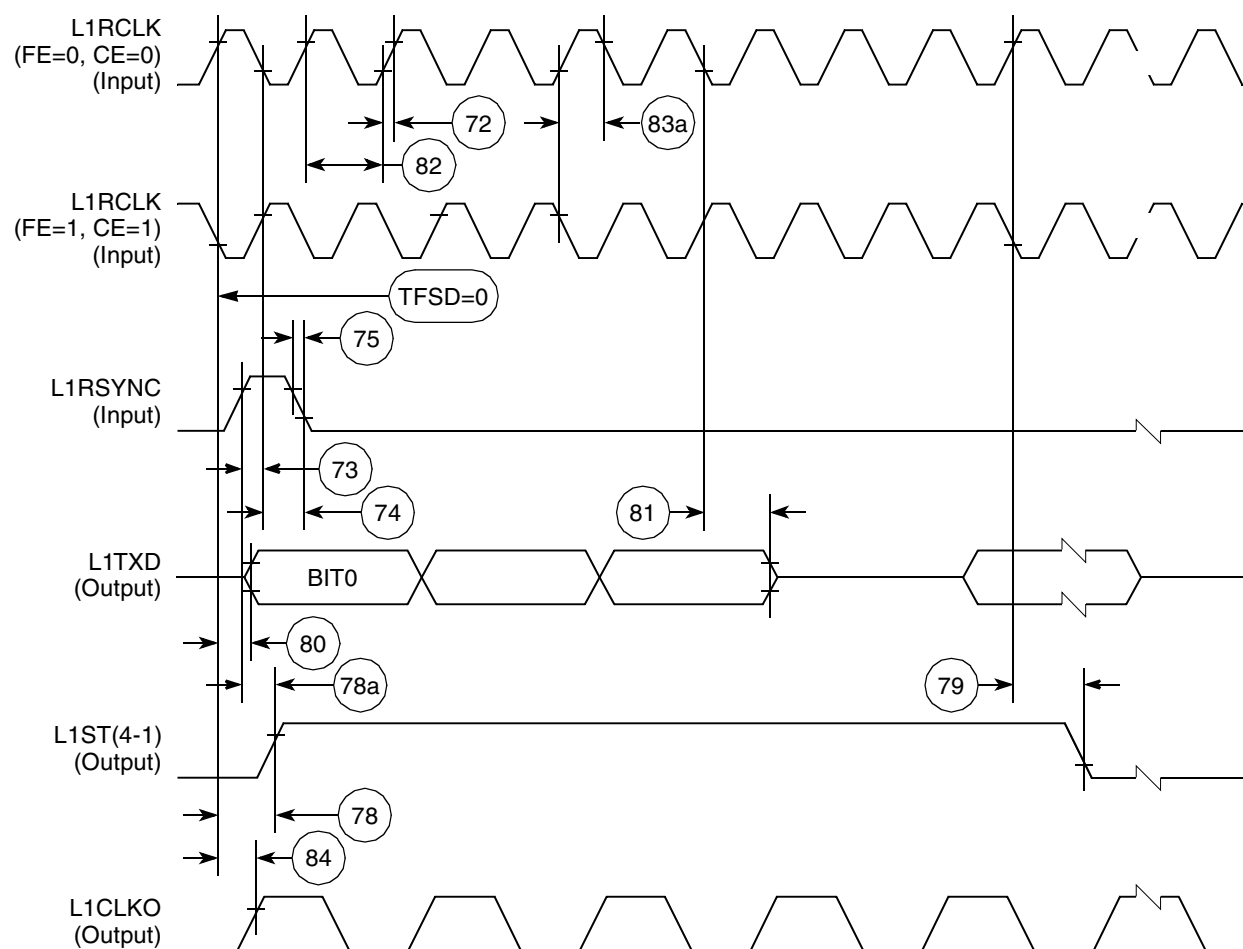
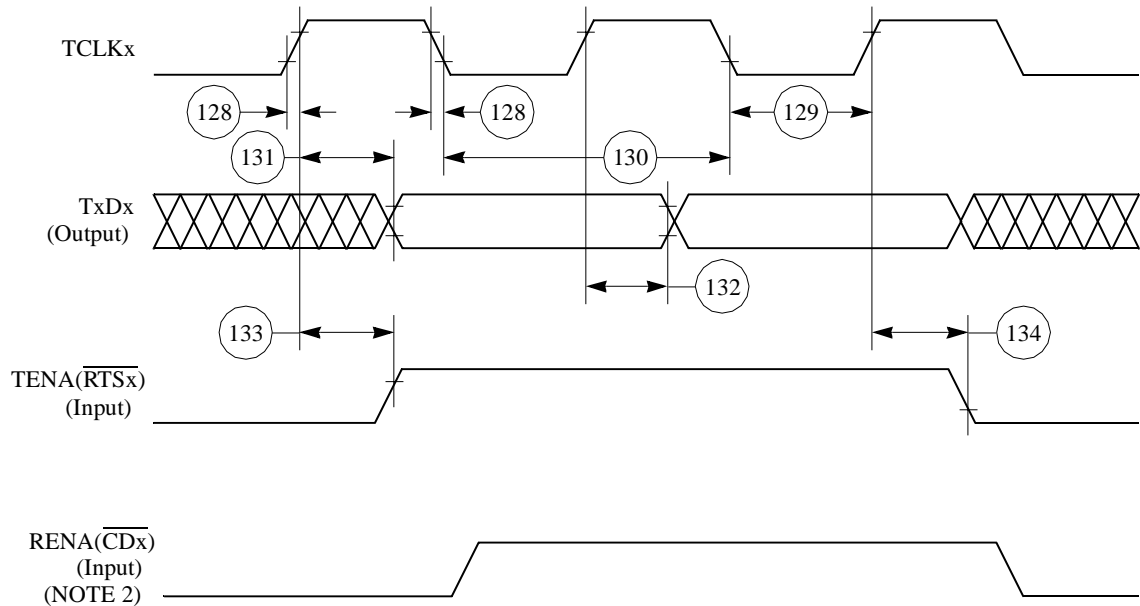


Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)



- NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
 2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 55. Ethernet Transmit Timing Diagram

8.8 SMC Transparent AC Electrical Specifications

Figure 21 provides the SMC transparent timings as shown in Figure 56.

Table 21. Serial Management Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
150	SMCLKx clock period ¹	100.00	—	ns
151	SMCLKx width low	50.00	—	ns
151a	SMCLKx width high	50.00	—	ns
152	SMCLKx rise/fall time	—	15.00	ns
153	SMTXDx active delay (from SMCLKx falling edge)	10.00	50.00	ns
154	SMRXDx/SMSYNx setup time	20.00	—	ns
155	SMRXDx/SMSYNx hold time	5.00	—	ns

¹ The ratio SyncCLK/SMCLKx must be greater or equal to 2/1.

PC14	PB28	PB27	PC12	TCK	PB24	PB23	PA8	PA7	VDDL	PA5	PC7	PC4	PD14	PD10	PD8	U
PC15	PA14	PA13	PA12	TMS	TDI	PC11	PB22	PC9	PB19	PA4	PB16	PD15	PD12	PD7	PD6	T
PA15	PB30	PB29	PC13	PB26	TRST	N/C	PC10	PA6	PB18	PC5	PD13	PD9	PD4	PD5	N/C	R
A8	A7	PB31	N/C	TDO	PB25	PA9	N/C	PC8	PB17	PC6	PD11	PD3	IRQ7	IRQ1	IRQ0	P
A11	A9	A12	A6									D12	D13	D8	D0	N
A15	A14	A13	A10									D23	D27	D4	D1	M
A27	A19	A16	A17									D17	D10	D9	D11	L
VDDL	A20	A21	N/C					GND				D15	D14	D2	D3	K
A29	A23	A25	A24									D22	D18	D16	D5	J
A28	A30	A22	A18									D25	D20	D19	VDDL	H
A31	TSIZ0	A26	WE3									D28	D24	D21	D6	G
WE1	TSIZ1	N/C	GPLA0								VDDH	D26	D31	D29	D7	F
WE0	WE2	GPLA3	CS5	CS0	GPLA4	TS	IRQ2	IPB7	IPB2	MODCK1	TEXP	DP1	DP2	D30	CLKOUT	E
GPLA1	GPLA2	CS6	WR	GPLA5	TEA	BG	IPB5	IPB1	IPB6	N/C	RSTCONFWAITB	DP0	DP3	N/C		D
CS4	CS7	CS2	GPLB4	BI	BR	BURST	IPB4	ALEB	IRQ4	MODCK	JRESE	JRESE	TPORESETXFC		VDDSYN	C
N/C	CS3	CS1	BDIP	TA	BB	IRQ6	IPB3	IPB0	VDDL	EXTCLK	XTAL	XTAL	KAPWRSSSYN	SSSYN		B
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	

Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

Figure 64 shows the non-JEDEC package dimensions of the PBGA.

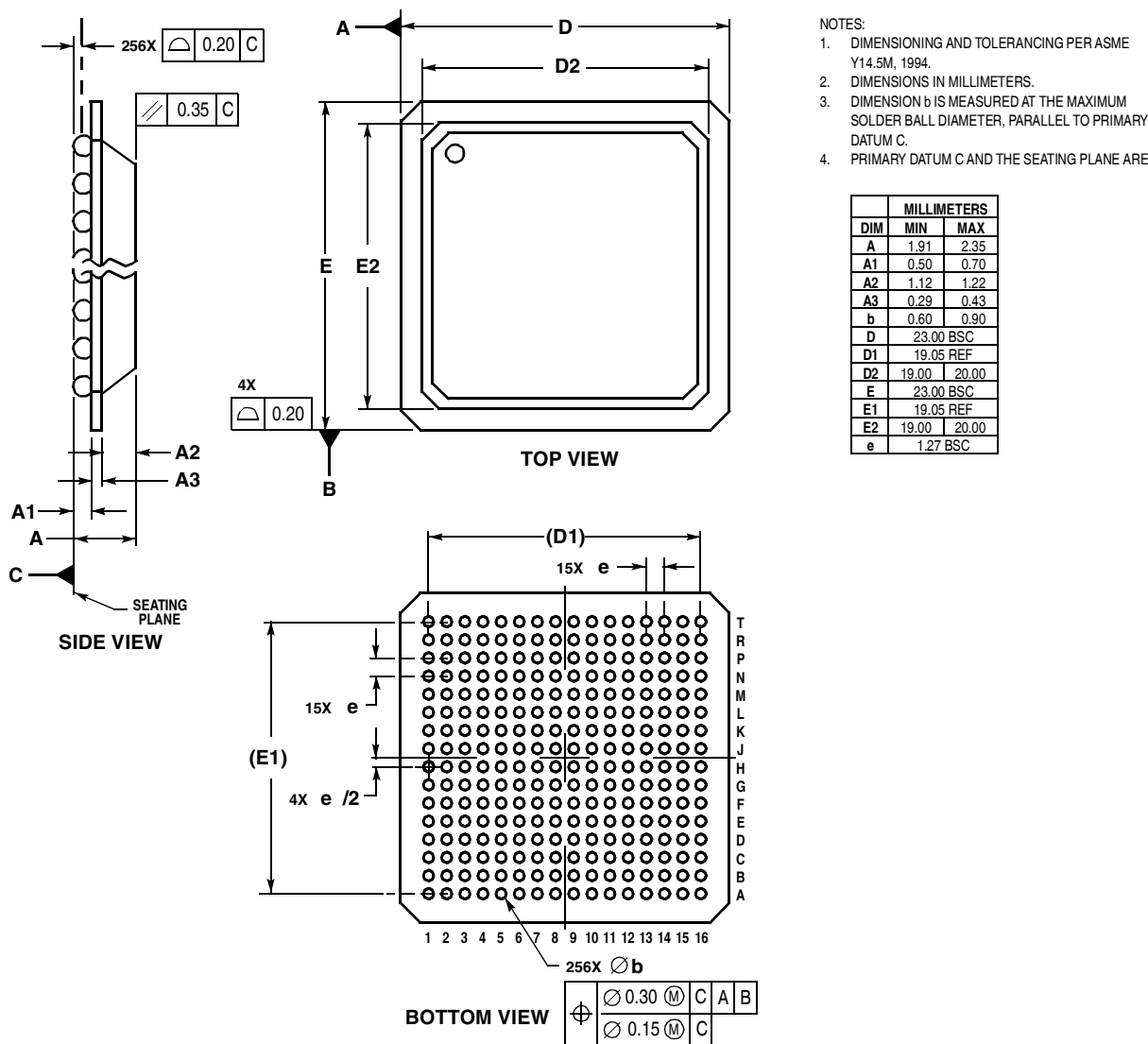


Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)—non-JEDEC Standard

Figure 65 shows the JEDEC package dimensions of the PBGA.

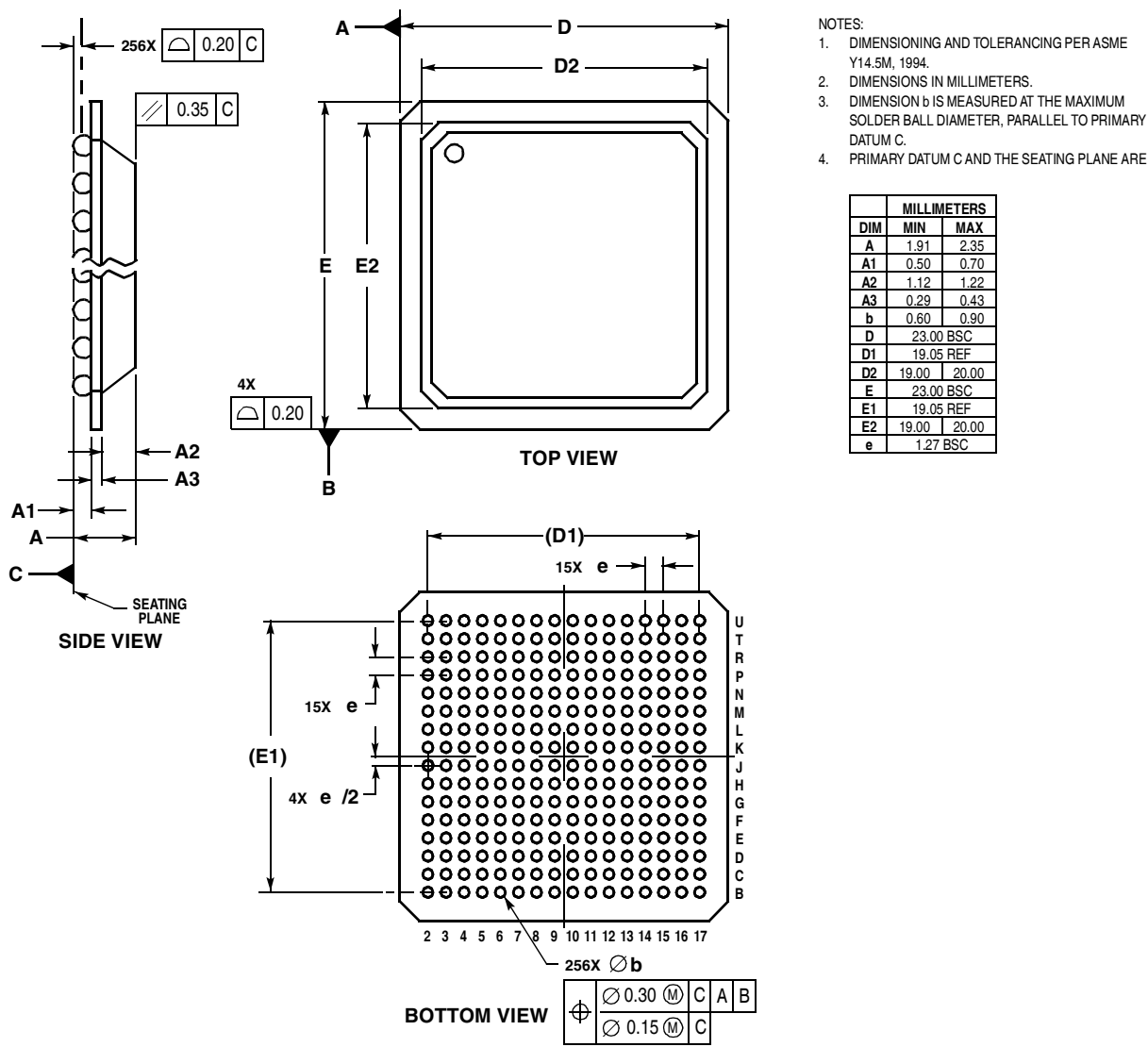


Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard

10 Document Revision History

Table 28 lists significant changes between revisions of this document.

Table 28. Document Revision History

Revision	Date	Change
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.
0.2	04/2002	Updated power numbers and added Rev. C
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.

How to Reach Us:

Home Page:

www.freescale.com

email:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2005.