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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850dslzt50bu

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



NP,

2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:



Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
 - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution



Features

- 2-Kbyte instruction cache and 1-Kbyte data cache (Harvard architecture)
 - Caches are two-way, set-associative
 - Physically addressed
 - Cache blocks can be updated with a 4-word line burst
 - Least-recently used (LRU) replacement algorithm
 - Lockable one-line granularity
- Memory management units (MMUs) with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
- MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and eight protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8, 16, and 32-bit buses
 - Supports traditional 68000 big-endian, traditional x86 little-endian and modified little-endian memory systems
 - Twenty-six external address lines
- Completely static design (0–80 MHz operation)
- System integration unit (SIU)
 - Hardware bus monitor
 - Spurious interrupt monitor
 - Software watchdog
 - Periodic interrupt timer
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer, time base, and real-time clock (RTC) from the PowerPC architecture
 - Reset controller
 - IEEE 1149.1 test access port (JTAG)
- Memory controller (eight banks)
 - Glueless interface to DRAM single in-line memory modules (SIMMs), synchronous DRAM (SDRAM), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), flash EPROM, etc.
 - Memory controller programmable to support most size and speed memory interfaces
 - Boot chip-select available at reset (options for 8, 16, or 32-bit memory)
 - Variable block sizes, 32 Kbytes to 256 Mbytes
 - Selectable write protection
 - On-chip bus arbiter supports one external bus master
 - Special features for burst mode support
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers





- Interrupt can be masked on reference match and event capture
- Interrupts
 - Eight external interrupt request (IRQ) lines
 - Twelve port pins with interrupt capability
 - Fifteen internal interrupt sources
 - Programmable priority among SCCs and USB
 - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
 - Master (socket) interface, release 2.1 compliant
 - Single PCMCIA socket
 - Supports eight memory or I/O windows
- Communications processor module (CPM)
 - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
 - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 8 Kbytes of dual-port RAM
 - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
 - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
 - Can be connected to any SCC, SMC, or USB
 - Allow changes during operation
 - Autobaud support option
- Two SCCs (serial communications controllers)
 - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
 - HDLC/SDLCTM (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support PPP (point-to-point protocol)
 - AppleTalk[®]
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))

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Table 6.	Bus	Operation	Timing	1
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Num	Chavastavistis	50 I	MHz	66 I	MHz	80 MHz		FEACT	Cap Load	l lm it
NUM	Characteristic	Min	Мах	Min	Max	Min	Мах	FFACI	50 pF)	Unit
B1	CLKOUT period	20	_	30.30	—	25	—	—		ns
B1a	EXTCLK to CLKOUT phase skew (EXTCLK > 15 MHz and MF <= 2)	-0.90	0.90	-0.90	0.90	-0.90	0.90	—	50.00	ns
B1b	EXTCLK to CLKOUT phase skew (EXTCLK > 10 MHz and MF < 10)	-2.30	2.30	-2.30	2.30	-2.30	2.30	_	50.00	ns
B1c	CLKOUT phase jitter (EXTCLK > 15 MHz and MF <= 2) 2	-0.60	0.60	-0.60	0.60	-0.60	0.60	—	50.00	ns
B1d	CLKOUT phase jitter ²	-2.00	2.00	-2.00	2.00	-2.00	2.00	—	50.00	ns
B1e	CLKOUT frequency jitter (MF < 10) ²	—	0.50	—	0.50	_	0.50	_	50.00	%
B1f	CLKOUT frequency jitter (10 < MF < 500) ²	—	2.00	—	2.00	_	2.00	—	50.00	%
B1g	CLKOUT frequency jitter (MF > 500) ²	_	3.00	—	3.00	_	3.00	_	50.00	%
B1h	Frequency jitter on EXTCLK ³	—	0.50	—	0.50	—	0.50	—	50.00	%
B2	CLKOUT pulse width low	8.00	_	12.12	—	10.00	_	—	50.00	ns
B3	CLKOUT width high	8.00	_	12.12	_	10.00	_	—	50.00	ns
B4	CLKOUT rise time	_	4.00	_	4.00	—	4.00	—	50.00	ns
B5	CLKOUT fall time	—	4.00	_	4.00	—	4.00	—	50.00	ns
B7	CLKOUT to A[6–31], RD/WR, BURST, D[0–31], DP[0–3] invalid	5.00		7.58	_	6.25	_	0.250	50.00	ns
B7a	CLKOUT to TSIZ[0–1], REG, RSV, AT[0–3], BDIP, PTR invalid	5.00		7.58	—	6.25	—	0.250	50.00	ns
B7b	CLKOUT to BR, BG, FRZ, VFLS[0–1], VF[0–2] IWP[0–2], LWP[0–1], STS invalid ⁴	5.00	_	7.58	—	6.25	—	0.250	50.00	ns
B8	CLKOUT to A[6–31], RD/WR, BURST, D[0–31], DP[0–3] valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8a	CLKOUT to TSIZ[0-1], REG, RSV, AT[0-3] BDIP, PTR valid	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B8b	CLKOUT to BR, BG, VFLS[0–1], VF[0–2], IWP[0–2], FRZ, LWP[0–1], STS valid ⁴	5.00	11.74	7.58	14.33	6.25	13.00	0.250	50.00	ns



Num	um Characteristic		50 MHz		66 MHz		80 MHz		Cap Load	lleit
NUM	Characteristic	Min	Max	Min	Мах	Min	Max	FFACI	50 pF)	Unit
B22	CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = 0,1	—	8.00	—	8.00	—	8.00	—	50.00	ns
B22b	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	_	50.00	ns
B24	A[6-31] to \overline{CS} asserted GPCM ACS = 10, TRLX = 0.	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B24a	A[6–31] to \overline{CS} asserted GPCM ACS = 11, TRLX = 0	8.00	_	13.00	_	11.00	_	0.500	50.00	ns
B25	CLKOUT rising edge to \overline{OE} , WE[0-3] asserted	—	9.00	—	9.00	_	9.00	—	50.00	ns
B26	CLKOUT rising edge to OE negated	2.00	9.00	2.00	9.00	2.00	9.00	—	50.00	ns
B27	A[6-31] to \overline{CS} asserted GPCM ACS = 10, TRLX = 1	23.00	_	36.00	—	29.00	_	1.250	50.00	ns
B27a	A[6–31] to \overline{CS} asserted GPCM ACS = 11, TRLX = 1	28.00	—	43.00	—	36.00	_	1.500	50.00	ns
B28	CLKOUT rising edge to WE[0–3] negated GPCM write access CSNT = 0	—	9.00	_	9.00	—	9.00	—	50.00	ns
B28a	$\frac{CLKOUT}{WE[0-3]}$ negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	_	12.00		14.00		13.00	0.250	50.00	ns

Table 6.	Bus O	peration	Timing	1	(continued)
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Niumo	m Charaotoristia		50 MHz		66 MHz		80 MHz		Cap Load	l lm it
NUM	Characteristic	Min	Max	Min	Max	Min	Max	FFACI	50 pF)	Unit
B33a	CLKOUT rising edge to GPL valid - as requested by control bit GxT3 in the corresponding word in the UPM	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B34	A[6–31] and D[0–31] to CS valid - as requested by control bit CST4 in the corresponding word in the UPM	3.00	_	6.00	_	4.00	_	0.250	50.00	ns
B34a	A[6–31] and D[0–31] to CS valid - as requested by control bit CST1 in the corresponding word in the UPM	8.00	_	13.00	_	11.00	_	0.500	50.00	ns
B34b	A[6–31] and D[0–31] to CS valid - as requested by CST2 in the corresponding word in UPM	13.00	—	21.00	—	17.00		0.750	50.00	ns
B35	A[6-31] to \overline{CS} valid - as requested by control bit BST4 in the corresponding word in UPM	3.00	—	6.00	—	4.00		0.250	50.00	ns
B35a	A[6–31] and D[0–31] to BS valid - as requested by BST1 in the corresponding word in the UPM	8.00	_	13.00	—	11.00		0.500	50.00	ns
B35b	A[6–31] and D[0–31] to BS valid - as requested by control bit BST2 in the corresponding word in the UPM	13.00	_	21.00	_	17.00	_	0.750	50.00	ns
B36	A[6–31] and D[0–31] to GPL valid - as requested by control bit GxT4 in the corresponding word in the UPM	3.00	_	6.00	_	4.00	_	0.250	50.00	ns
B37	UPWAIT valid to CLKOUT falling edge 10	6.00	_	6.00	_	6.00	_	_	50.00	ns
B38	CLKOUT falling edge to UPWAIT valid ¹⁰	1.00	—	1.00	—	1.00	—	—	50.00	ns
B39	AS valid to CLKOUT rising edge	7.00	—	7.00	—	7.00	—	_	50.00	ns
B40	A[6-31], TSIZ[0-1], RD/WR, BURST, valid to CLKOUT rising edge.	7.00	—	7.00	—	7.00	—	—	50.00	ns
B41	TS valid to CLKOUT rising edge (setup time)	7.00		7.00		7.00	-	_	50.00	ns





Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)



Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)







Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)



Bus Signal Timing



Figure 19 provides the timing for the synchronous external master access controlled by the GPCM.

Figure 19. Synchronous External Master Access Timing (GPCM Handled ACS = 00)

Figure 20 provides the timing for the asynchronous external master memory access controlled by the GPCM.





Figure 21 provides the timing for the asynchronous external master control signals negation.



Figure 21. Asynchronous External Master—Control Signals Negation Timing



IEEE 1149.1 Electrical Specifications



Figure 34. JTAG Test Clock Input Timing



Figure 35. JTAG Test Access Port Timing Diagram



Figure 36. JTAG TRST Timing Diagram



CPM Electrical Characteristics



Figure 41. SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock







CPM Electrical Characteristics



Figure 47. SI Transmit Timing Diagram



CPM Electrical Characteristics



Figure 48. SI Transmit Timing with Double Speed Clocking (DSC = 1)



CPM Electrical Characteristics

Figure 50 through Figure 52 show the NMSI timings.





Num	Charactoristic	All Free	luencies	Unit
	Characteristic	Min	Мах	Omi
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to SDACK asserted ²	_	20.00	ns
139	CLKOUT low to SDACK negated ²	_	20.00	ns

Table 20. Ethernet Timing (continued)

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

² SDACK is asserted whenever the SDMA writes the incoming frame destination address into memory.



Figure 53. Ethernet Collision Timing Diagram



Figure 54. Ethernet Receive Timing Diagram





8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

Table 23. SPI Slave Timing

Num	Characteristic	All Frequ	Unit	
Nulli	Characteristic	Min	Max	Onit
170	Slave cycle time	2	—	t _{cyc}
171	Slave enable lead time	15.00	_	ns
172	Slave enable lag time	15.00	_	ns
173	Slave clock (SPICLK) high or low time	1	_	t _{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	_	t _{cyc}
175	Slave data setup time (inputs)	20.00	—	ns
176	Slave data hold time (inputs)	20.00	—	ns
177	Slave access time	_	50.00	ns
178	Slave SPI MISO disable time	_	50.00	ns
179	Slave data valid (after SPICLK edge)	_	50.00	ns
180	Slave data hold time (outputs)	0.00	_	ns
181	Rise time (input)	_	15.00	ns
182	Fall time (input)	_	15.00	ns



9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivativ

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

 Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support



Mechanical Data and Ordering Information

customers that are currently using the non-JEDEC pin numbering scheme, two sets of pinouts, JEDEC and non-JEDEC, are presented in this document.

Figure 62 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface.



Figure 62. Pin Assignments for the PBGA (Top View)—non-JEDEC Standard



Document Revision History

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