E·XFL



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850srvr50bu

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview

The CPM of the MPC850 supports up to seven serial channels, as follows:

- One or two serial communications controllers (SCCs). The SCCs support Ethernet, ATM (MPC850SR and MPC850DSL), HDLC and a number of other protocols, along with a transparent mode of operation.
- One USB channel
- Two serial management controllers (SMCs)
- One I²C port
- One serial peripheral interface (SPI).

Table 1 shows the functionality supported by the members of the MPC850 family.

Part	Number of SCCs Supported	Ethernet Support	ATM Support	USB Support	Multi-channel HDLC Support	Number of PCMCIA Slots Supported
MPC850	1	Yes	-	Yes	-	1
MPC850DE	2	Yes	-	Yes	-	1
MPC850SR	2	Yes	Yes	Yes	Yes	1
MPC850DSL	2	Yes	Yes	Yes	No	1

Table 1. MPC850 Functionality Matrix

Additional documentation may be provided for parts listed in Table 1.



NP,

2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:



Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
 - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution





- Interrupt can be masked on reference match and event capture
- Interrupts
 - Eight external interrupt request (IRQ) lines
 - Twelve port pins with interrupt capability
 - Fifteen internal interrupt sources
 - Programmable priority among SCCs and USB
 - Programmable highest-priority request
- Single socket PCMCIA-ATA interface
 - Master (socket) interface, release 2.1 compliant
 - Single PCMCIA socket
 - Supports eight memory or I/O windows
- Communications processor module (CPM)
 - 32-bit, Harvard architecture, scalar RISC communications processor (CP)
 - Protocol-specific command sets (for example, GRACEFUL STOP TRANSMIT stops transmission after the current frame is finished or immediately if no frame is being sent and CLOSE RXBD closes the receive buffer descriptor)
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 8 Kbytes of dual-port RAM
 - Twenty serial DMA (SDMA) channels for the serial controllers, including eight for the four USB endpoints
 - Three parallel I/O registers with open-drain capability
- Four independent baud-rate generators (BRGs)
 - Can be connected to any SCC, SMC, or USB
 - Allow changes during operation
 - Autobaud support option
- Two SCCs (serial communications controllers)
 - Ethernet/IEEE 802.3, supporting full 10-Mbps operation
 - HDLC/SDLCTM (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support PPP (point-to-point protocol)
 - AppleTalk[®]
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))





- Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
- Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface

(GND = 0V)

- Eight comparators: four operate on instruction address, two operate on data address, and two
 operate on data
- The MPC850 can compare using the =, \neq , <, and > conditions to generate watchpoints
- Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility on all general purpose I/O pins.

3 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC850. Table 2 provides the maximum ratings.

Rating	Symbol	Value	Unit
Supply voltage	VDDH	-0.3 to 4.0	V
	VDDL	-0.3 to 4.0	V
	KAPWR	-0.3 to 4.0	V
	VDDSYN	-0.3 to 4.0	V
Input voltage ¹	V _{in}	GND-0.3 to VDDH + 2.5 V	V
Junction temperature ²	Тј	0 to 95 (standard) -40 to 95 (extended)	°C
Storage temperature range	T _{stg}	-55 to +150	°C

¹ Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. CAUTION: All inputs that tolerate 5 V cannot be more than 2.5 V greater than the supply voltage. This restriction

applies to power-up and normal operation (that is, if the MPC850 is unpowered, voltage greater than 2.5 V must not be applied to its inputs).

² The MPC850, a high-frequency device in a BGA package, does not provide a guaranteed maximum ambient temperature. Only maximum junction temperature is guaranteed. It is the responsibility of the user to consider power dissipation and thermal management. Junction temperature ratings are the same regardless of frequency rating of the device.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}). Table 3 provides the package thermal characteristics for the MPC850.



Thermal Characteristics

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA ¹	θ_{JA}	40 ²	°C/W
	θ_{JA}	31 ³	°C/W
	θ_{JA}	24 ⁴	°C/W
Thermal Resistance for BGA (junction-to-case)	θ _{JC}	8	°C/W

¹ For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

² Assumes natural convection and a single layer board (no thermal vias).

³ Assumes natural convection, a multilayer board with thermal vias⁴, 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

⁴ Assumes natural convection, a multilayer board with thermal vias⁴, 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

 $\begin{aligned} T_J &= T_A + (P_D \bullet \theta_{JA}) \\ P_D &= (V_{DD} \bullet I_{DD}) + P_{I/O} \\ \text{where:} \end{aligned}$

 $P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical ¹	Maximum ²	Unit
Power Dissipation	33	TBD	515	mW
All Revisions	40	TBD	590	mW
	50	TBD	725	mW

¹ Typical power dissipation is measured at 3.3V

² Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V



Bus Signal Timing

Num	Chavastavistis	50 I	MHz	66 I	MHz	80 I	MHz	FFACT	Cap Load	llmit
NUM	Characteristic	Min	Мах	Min	Max	Min	Мах	FFACI	50 pF)	Unit
B28c	CLKOUT falling edge to WE[0-3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	_	14.00	_	18.00		16.00	0.375	50.00	ns
B29	$\overline{WE[0-3]}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, CSNT = 0	3.00		6.00	—	4.00		0.250	50.00	ns
B29a	WE[0-3] negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	_	13.00	_	11.00		0.500	50.00	ns
B29b	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	_	6.00	_	4.00	_	0.250	50.00	ns
B29c	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	_	13.00		11.00		0.500	50.00	ns
B29d	$\overline{WE[0-3]}$ negated to D[0-31], DP[0-3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	_	43.00	_	36.00		1.500	50.00	ns
B29e	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	_	43.00	_	36.00		1.500	50.00	ns
B29f	WE[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	_	9.00		7.00		0.375	50.00	ns
B29g	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	_	9.00		7.00		0.375	50.00	ns

Table 6.	Bus O	peration	Timing	1	(continued)
----------	-------	----------	--------	---	-------------



Figure 6 provides the timing for the synchronous input signals.



Figure 6. Synchronous Input Signals Timing

Figure 7 provides normal case timing for input data.



Figure 7. Input Data Timing in Normal Case





Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)



Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)



Bus Signal Timing

Figure 25 provides the PCMCIA access cycle timing for the external bus write.



Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.



Figure 26. PCMCIA WAIT Signal Detection Timing







Figure 37. Boundary Scan (JTAG) Timing Diagram

8 **CPM Electrical Characteristics**

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC850.

8.1 PIO AC Electrical Specifications

Table 13 provides the parallel I/O timings for the MPC850 as shown in Figure 38.

Table 13. Parallel I/O Timing

Num	Characteristic	All Freque	Unit	
Num	Characteristic		Max	onit
29	Data-in setup time to clock high	15	—	ns
30	Data-in hold time from clock high	7.5	_	ns
31	Clock low to data-out valid (CPU writes data, control, or direction)	—	25	ns





Figure 40. SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock



CPM Electrical Characteristics



Figure 41. SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock





	Table 17. SI Timing (cont	inued)		
	Oh ann a thurin tha	All Fre	quencies	11
NUM	Characteristic	Min	Мах	Unit
82	L1RCLK, L1TCLK frequency (DSC =1)	_	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83A	L1RCLK, L1TCLK width high (DSC = 1) ³	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)		30.00	ns
85	L1RQ valid before falling edge of L1TSYNC ⁴	1.00	—	L1TCLK
86	L1GR setup time ²	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	_	0.00	ns

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

- 2 These specs are valid for IDL mode only.
- ³ Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.







CPM Electrical Characteristics

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

	Table 18.	NMSI	External	Clock	Timing
--	-----------	------	----------	-------	--------

Num	Characteristic	All Frequencies Min Max		Unit	
Num	Characteristic			Unit	
100	RCLKx and TCLKx frequency 1 (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns	
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns	
102	RCLKx and TCLKx rise/fall time	—	15.00	ns	
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns	
104	RTSx active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns	
105	CTSx setup time to TCLKx rising edge	5.00	—	ns	
106	RXDx setup time to RCLKx rising edge	5.00	—	ns	
107	RXDx hold time from RCLKx rising edge ²	5.00	—	ns	
108	CDx setup time to RCLKx rising edge	5.00	—	ns	

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Charactoristic	All Fr	equencies	Unit		
Num	Characteristic	Min	Мах	< 0mit		
100	RCLKx and TCLKx frequency 1 (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz		
102	RCLKx and TCLKx rise/fall time	_	—	ns		
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns		
104	RTSx active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns		
105	CTSx setup time to TCLKx rising edge	40.00	—	ns		
106	RXDx setup time to RCLKx rising edge	40.00	—	ns		
107	RXDx hold time from RCLKx rising edge ²	0.00	—	ns		
108	CDx setup time to RCLKx rising edge	40.00		ns		

¹ The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

² Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.



CPM Electrical Characteristics

Figure 50 through Figure 52 show the NMSI timings.





CPM Electrical Characteristics



Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Niumo	Chavastavistis	All Frequencies		11	
Num	Characteristic	Min	Max		
120	CLSN width high	40.00	_	ns	
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns	
122	RCLKx width low	40.00		ns	
123	RCLKx clock period ¹	80.00	120.00	ns	
124	RXDx setup time	20.00	_	ns	
125	RXDx hold time	5.00	_	ns	
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	-	ns	
127	RENA width low	100.00	-	ns	
128	TCLKx rise/fall time	—	15.00	ns	
129	TCLKx width low	40.00	_	ns	
130	TCLKx clock period ¹	99.00	101.00	ns	
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns	
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns	
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns	



9 Mechanical Data and Ordering Information

Table 26 provides information on the MPC850 derivative devices.

Table 26. MPC850 Family Derivativ

Device	Ethernet Support	Number of SCCs ¹	32-Channel HDLC Support	64-Channel HDLC Support ²
MPC850	N/A	One	N/A	N/A
MPC850DE	Yes	Two	N/A	N/A
MPC850SR	Yes	Two	N/A	Yes
MPC850DSL	Yes	Two	No	No

¹ Serial Communication Controller (SCC)

² 50 MHz version supports 64 time slots on a time division multiplexed line using one SCC

Table 27 identifies the packages and operating frequencies available for the MPC850.

 Table 27. MPC850 Package/Frequency/Availability

Package Type	Frequency (MHz)	Temperature (Tj)	Order Number
256-Lead Plastic Ball Grid Array (ZT suffix)	50	0°C to 95°C	XPC850ZT50BU XPC850DEZT50BU XPC850SRZT50BU XPC850DSLZT50BU
	66	0°C to 95°C	XPC850ZT66BU XPC850DEZT66BU XPC850SRZT66BU
	80	0°C to 95°C	XPC850ZT80BU XPC850DEZT80BU XPC850SRZT80BU
256-Lead Plastic Ball Grid Array (CZT suffix)	50	-40°C to 95°C	XPC850CZT50BU XPC850DECZT50BU XPC850SRCZT50BU XPC850DSLCZT50BU
	66		XPC850CZT66BU XPC850DECZT66BU XPC850SRCZT66BU
	80		XPC850CZT80B XPC850DECZT80B XPC850SRCZT80B

9.1 Pin Assignments and Mechanical Dimensions of the PBGA

The original pin numbering of the MPC850 conformed to a Freescale proprietary pin numbering scheme that has since been replaced by the JEDEC pin numbering standard for this package type. To support

Mechanical Data and Ordering Information

Figure 64 shows the non-JEDEC package dimensions of the PBGA.



Figure 64. Package Dimensions for the Plastic Ball Grid Array (PBGA)-non-JEDEC Standard



Document Revision History

10 Document Revision History

Table 28 lists significant changes between revisions of this document.

Table 28. Document Revision History

Revision	Date	Change
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.
0.2	04/2002	Updated power numbers and added Rev. C
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.



Document Revision History

THIS PAGE INTENTIONALLY LEFT BLANK