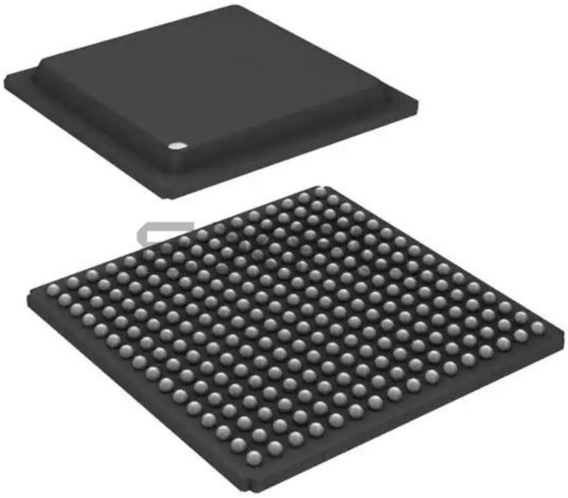
NXP USA Inc. - XPC850ZT50BU Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	50MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850zt50bu

2 Features

Figure 1 is a block diagram of the MPC850, showing its major components and the relationships among those components:

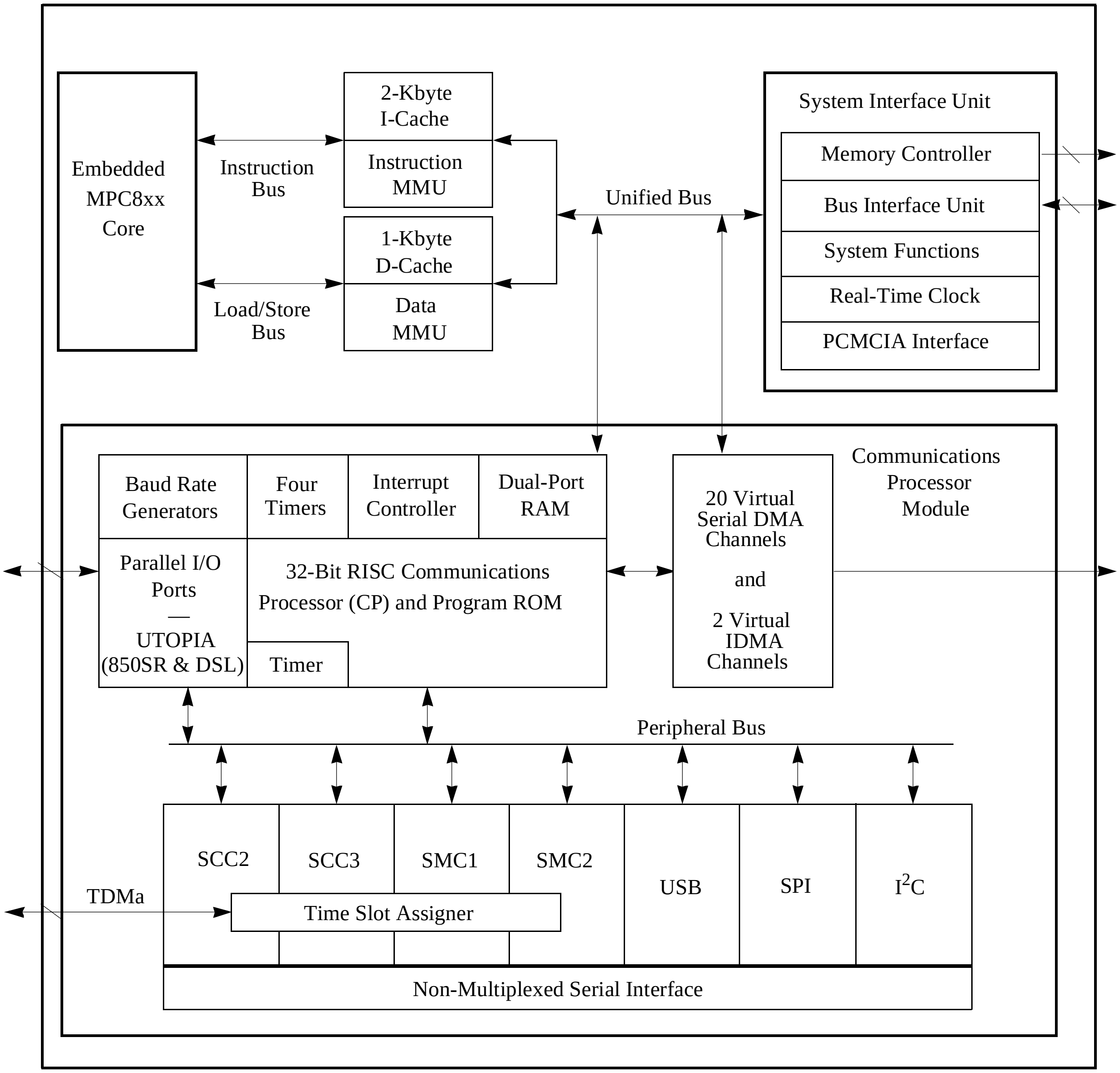


Figure 1. MPC850 Microprocessor Block Diagram

The following list summarizes the main features of the MPC850:

- Embedded single-issue, 32-bit MPC8xx core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA [1]	θ_{JA}	40 [2]	°C/W
	θ_{JA}	31 [3]	°C/W
	θ_{JA}	24 [4]	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

[1] For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

[2] Assumes natural convection and a single layer board (no thermal vias).

[3] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

[4] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

[1] Typical power dissipation is measured at 3.3V

[2] Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B22	CLKOUT rising edge to CS asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to CS asserted GPCM ACS = 10, TRLX = 0,1	—	8.00	—	8.00	—	8.00	—	50.00	ns
B22b	CLKOUT falling edge to CS asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to CS asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to CS negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	—	50.00	ns
B24	A[6–31] to CS asserted GPCM ACS = 10, TRLX = 0.	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B24a	A[6–31] to CS asserted GPCM ACS = 11, TRLX = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B25	CLKOUT rising edge to OE, WE[0–3] asserted	—	9.00	—	9.00	—	9.00	—	50.00	ns
B26	CLKOUT rising edge to OE negated	2.00	9.00	2.00	9.00	2.00	9.00	—	50.00	ns
B27	A[6–31] to CS asserted GPCM ACS = 10, TRLX = 1	23.00	—	36.00	—	29.00	—	1.250	50.00	ns
B27a	A[6–31] to CS asserted GPCM ACS = 11, TRLX = 1	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B28	CLKOUT rising edge to WE[0–3] negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	50.00	ns
B28a	CLKOUT falling edge to WE[0–3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to CS negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	—	12.00	—	14.00	—	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B28c	CLKOUT falling edge to WE[0–3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to CS negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	—	14.00	—	18.00	—	16.00	0.375	50.00	ns
B29	WE[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access, CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29a	WE[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29b	CS negated to D[0–31], DP[0–3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29c	CS negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29d	WE[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29e	CS negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29f	WE[0–3] negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns
B29g	CS negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B29h	$\overline{\text{WE}[0–3]}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B29i	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns
B30	$\overline{\text{CS}}$, $\overline{\text{WE}[0–3]}$ negated to A[6–31] invalid GPCM write access [9]	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B30a	$\overline{\text{WE}[0–3]}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 0, CSNT =1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B30b	$\overline{\text{WE}[0–3]}$ negated to A[6–31] invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] Invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B30c	$\overline{\text{WE}[0–3]}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	8.00	—	6.00	—	0.375	50.00	ns
B30d	$\overline{\text{WE}[0–3]}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT =1, $\overline{\text{CS}}$ negated to A[6–31] invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	25.00	—	39.00	—	31.00	—	1.375	50.00	ns

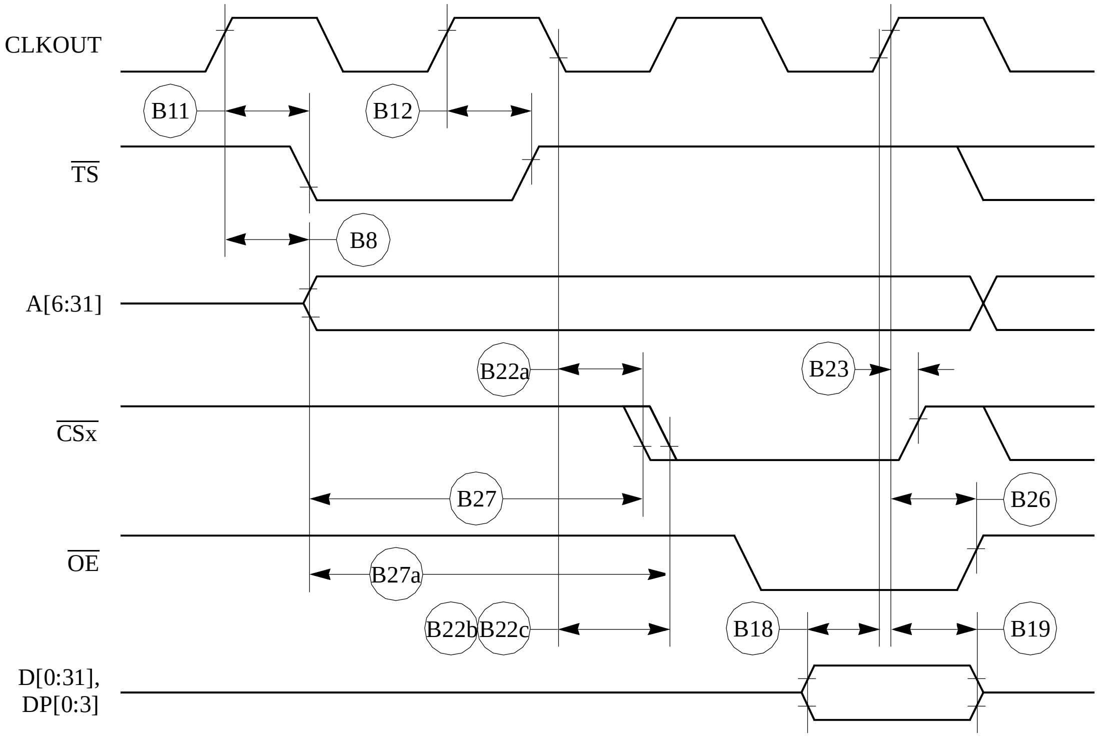


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 25 provides the PCMCIA access cycle timing for the external bus write.

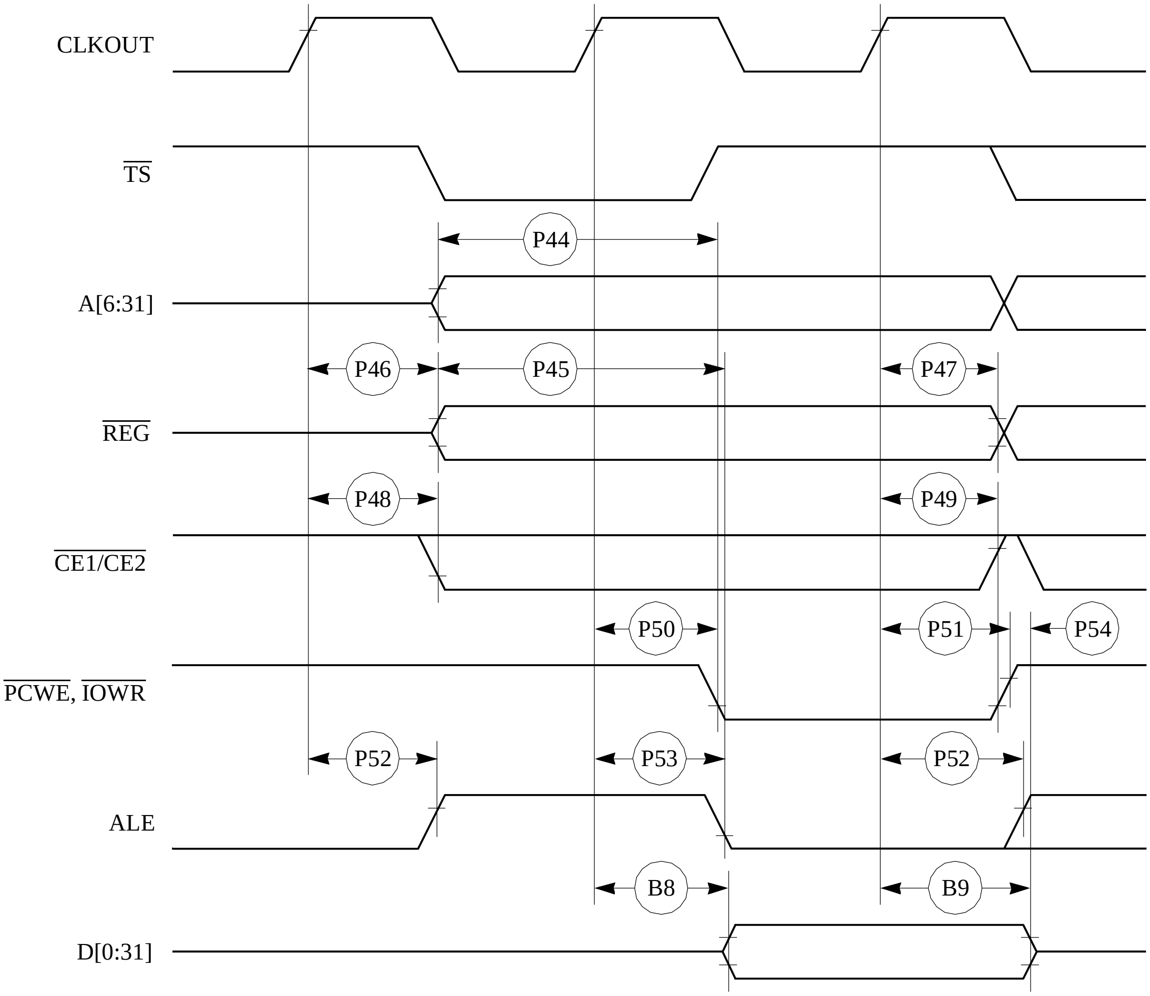


Figure 25. PCMCIA Access Cycles Timing External Bus Write

Figure 26 provides the PCMCIA WAIT signals detection timing.

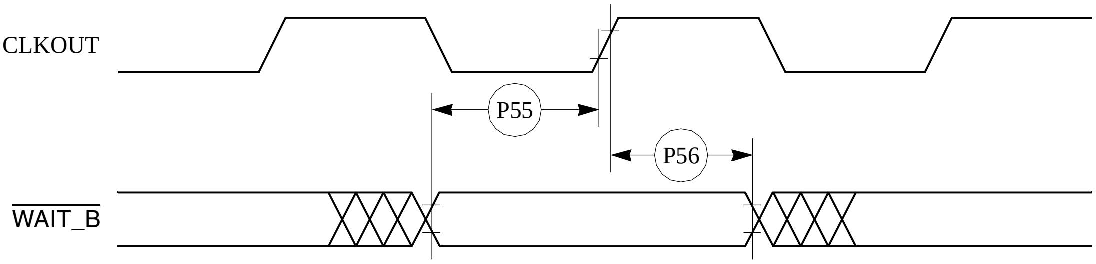


Figure 26. PCMCIA WAIT Signal Detection Timing

Table 11 shows the reset timing for the MPC850.

Table 11. Reset Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		FFACTOR	Unit
		Min	Max	Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance	—	20.00	—	20.00	—	20.00	—	ns
R71	$\overline{\text{RSTCONF}}$ pulse width	340.00	—	515.00	—	425.00	—	17.000	ns
R72		—	—	—	—	—	—	—	
R73	Configuration data to $\overline{\text{HRESET}}$ rising edge set up time	350.00	—	505.00	—	425.00	—	15.000	ns
R74	Configuration data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00	—	350.00	—	350.00	—	—	ns
R75	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R76	Configuration data hold time after $\overline{\text{HRESET}}$ negation	0.00	—	0.00	—	0.00	—	—	ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive	—	25.00	—	25.00	—	25.00	—	ns
R78	$\overline{\text{RSTCONF}}$ negated to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to data out high impedance.	—	25.00	—	25.00	—	25.00	—	ns
R80	DSDI, DSCK set up	60.00	—	90.00	—	75.00	—	3.000	ns
R81	DSDI, DSCK hold time	0.00	—	0.00	—	0.00	—	—	ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	160.00	—	242.00	—	200.00	—	8.000	ns

Figure 31 shows the reset timing for the data bus configuration.

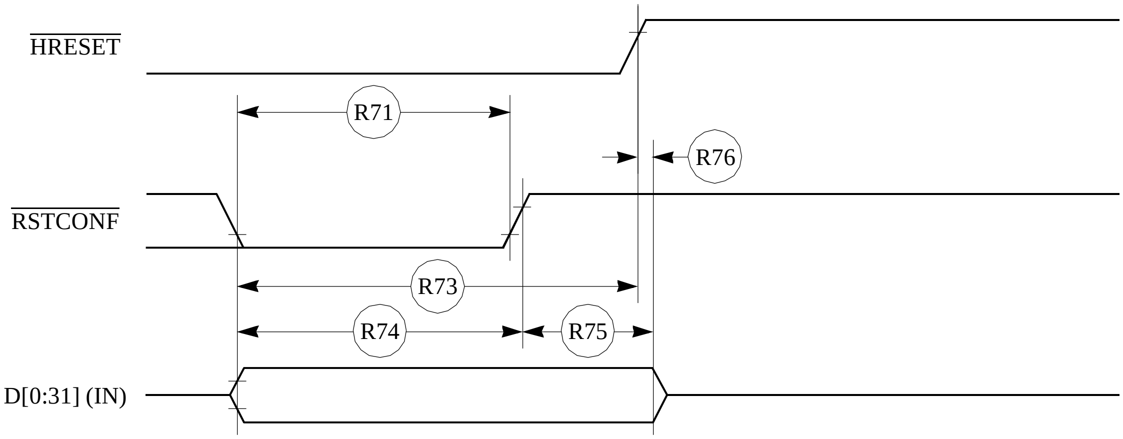


Figure 31. Reset Timing—Configuration from Data Bus

Figure 32 provides the reset timing for the data bus weak drive during configuration.

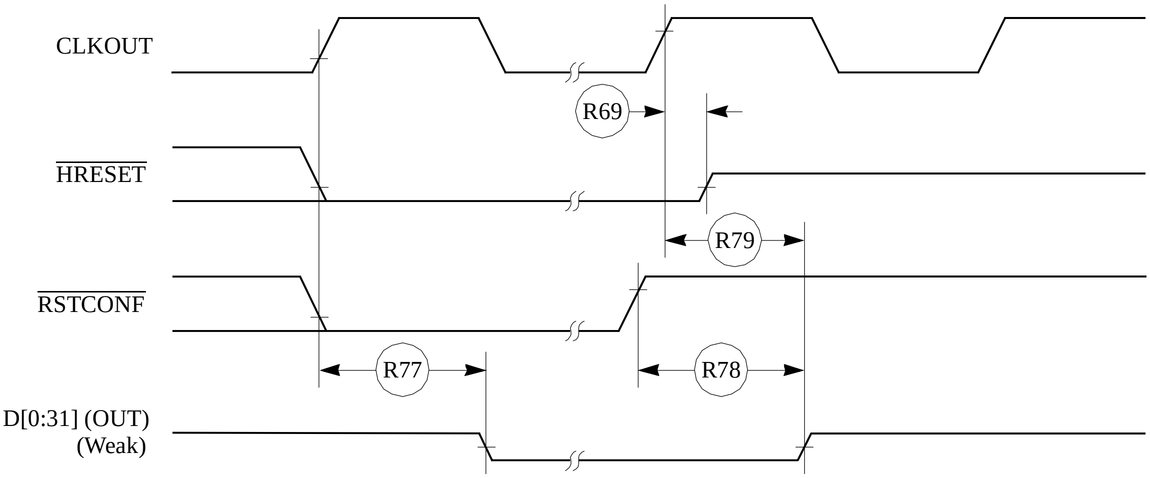


Figure 32. Reset Timing—Data Bus Weak Drive during Configuration

Figure 33 provides the reset timing for the debug port configuration.

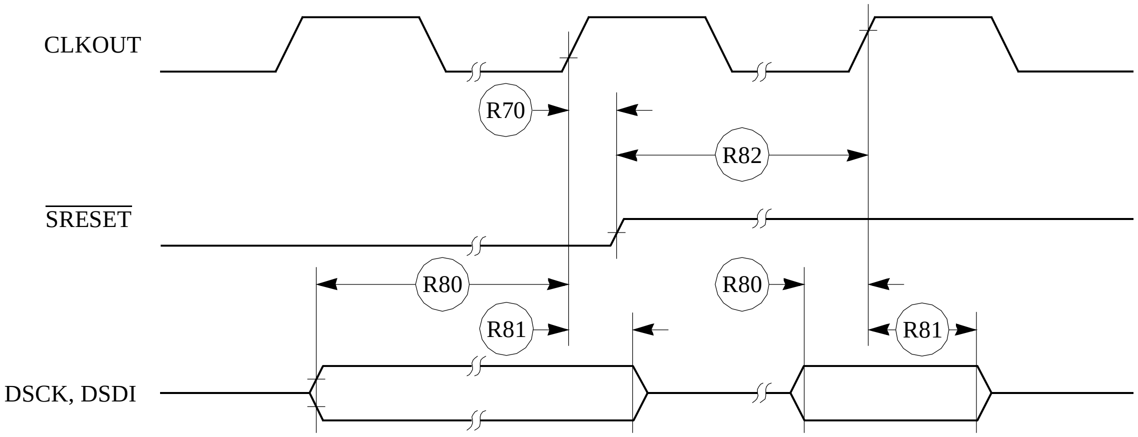


Figure 33. Reset Timing—Debug Port Configuration

7 IEEE 1149.1 Electrical Specifications

Table 12 provides the JTAG timings for the MPC850 as shown in Figure 34 to Figure 37.

Table 12. JTAG Timing

Num	Characteristic	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
J82	TCK cycle time	100.00	—	100.00	—	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	40.00	—	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	0.00	10.00	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	5.00	—	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	25.00	—	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	—	27.00	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	0.00	—	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	—	20.00	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	100.00	—	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	40.00	—	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	—	50.00	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	—	50.00	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	—	50.00	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	50.00	—	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	50.00	—	50.00	—	ns

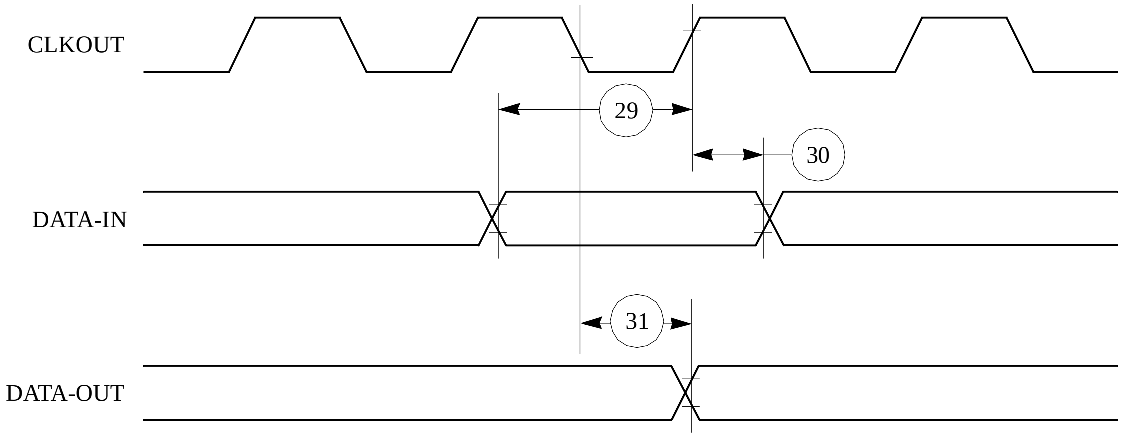


Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Table 14. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7.00	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3.00	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12.00	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12.00	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20.00	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15.00	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7.00	—	ns

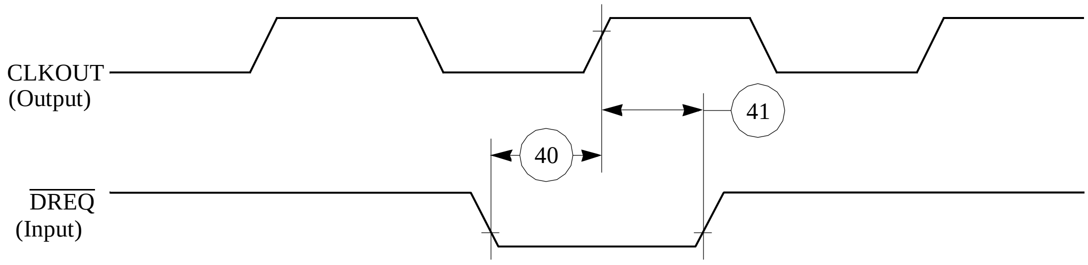


Figure 39. IDMA External Requests Timing Diagram

8.3 Baud Rate Generator AC Electrical Specifications

Table 15 provides the baud rate generator timings as shown in Figure 43.

Table 15. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10.00	ns
51	BRGO duty cycle	40.00	60.00	%
52	BRGO cycle	40.00	—	ns

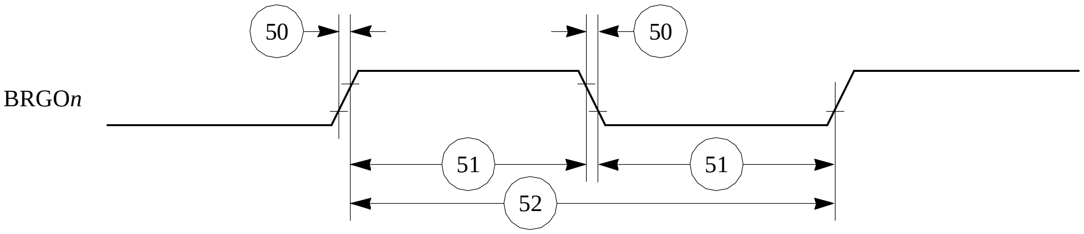


Figure 43. Baud Rate Generator Timing Diagram

8.4 Timer AC Electrical Specifications

Table 16 provides the baud rate generator timings as shown in Figure 44.

Table 16. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10.00	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1.00	—	clk
63	TIN/$\overline{\text{TGATE}}$ high time	2.00	—	clk
64	TIN/$\overline{\text{TGATE}}$ cycle time	3.00	—	clk
65	CLKO high to $\overline{\text{TOUT}}$ valid	3.00	25.00	ns

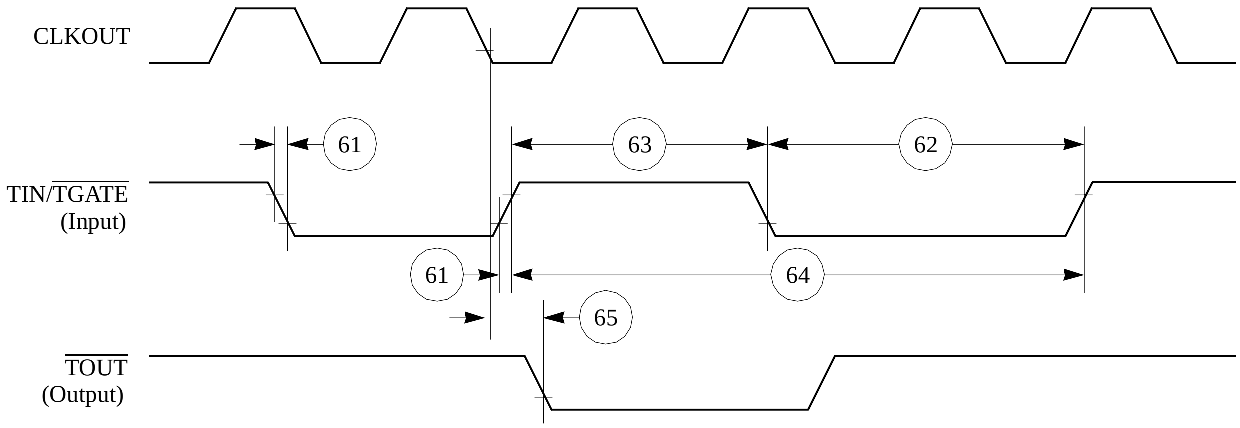


Figure 44. CPM General-Purpose Timers Timing Diagram

8.5 Serial Interface AC Electrical Specifications

Table 17 provides the serial interface timings as shown in Figure 45 to Figure 49.

Table 17. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLK, L1TCLK frequency (DSC = 0) [1, 2]	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLK, L1TCLK width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXD, L1ST*n*, $\overline{\text{L1RQ}}$, L1xCLKO rise/fall time	—	15.00	ns
73	L1RSYNC, L1TSYNC valid to L1xCLK edge Edge (SYNC setup time)	20.00	—	ns
74	L1xCLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time)	35.00	—	ns
75	L1RSYNC, L1TSYNC rise/fall time	—	15.00	ns
76	L1RXD valid to L1xCLK edge (L1RXD setup time)	17.00	—	ns
77	L1xCLK edge to L1RXD invalid (L1RXD hold time)	13.00	—	ns
78	L1xCLK edge to L1ST*n* valid [4]	10.00	45.00	ns
78A	L1SYNC valid to L1ST*n* valid	10.00	45.00	ns
79	L1xCLK edge to L1ST*n* invalid	10.00	45.00	ns
80	L1xCLK edge to L1TXD valid	10.00	55.00	ns
80A	L1TSYNC valid to L1TXD valid [4]	10.00	55.00	ns
81	L1xCLK edge to L1TXD high impedance	0.00	42.00	ns

8.6 SCC in NMSI Mode Electrical Specifications

Table 18 provides the NMSI external clock timing.

Table 18. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table)	1/SYNCCLK	—	ns
101	RCLKx and TCLKx width low	1/SYNCCLK +5	—	ns
102	RCLKx and TCLKx rise/fall time	—	15.00	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS}}$x active/inactive delay (from TCLKx falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS}}$x setup time to TCLKx rising edge	5.00	—	ns
106	RXDx setup time to RCLKx rising edge	5.00	—	ns
107	RXDx hold time from RCLKx rising edge [2]	5.00	—	ns
108	$\overline{\text{CD}}$x setup time to RCLKx rising edge	5.00	—	ns

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater than or equal to 2.25/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 19 provides the NMSI internal clock timing.

Table 19. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLKx and TCLKx frequency [1] (x = 2, 3 for all specs in this table)	0.00	SYNCCLK/3	MHz
102	RCLKx and TCLKx rise/fall time	—	—	ns
103	TXDx active delay (from TCLKx falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS}}$x active/inactive delay (from TCLKx falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS}}$x setup time to TCLKx rising edge	40.00	—	ns
106	RXDx setup time to RCLKx rising edge	40.00	—	ns
107	RXDx hold time from RCLKx rising edge [2]	0.00	—	ns
108	$\overline{\text{CD}}$x setup time to RCLKx rising edge	40.00	—	ns

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLK1x must be greater or equal to 3/1.

[2] Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

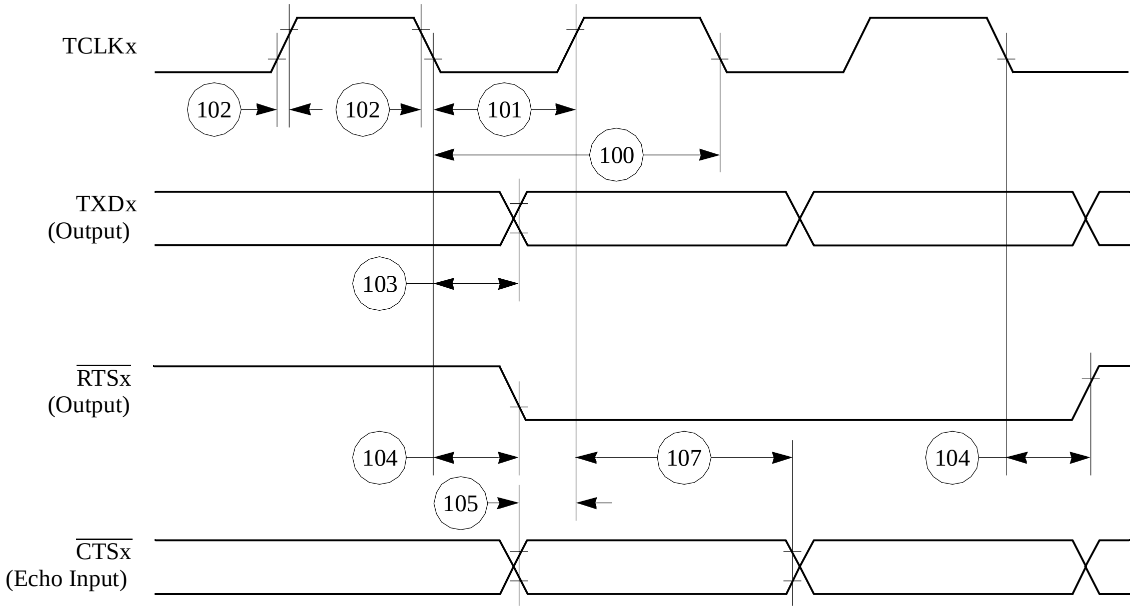


Figure 52. HDLC Bus Timing Diagram

8.7 Ethernet Electrical Specifications

Table 20 provides the Ethernet timings as shown in Figure 53 to Figure 55.

Table 20. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40.00	—	ns
121	RCLKx rise/fall time (x = 2, 3 for all specs in this table)	—	15.00	ns
122	RCLKx width low	40.00	—	ns
123	RCLKx clock period [1]	80.00	120.00	ns
124	RXDx setup time	20.00	—	ns
125	RXDx hold time	5.00	—	ns
126	RENA active delay (from RCLKx rising edge of the last data bit)	10.00	—	ns
127	RENA width low	100.00	—	ns
128	TCLKx rise/fall time	—	15.00	ns
129	TCLKx width low	40.00	—	ns
130	TCLKx clock period[1]	99.00	101.00	ns
131	TXDx active delay (from TCLKx rising edge)	10.00	50.00	ns
132	TXDx inactive delay (from TCLKx rising edge)	10.00	50.00	ns
133	TENA active delay (from TCLKx rising edge)	10.00	50.00	ns

Table 20. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to $\overline{\text{SDACK}}$ asserted [2]	—	20.00	ns
139	CLKOUT low to $\overline{\text{SDACK}}$ negated [2]	—	20.00	ns

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame destination address into memory.

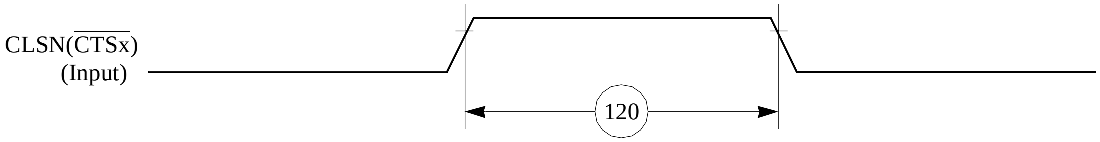


Figure 53. Ethernet Collision Timing Diagram

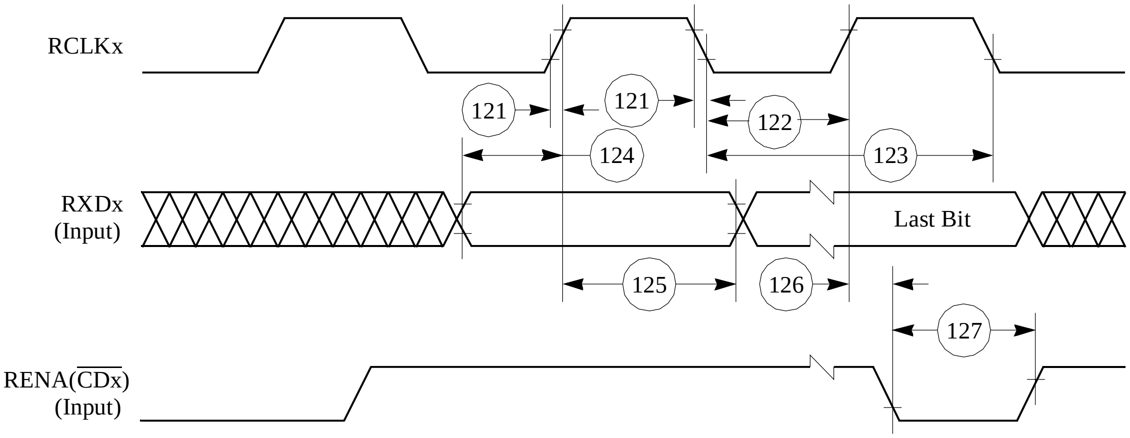


Figure 54. Ethernet Receive Timing Diagram

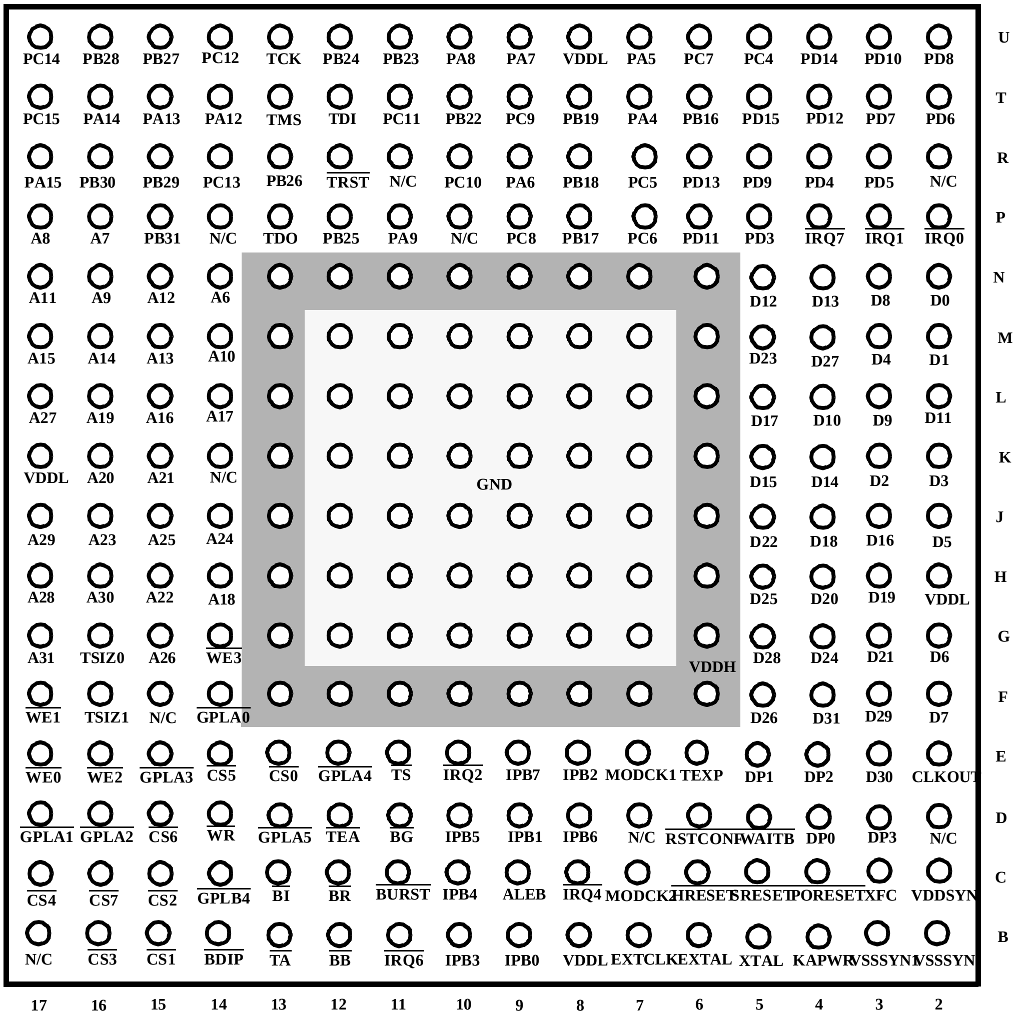
8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

Table 23. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15.00	—	ns
172	Slave enable lag time	15.00	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20.00	—	ns
176	Slave data hold time (inputs)	20.00	—	ns
177	Slave access time	—	50.00	ns
178	Slave SPI MISO disable time	—	50.00	ns
179	Slave data valid (after SPICLK edge)	—	50.00	ns
180	Slave data hold time (outputs)	0.00	—	ns
181	Rise time (input)	—	15.00	ns
182	Fall time (input)	—	15.00	ns

Figure 63 shows the JEDEC pinout of the PBGA package as viewed from the top surface.



	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
U	PC14	PB28	PB27	PC12	TCK	PB24	PB23	PA8	PA7	VDDL	PA5	PC7	PC4	PD14	PD10	PD8
T	PC15	PA14	PA13	PA12	TMS	TDI	PC11	PB22	PC9	PB19	PA4	PB16	PD15	PD12	PD7	PD6
R	PA15	PB30	PB29	PC13	PB26	TRST	N/C	PC10	PA6	PB18	PC5	PD13	PD9	PD4	PD5	N/C
P	A8	A7	PB31	N/C	TDO	PB25	PA9	N/C	PC8	PB17	PC6	PD11	PD3	IRQ7	IRQ1	IRQ0
N	A11	A9	A12	A6									D12	D13	D8	D0
M	A15	A14	A13	A10									D23	D27	D4	D1
L	A27	A19	A16	A17									D17	D10	D9	D11
K	VDDL	A20	A21	N/C				GND					D15	D14	D2	D3
J	A29	A23	A25	A24									D22	D18	D16	D5
H	A28	A30	A22	A18									D25	D20	D19	VDDL
G	A31	TSIZ0	A26	WE3								VDDH	D28	D24	D21	D6
F	WE1	TSIZ1	N/C	GPLA0									D26	D31	D29	D7
E	WE0	WE2	GPLA3	CS5	CS0	GPLA4	TS	IRQ2	IPB7	IPB2	MODCK1	TEXP	DP1	DP2	D30	CLKOUT
D	GPLA1	GPLA2	CS6	WR	GPLA5	TEA	BG	IPB5	IPB1	IPB6	N/C	RSTCONF	WAITB	DP0	DP3	N/C
C	CS4	CS7	CS2	GPLB4	BI	BR	BURST	IPB4	ALEB	IRQ4	MODCK2	HRESET	SRESET	PORESET	XFC	VDDSYN
B	N/C	CS3	CS1	BDIP	TA	BB	IRQ6	IPB3	IPB0	VDDL	EXTCLK	EXTAL	XTAL	KAPWR	VSSSYN1	VSSSYN

Figure 63. Pin Assignments for the PBGA (Top View)—JEDEC Standard

For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

10 Document Revision History

Table 28 lists significant changes between revisions of this document.

Table 28. Document Revision History

Revision	Date	Change
2	7/2005	Added footnote 3 to Table 5 (previously Table 4.5) and deleted IOL limit.
1	10/2002	Added MPC850DSL. Corrected Figure 25 on page 34.
0.2	04/2002	Updated power numbers and added Rev. C
0.1	11/2001	Removed reference to 5 Volt tolerance capability on peripheral interface pins. Replaced SI and IDL timing diagrams with better images. Updated to new template, added this revision table.

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