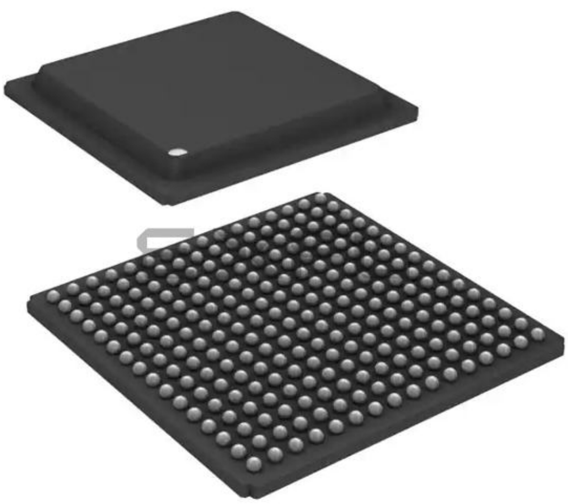
NXP USA Inc. - XPC850ZT80BU Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MPC8xx
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	80MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 95°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xpc850zt80bu

- QUICC multichannel controller (QMC) microcode features
  - Up to 64 independent communication channels on a single SCC
  - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
  - Supports either transparent or HDLC protocols for each channel
  - Independent TxBDs/Rx and event/interrupt reporting for each channel
- One universal serial bus controller (USB)
  - Supports host controller and slave modes at 1.5 Mbps and 12 Mbps
- Two serial management controllers (SMCs)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division-multiplexed (TDM) channel
- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I^2C® (interprocessor-integrated circuit) port
  - Supports master and slave modes
  - Supports multimaster environment
- Time slot assigner
  - Allows SCCs and SMCs to run in multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame syncs, clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and CPM in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, except the real-time clock and periodic interrupt timer
  - Low-power stop: to provide lower power dissipation

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC850.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA [1]	θ_{JA}	40 [2]	°C/W
	θ_{JA}	31 [3]	°C/W
	θ_{JA}	24 [4]	°C/W
Thermal Resistance for BGA (junction-to-case)	θ_{JC}	8	°C/W

[1] For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to AN-1231/D, Plastic Ball Grid Array Application Note available from your local Freescale sales office.

[2] Assumes natural convection and a single layer board (no thermal vias).

[3] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 20°C above ambient.

[4] Assumes natural convection, a multilayer board with thermal vias[4], 1 watt MPC850 dissipation, and a board temperature rise of 13°C above ambient.

$T_J = T_A + (P_D \bullet \theta_{JA})$

$P_D = (V_{DD} \bullet I_{DD}) + P_{I/O}$

where:

$P_{I/O}$ is the power dissipation on pins

Table 4 provides power dissipation information.

Table 4. Power Dissipation (P_D)

Characteristic	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
Power Dissipation All Revisions (1:1) Mode	33	TBD	515	mW
	40	TBD	590	mW
	50	TBD	725	mW

[1] Typical power dissipation is measured at 3.3V

[2] Maximum power dissipation is measured at 3.65 V

Table 5 provides the DC electrical characteristics for the MPC850.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage at 40 MHz or less	VDDH, VDDL, KAPWR, VDDSYN	3.0	3.6	V
Operating voltage at 40 MHz or higher	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
Input high voltage (address bus, data bus, EXTAL, EXTCLK, and all bus control/status signals)	VIH	2.0	3.6	V
Input high voltage (all general purpose I/O and peripheral pins)	VIH	2.0	5.5	V

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B22	CLKOUT rising edge to $\overline{\text{CS}}$ asserted GPCM ACS = 00	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22a	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0,1	—	8.00	—	8.00	—	8.00	—	50.00	ns
B22b	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0	5.00	11.75	7.58	14.33	6.25	13.00	0.250	50.00	ns
B22c	CLKOUT falling edge to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B23	CLKOUT rising edge to $\overline{\text{CS}}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0	2.00	8.00	2.00	8.00	2.00	8.00	—	50.00	ns
B24	A[6–31] to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 0.	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B24a	A[6–31] to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B25	CLKOUT rising edge to $\overline{\text{OE}}$, $\overline{\text{WE}[0–3]}$ asserted	—	9.00	—	9.00	—	9.00	—	50.00	ns
B26	CLKOUT rising edge to $\overline{\text{OE}}$ negated	2.00	9.00	2.00	9.00	2.00	9.00	—	50.00	ns
B27	A[6–31] to $\overline{\text{CS}}$ asserted GPCM ACS = 10, TRLX = 1	23.00	—	36.00	—	29.00	—	1.250	50.00	ns
B27a	A[6–31] to $\overline{\text{CS}}$ asserted GPCM ACS = 11, TRLX = 1	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B28	CLKOUT rising edge to $\overline{\text{WE}[0–3]}$ negated GPCM write access CSNT = 0	—	9.00	—	9.00	—	9.00	—	50.00	ns
B28a	CLKOUT falling edge to $\overline{\text{WE}[0–3]}$ negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0	5.00	12.00	8.00	14.00	6.00	13.00	0.250	50.00	ns
B28b	CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	—	12.00	—	14.00	—	13.00	0.250	50.00	ns

Table 6. Bus Operation Timing [1] (continued)

Num	Characteristic	50 MHz		66 MHz		80 MHz		FFACT	Cap Load (default 50 pF)	Unit
		Min	Max	Min	Max	Min	Max			
B28c	CLKOUT falling edge to WE[0–3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.00	11.00	18.00	9.00	16.00	0.375	50.00	ns
B28d	CLKOUT falling edge to $\overline{\text{CS}}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	—	14.00	—	18.00	—	16.00	0.375	50.00	ns
B29	$\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29a	$\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0 CSNT = 1, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29b	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3], high-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0	3.00	—	6.00	—	4.00	—	0.250	50.00	ns
B29c	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	8.00	—	13.00	—	11.00	—	0.500	50.00	ns
B29d	$\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29e	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0	28.00	—	43.00	—	36.00	—	1.500	50.00	ns
B29f	$\overline{\text{WE[0–3]}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns
B29g	$\overline{\text{CS}}$ negated to D[0–31], DP[0–3] high-Z GPCM write access TRLX = 0, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1	5.00	—	9.00	—	7.00	—	0.375	50.00	ns

Figure 6 provides the timing for the synchronous input signals.

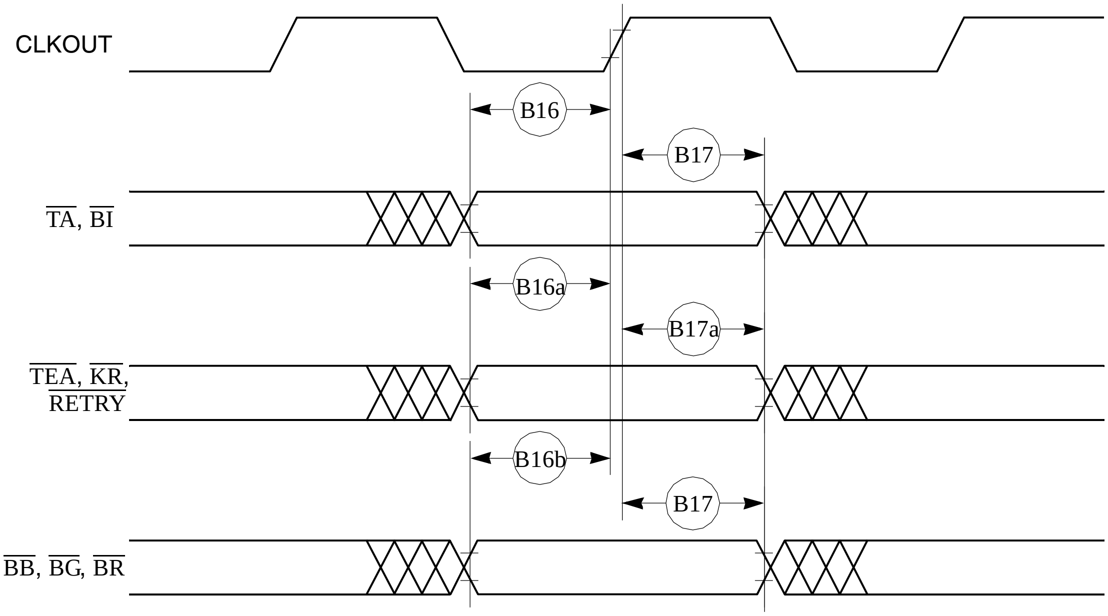


Figure 6. Synchronous Input Signals Timing

Figure 7 provides normal case timing for input data.

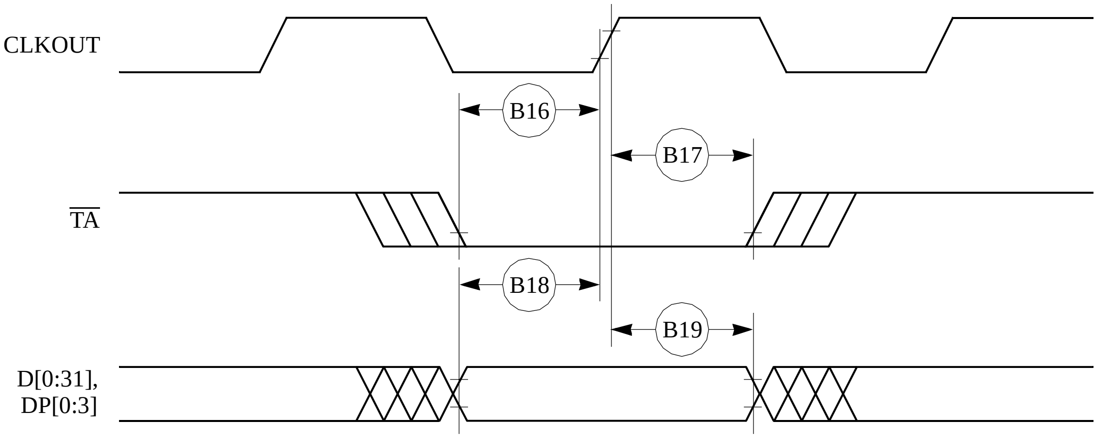


Figure 7. Input Data Timing in Normal Case

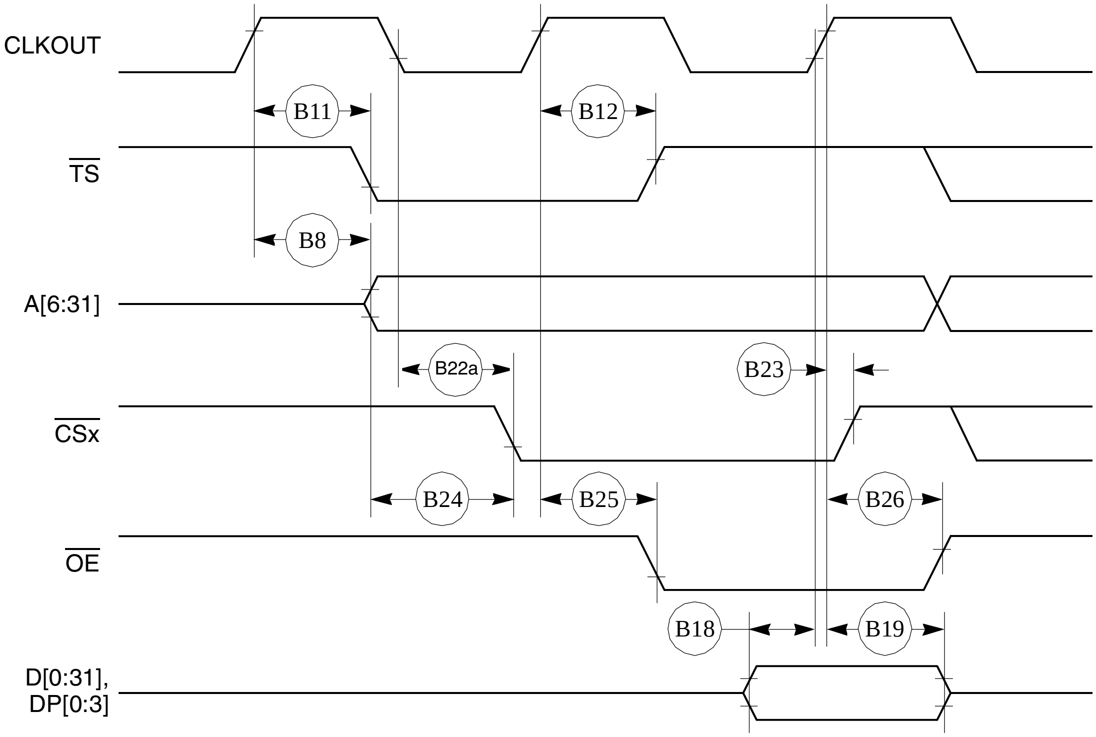


Figure 10. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

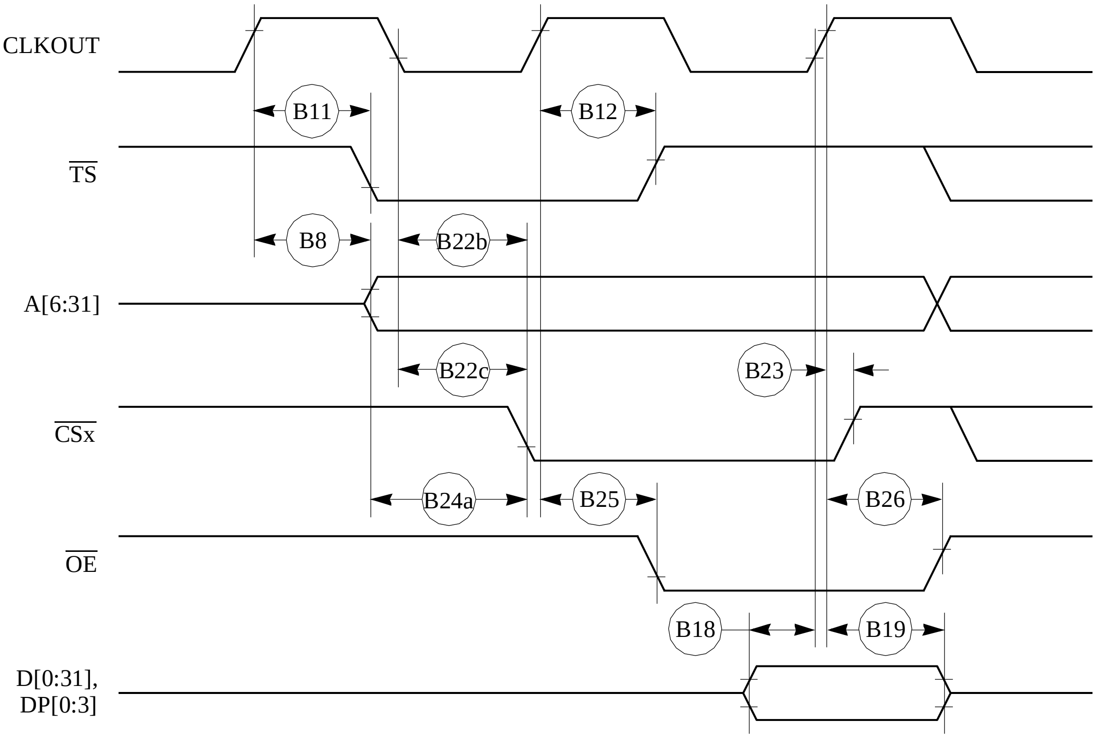


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

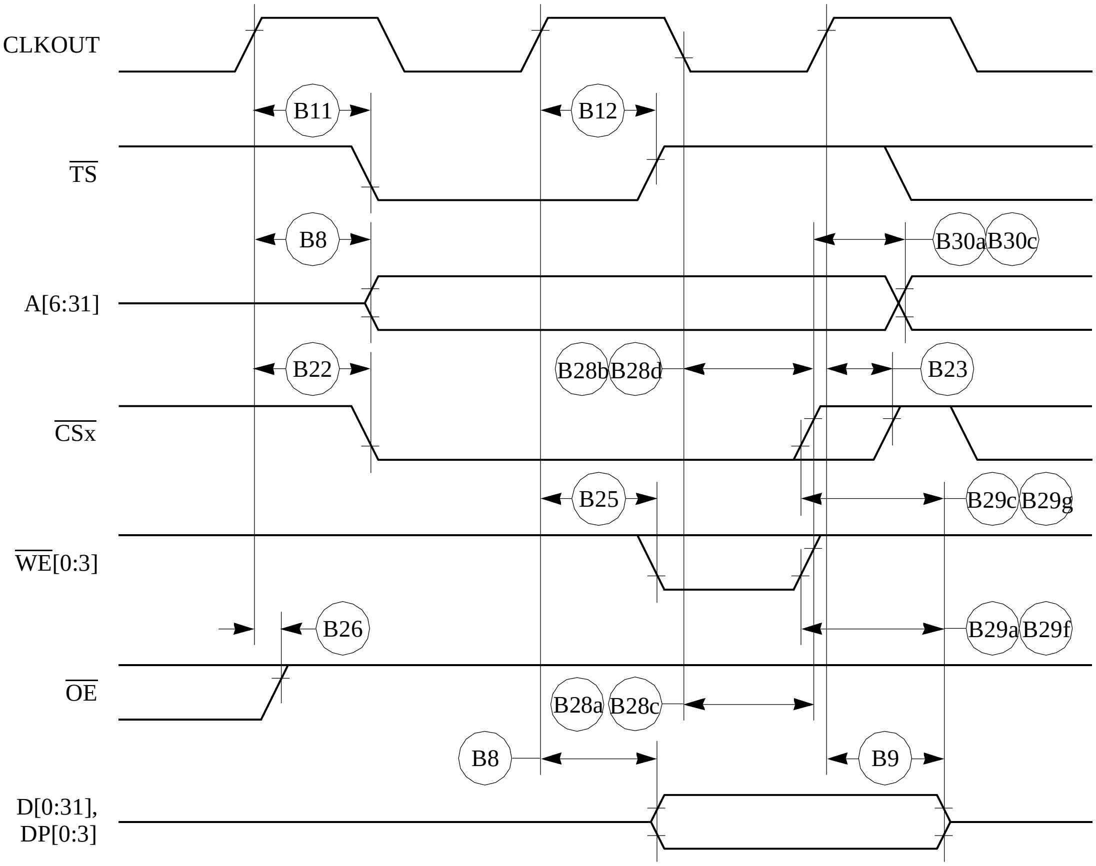


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

Table 7 provides interrupt timing for the MPC850.

Table 7. Interrupt Timing

Num	Characteristic [1]	50 MHz		66MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
I39	$\overline{\text{IRQx}}$ valid to CLKOUT rising edge (set up time)	6.00	—	6.00	—	6.00	—	ns
I40	$\overline{\text{IRQx}}$ hold time after CLKOUT.	2.00	—	2.00	—	2.00	—	ns
I41	$\overline{\text{IRQx}}$ pulse width low	3.00	—	3.00	—	3.00	—	ns
I42	$\overline{\text{IRQx}}$ pulse width high	3.00	—	3.00	—	3.00	—	ns
I43	$\overline{\text{IRQx}}$ edge-to-edge time	80.00	—	121.0	—	100.0	—	ns

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC850 is able to support

Figure 22 provides the interrupt detection timing for the external level-sensitive lines.

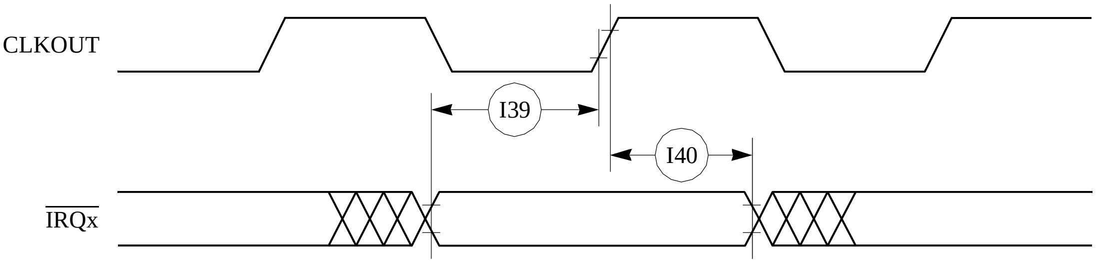


Figure 22. Interrupt Detection Timing for External Level Sensitive Lines

Figure 23 provides the interrupt detection timing for the external edge-sensitive lines.

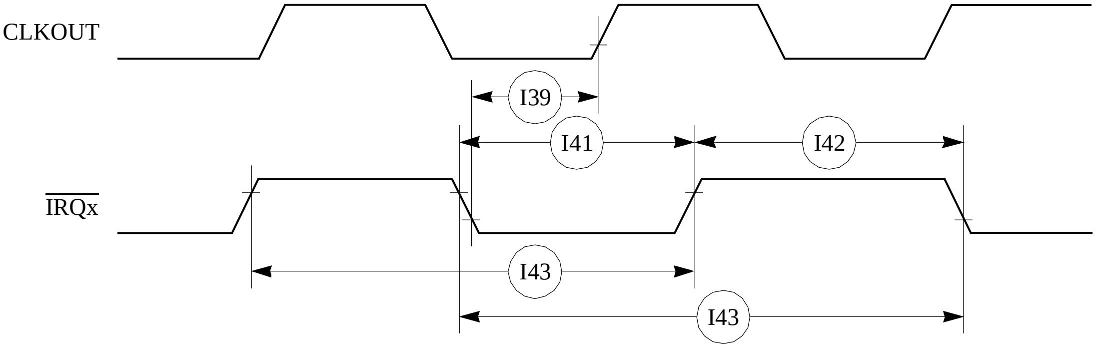


Figure 23. Interrupt Detection Timing for External Edge Sensitive Lines

Table 9 shows the PCMCIA port timing for the MPC850.

Table 9. PCMCIA Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx valid	—	19.00	—	19.00	—	19.00	ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive [1]	18.00	—	26.00	—	22.00	—	ns
P59	IP_Xx valid to CLKOUT rising edge	5.00	—	5.00	—	5.00	—	ns
P60	CLKOUT rising edge to IP_Xx invalid	1.00	—	1.00	—	1.00	—	ns

[1] OP2 and OP3 only.

Figure 27 provides the PCMCIA output port timing for the MPC850.

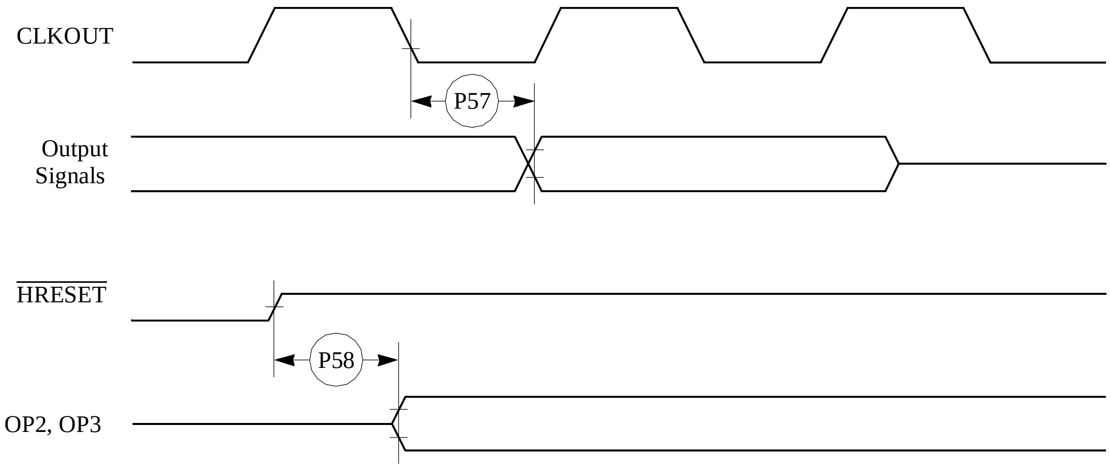


Figure 27. PCMCIA Output Port Timing

Figure 28 provides the PCMCIA output port timing for the MPC850.

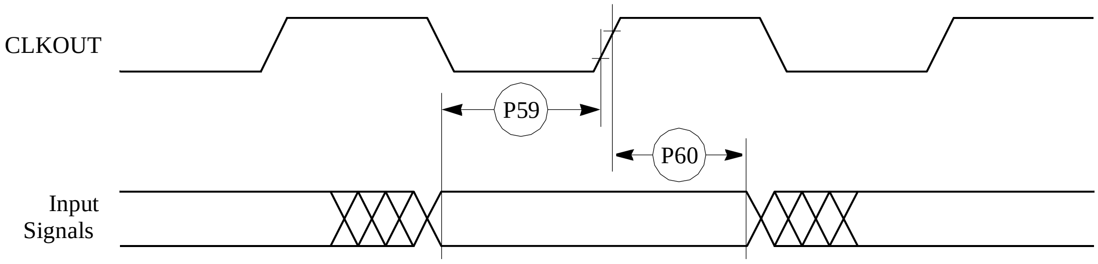


Figure 28. PCMCIA Input Port Timing

Table 10 shows the debug port timing for the MPC850.

Table 10. Debug Port Timing

Num	Characteristic	50 MHz		66 MHz		80 MHz		Unit
		Min	Max	Min	Max	Min	Max	
D61	DSCK cycle time	60.00	—	91.00	—	75.00	—	ns
D62	DSCK clock pulse width	25.00	—	38.00	—	31.00	—	ns
D63	DSCK rise and fall times	0.00	3.00	0.00	3.00	0.00	3.00	ns
D64	DSDI input data setup time	8.00	—	8.00	—	8.00	—	ns
D65	DSDI data hold time	5.00	—	5.00	—	5.00	—	ns
D66	DSCK low to DSDO data valid	0.00	15.00	0.00	15.00	0.00	15.00	ns
D67	DSCK low to DSDO invalid	0.00	2.00	0.00	2.00	0.00	2.00	ns

Figure 29 provides the input timing for the debug port clock.

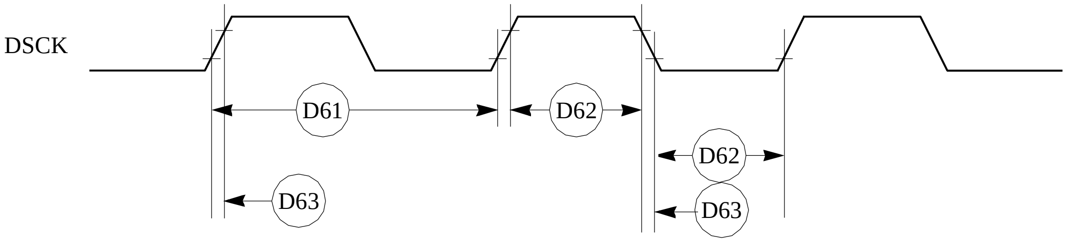


Figure 29. Debug Port Clock Input Timing

Figure 30 provides the timing for the debug port.

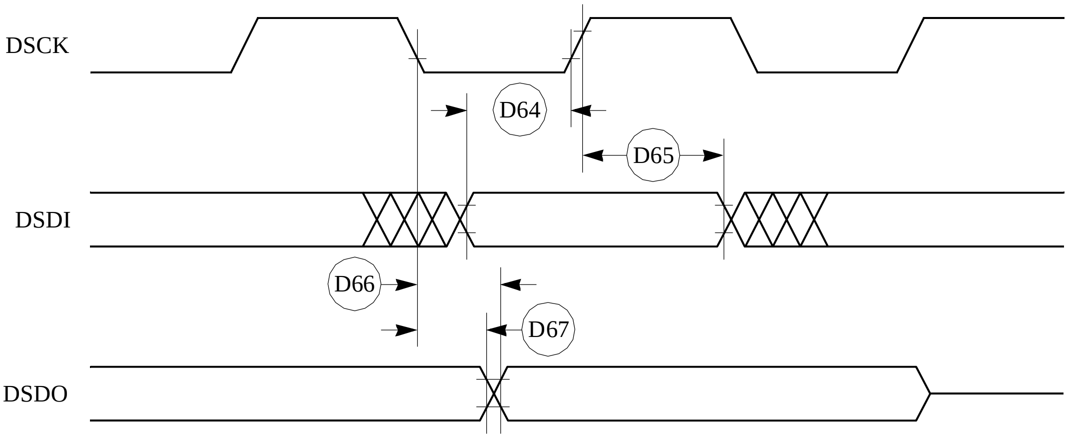


Figure 30. Debug Port Timings

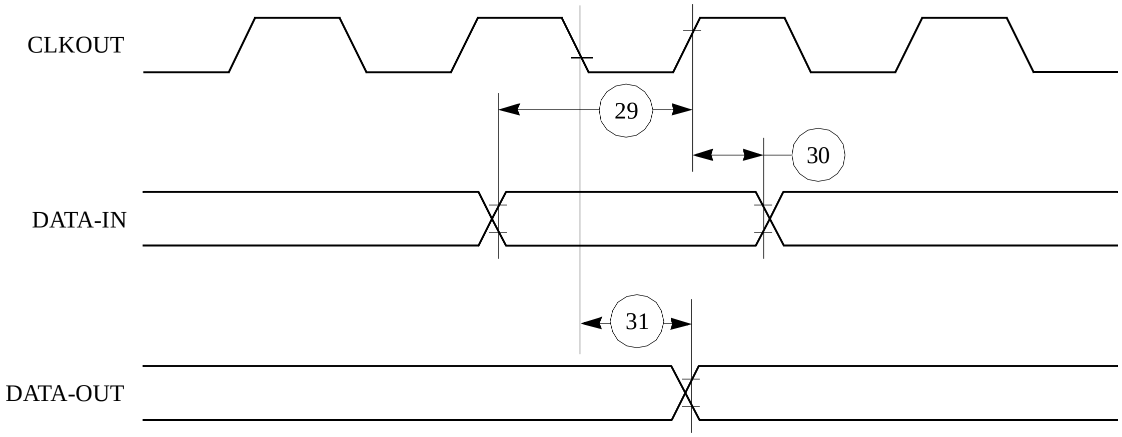


Figure 38. Parallel I/O Data-In/Data-Out Timing Diagram

8.2 IDMA Controller AC Electrical Specifications

Table 14 provides the IDMA controller timings as shown in Figure 39 to Figure 42.

Table 14. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7.00	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high	3.00	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12.00	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12.00	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20.00	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15.00	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7.00	—	ns

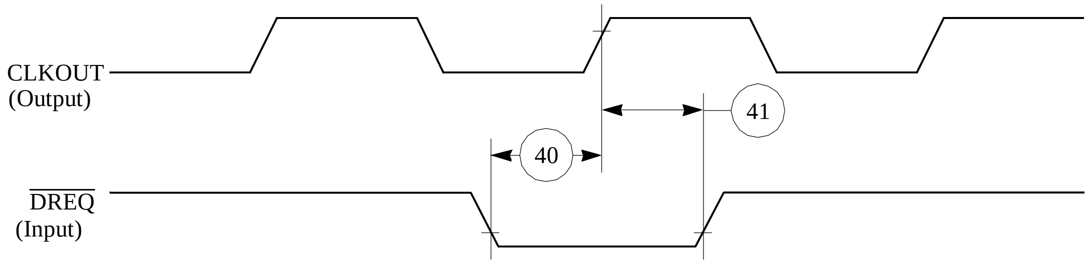


Figure 39. IDMA External Requests Timing Diagram

Table 17. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
82	L1RCLK, L1TCLK frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK width low (DSC =1)	P + 10	—	ns
83A	L1RCLK, L1TCLK width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLK edge to L1CLKO valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4]	1.00	—	L1TCLK
86	L1GR setup time[2]	42.00	—	ns
87	L1GR hold time	42.00	—	ns
88	L1xCLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

[1] The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

[2] These specs are valid for IDL mode only.

[3] Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

[4] These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

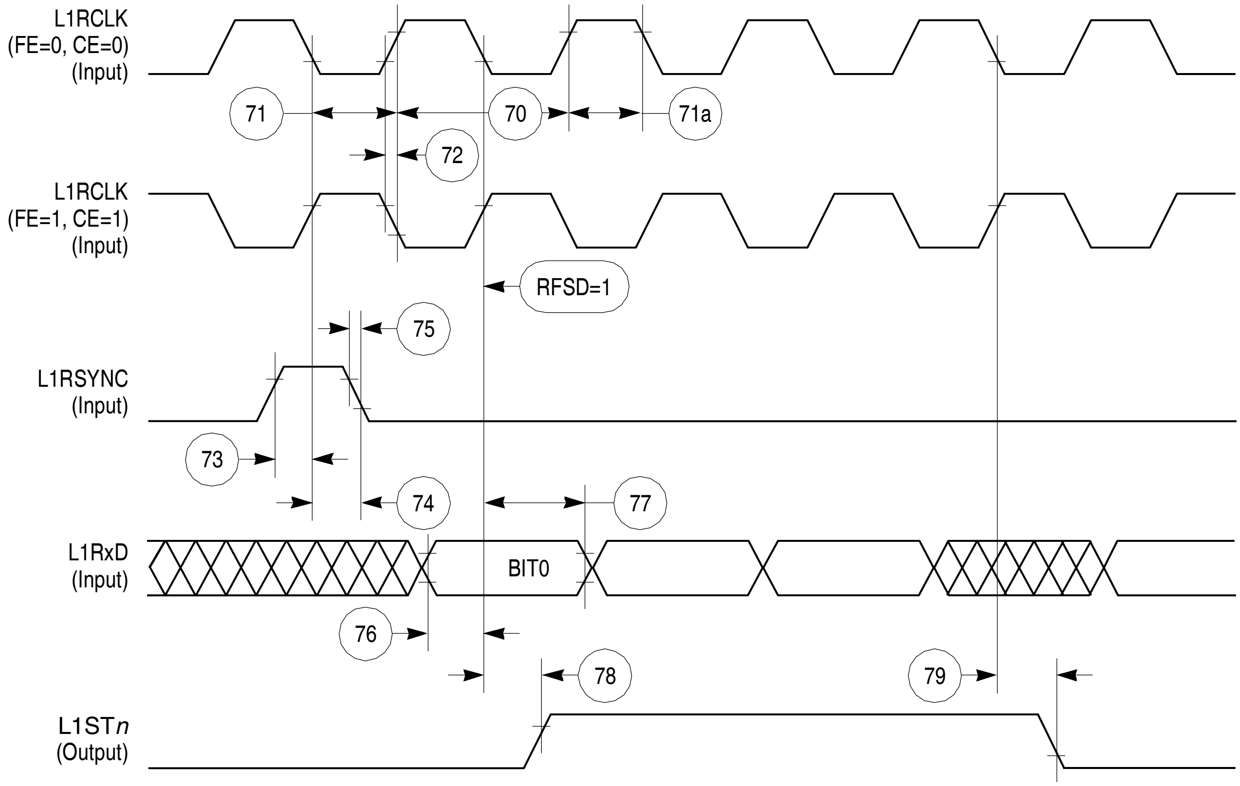


Figure 45. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

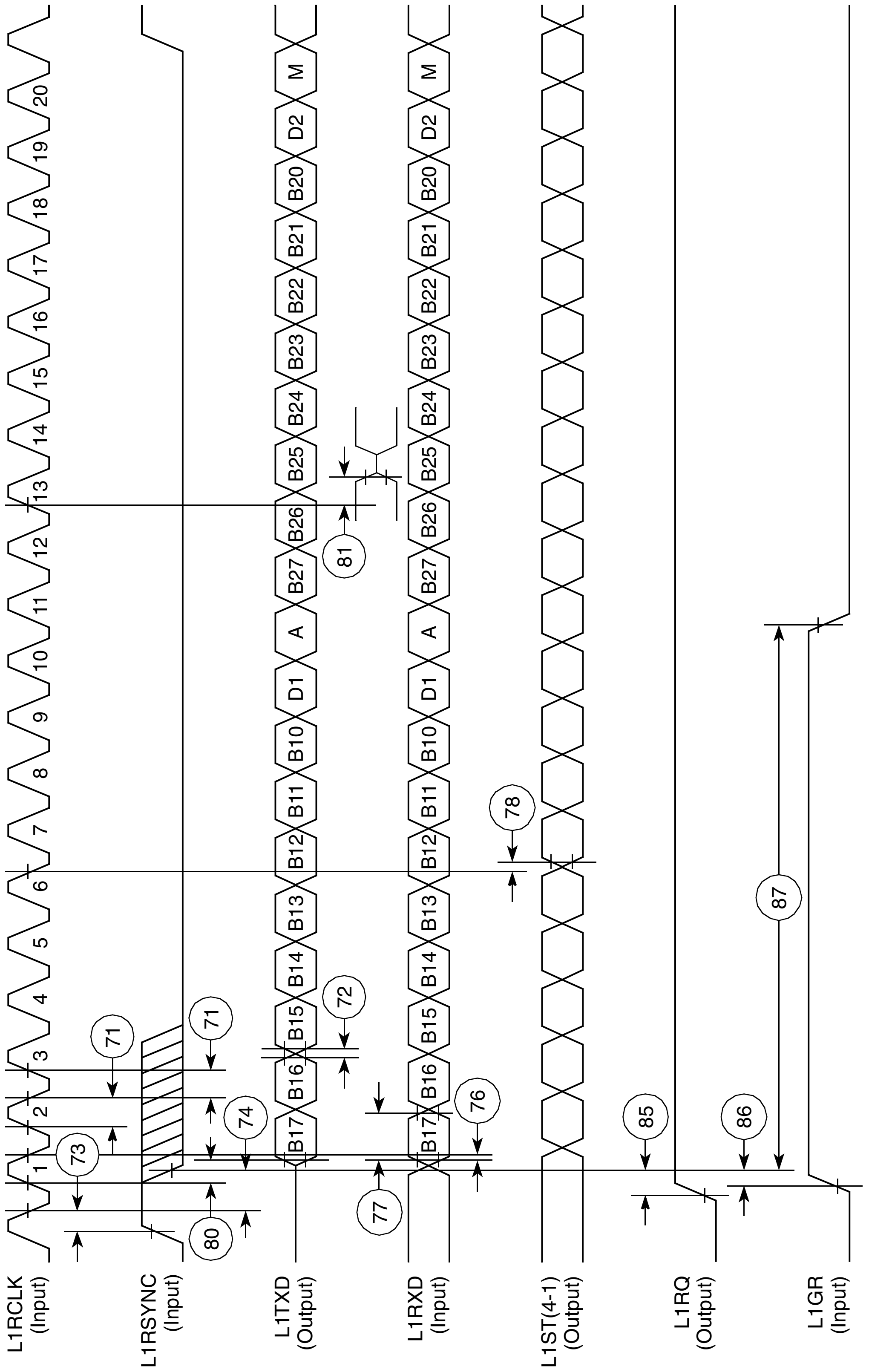


Figure 49. IDL Timing

Table 20. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLKx rising edge)	10.00	50.00	ns
138	CLKOUT low to $\overline{\text{SDACK}}$ asserted [2]	—	20.00	ns
139	CLKOUT low to $\overline{\text{SDACK}}$ negated [2]	—	20.00	ns

[1] The ratios SyncCLK/RCLKx and SyncCLK/TCLKx must be greater or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame destination address into memory.

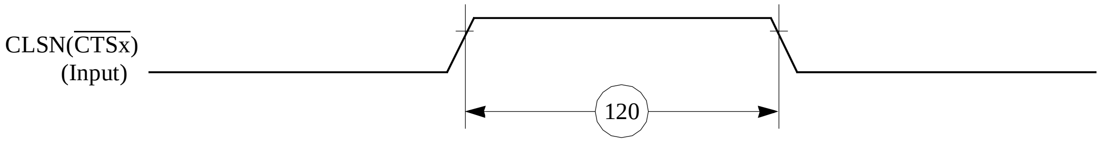


Figure 53. Ethernet Collision Timing Diagram

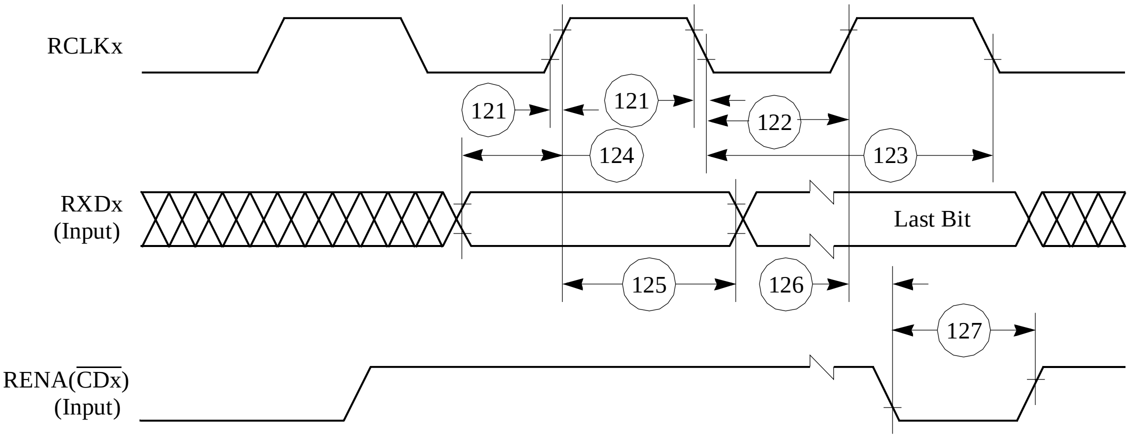
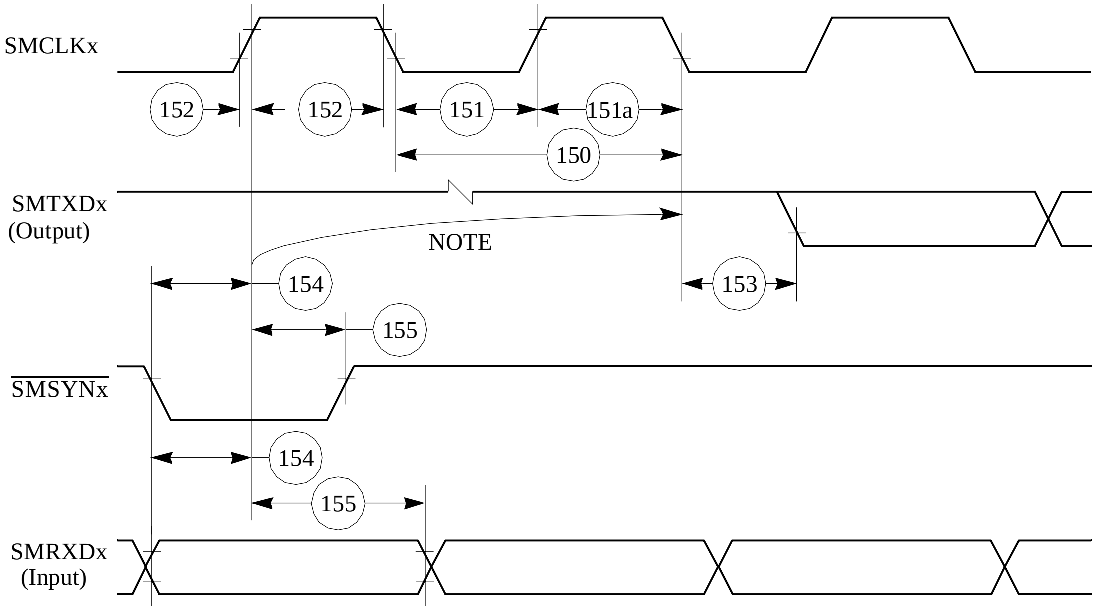


Figure 54. Ethernet Receive Timing Diagram



NOTE:
1. This delay is equal to an integer number of character-length clocks.

Figure 56. SMC Transparent Timing Diagram

8.9 SPI Master AC Electrical Specifications

Table 22 provides the SPI master timings as shown in Figure 57 and Figure 58.

Table 22. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	50.00	—	ns
163	Master data hold time (inputs)	0.00	—	ns
164	Master data valid (after SCK edge)	—	20.00	ns
165	Master data hold time (outputs)	0.00	—	ns
166	Rise time output	—	15.00	ns
167	Fall time output	—	15.00	ns

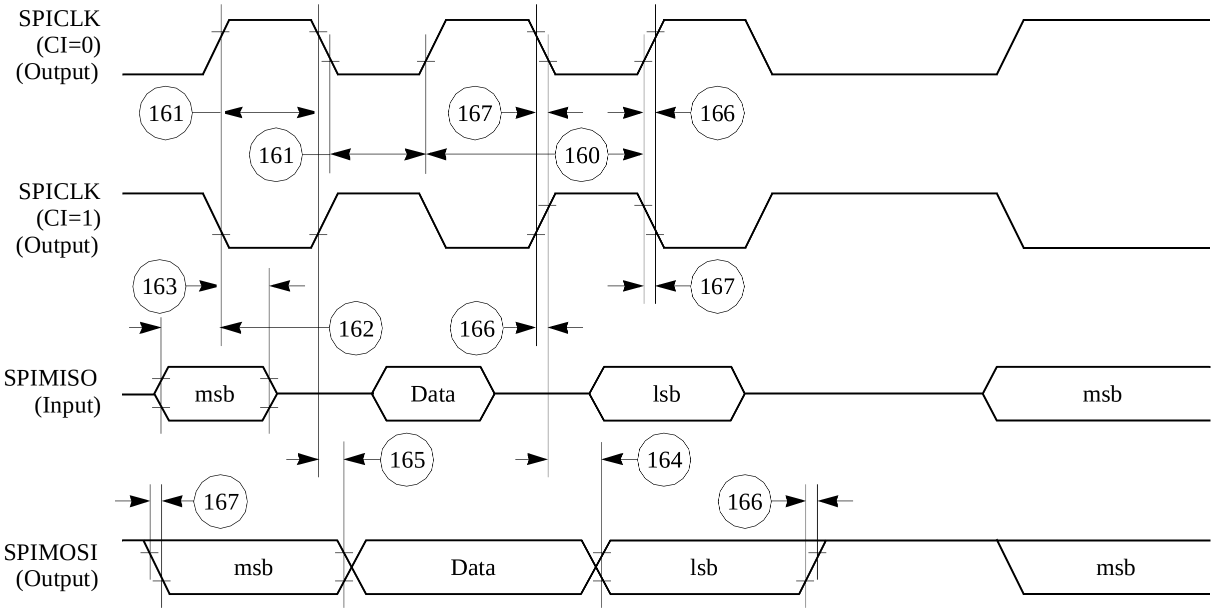


Figure 57. SPI Master (CP = 0) Timing Diagram

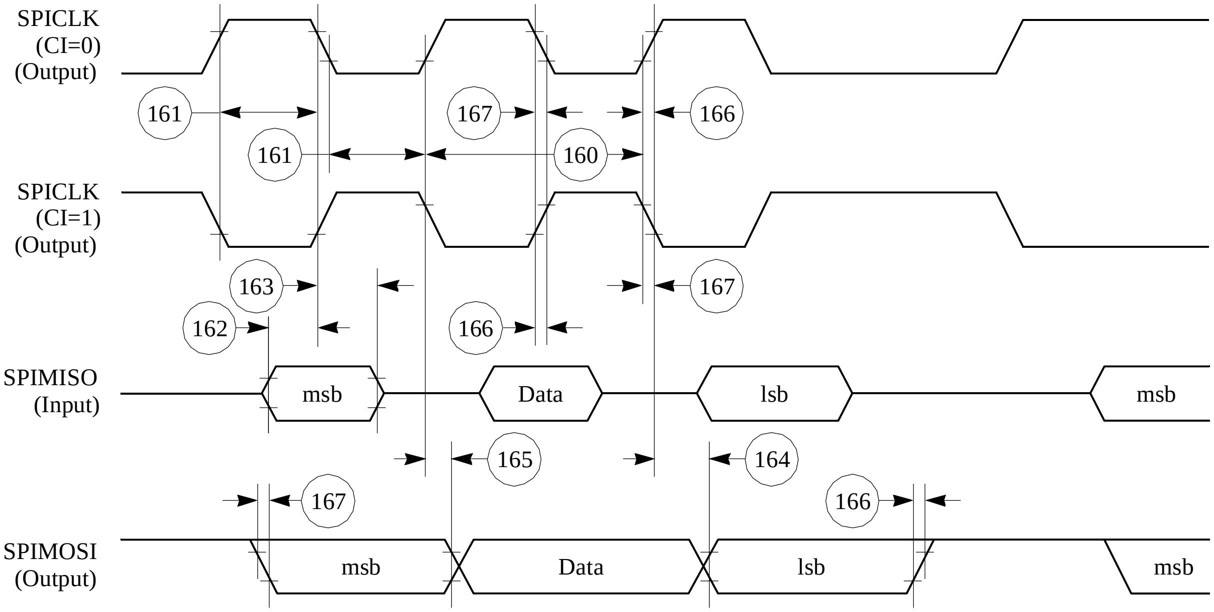


Figure 58. SPI Master (CP = 1) Timing Diagram

8.10 SPI Slave AC Electrical Specifications

Table 23 provides the SPI slave timings as shown in Figure 59 and Figure 60.

Table 23. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15.00	—	ns
172	Slave enable lag time	15.00	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20.00	—	ns
176	Slave data hold time (inputs)	20.00	—	ns
177	Slave access time	—	50.00	ns
178	Slave SPI MISO disable time	—	50.00	ns
179	Slave data valid (after SPICLK edge)	—	50.00	ns
180	Slave data hold time (outputs)	0.00	—	ns
181	Rise time (input)	—	15.00	ns
182	Fall time (input)	—	15.00	ns

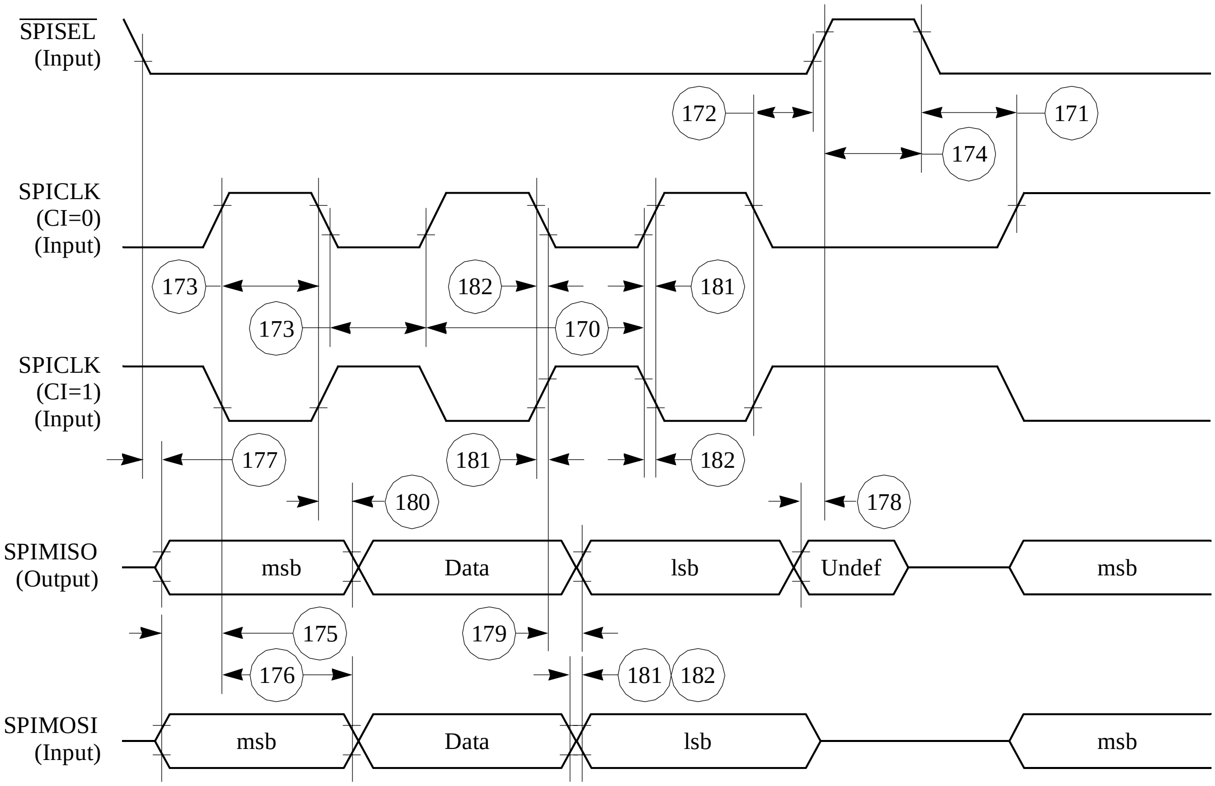
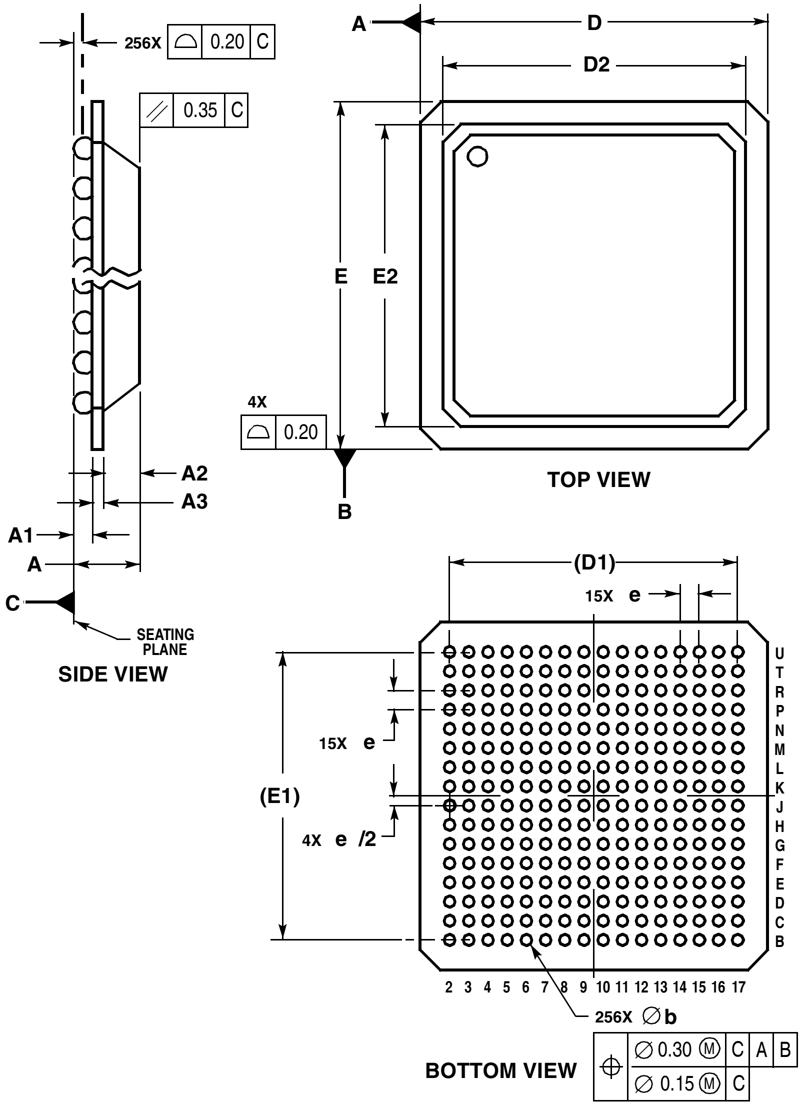


Figure 59. SPI Slave (CP = 0) Timing Diagram

Figure 65 shows the JEDEC package dimensions of the PBGA.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. PRIMARY DATUM C AND THE SEATING PLANE ARE

	MILLIMETERS	
DIM	MIN	MAX
A	1.91	2.35
A1	0.50	0.70
A2	1.12	1.22
A3	0.29	0.43
b	0.60	0.90
D	23.00 BSC	
D1	19.05 REF	
D2	19.00	20.00
E	23.00 BSC	
E1	19.05 REF	
E2	19.00	20.00
e	1.27 BSC	

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Figure 65. Package Dimensions for the Plastic Ball Grid Array (PBGA)—JEDEC Standard

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Document Number: MPC850EC
Rev. 2
07/2005