Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303cbt7tr

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F303xB/STM32F303xC family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F303xB/STM32F303xC family devices.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded Flash memory

All STM32F303xB/STM32F303xC devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

Figure 2. Clock tree

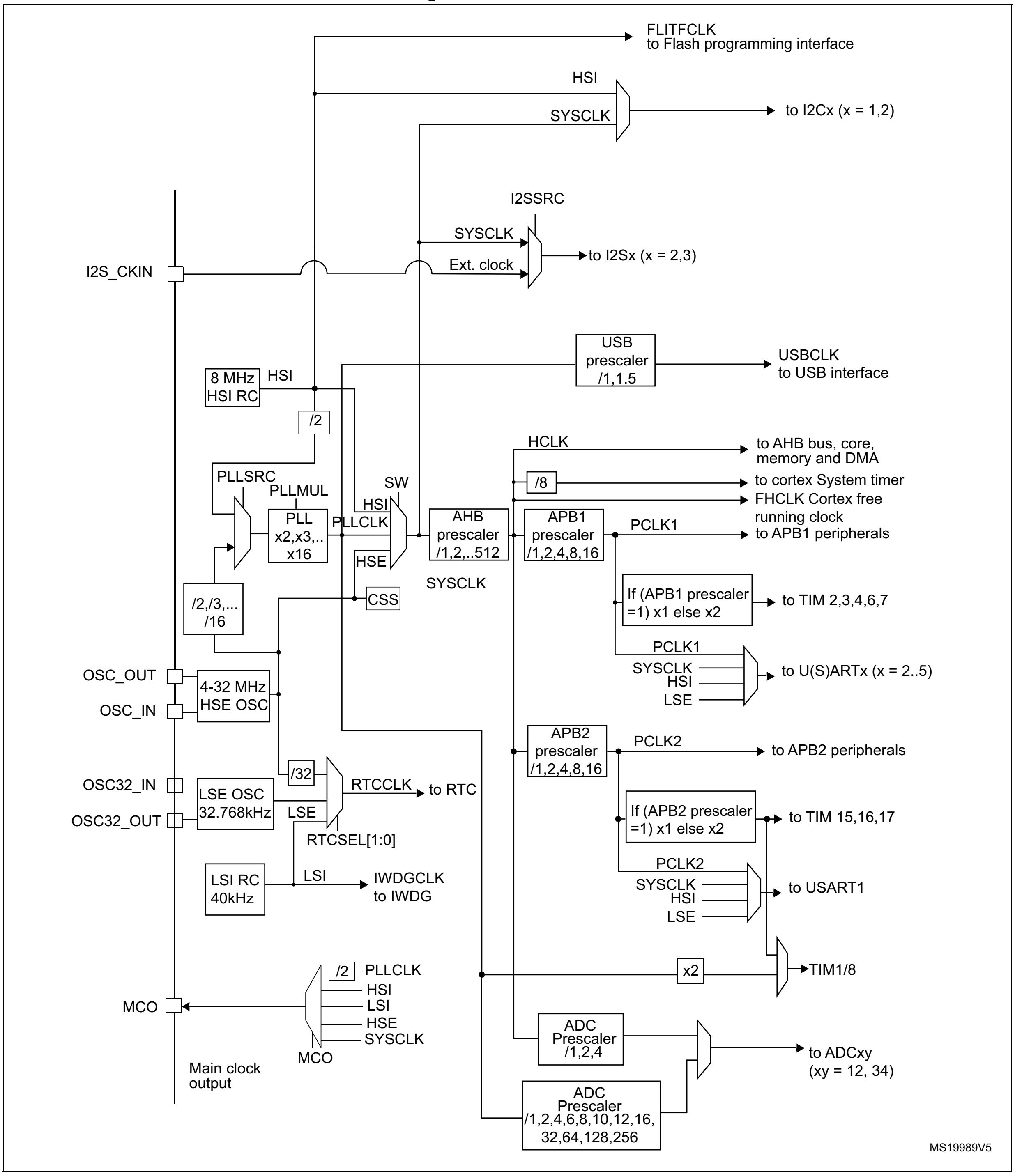


Table 13. STM32F303xB/STM32F303xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
J9	24	15	11	PA1	I/O	TTa	(4)	USART2_RTS_DE, TIM2_CH2, TSC_G1_IO2, TIM15_CH1N, RTC_REFIN, EVENTOUT	ADC1_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP
F7	25	16	12	PA2	I/O	TTa	(4) (5)	USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT
G7	26	17	13	PA3	I/O	TTa	(4)	USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4, EVENTOUT	ADC1_IN4, OPAMP1_VINP, COMP2_INP, OPAMP1_VINM
-	27	18	-	PF4	I/O	TTa	(1) (4)	COMP1_OUT, EVENTOUT	ADC1_IN5
K9, K10	-	-	-	VSS	S	-	-	Digital ground	
K8	28	19	-	VDD	S	-	-	Digital power supply	
J7	29	20	14	PA4	I/O	TTa	(4) (5)	SPI1_NSS, SPI3_NSS,I2S3_WS, USART2_CK, TSC_G2_IO1, TIM3_CH2, EVENTOUT	ADC2_IN1, DAC1_OUT1, OPAMP4_VINP, COMP1_INM, COMP2_INM, COMP3_INM, COMP4_INM, COMP5_INM, COMP6_INM, COMP7_INM
H7	30	21	15	PA5	I/O	TTa	(4) (5)	SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2, EVENTOUT	ADC2_IN2, DAC1_OUT2 OPAMP1_VINP, OPAMP2_VINM, OPAMP3_VINP COMP1_INM, COMP2_INM, COMP3_INM, COMP4_INM, COMP5_INM, COMP6_INM, COMP7_INM
H6	31	22	16	PA6	I/O	TTa	(4) (5)	SPI1_MISO, TIM3_CH1, TIM8_BKIN, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC2_IN3, OPAMP2_VOUT
K7	32	23	17	PA7	I/O	TTa	(4)	SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, TIM8_CH1N, TSC_G2_IO4, COMP2_OUT, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP2_VINP, OPAMP1_VINP
G6	33	24	-	PC4	I/O	TTa	(1) (4)	USART1_TX, EVENTOUT	ADC2_IN5

Table 15. Alternate functions for port B

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB0	-	-	TIM3_ CH3	TSC_ G3_IO2	TIM8_ CH2N	-	TIM1_CH2N	-	-	-	-	-	EVENT OUT
PB1	-	-	TIM3_ CH4	TSC_ G3_IO3	TIM8_ CH3N	-	TIM1_CH3N	-	COMP4_ OUT	-	-	-	EVENT OUT
PB2	-	-	-	TSC_ G3_IO4	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO-TRACES WO	TIM2_ CH2	TIM4_ ETR	TSC_ G5_IO1	TIM8_ CH1N	SPI1_ SCK	SPI3_SCK, I2S3_CK	USART2_ TX	-	-	TIM3_ ETR	-	EVENT OUT
PB4	NJTRST	TIM16_ CH1	TIM3_ CH1	TSC_ G5_IO2	TIM8_ CH2N	SPI1_ MISO	SPI3_MISO, I2S3ext_SD	USART2_ RX	-	-	TIM17_ BKIN	-	EVENT OUT
PB5	-	TIM16_ BKIN	TIM3_ CH2	TIM8_ CH3N	I2C1_ SMBA	SPI1_ MOSI	SPI3_MOSI, I2S3_SD	USART2_ CK	-	-	TIM17_ CH1	-	EVENT OUT
PB6	-	TIM16_ CH1N	TIM4_ CH1	TSC_ G5_IO3	I2C1_SCL	TIM8_CH1	TIM8_ ETR	USART1_ TX	-	-	TIM8_ BKIN2	-	EVENT OUT
PB7	-	TIM17_ CH1N	TIM4_ CH2	TSC_ G5_IO4	I2C1_ SDA	TIM8_ BKIN	-	USART1_ RX	-	-	TIM3_ CH4	-	EVENT OUT
PB8	-	TIM16_ CH1	TIM4_ CH3	TSC_ SYNC	I2C1_SCL	-	-	-	COMP1_ OUT	CAN_RX	TIM8_ CH2	TIM1_ BKIN	EVENT OUT
PB9	-	TIM17_ CH1	TIM4_ CH4		I2C1_ SDA	-	IR_OUT	-	COMP2_ OUT	CAN_TX	TIM8_ CH3	-	EVENT OUT
PB10	-	TIM2_ CH3	-	TSC_ SYNC	-	-	-	USART3_ TX	-	-	-	-	EVENT OUT
PB11	-	TIM2_ CH4	-	TSC_ G6_IO1	-	-	-	USART3_ RX	-	-	-	-	EVENT OUT
PB12	-	-	-	TSC_ G6_IO2	I2C2_ SMBA	SPI2_NSS, I2S2_WS	TIM1_ BKIN	USART3_ CK	-	-	-	-	EVENT OUT

Table 15. Alternate functions for port B (continued)

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB13	-	-	-	TSC_ G6_IO3	-	SPI2_SCK, I2S2_CK	TIM1_ CH1N	USART3_ CTS	-	-	-	-	EVENT OUT
PB14	-	TIM15_ CH1	-	TSC_ G6_IO4	-	SPI2_MISO, I2S2ext_SD	TIM1_ CH2N	USART3_ RTS_DE	-	-	-	-	EVENT OUT
PB15	RTC_ REFIN	TIM15_ CH2	TIM15_ CH1N	-	TIM1_ CH3N	SPI2_MOSI, I2S2_SD	-	-	-	-	-	-	EVENT OUT

2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA}.
3. V_{IN} maximum must always be respected. Refer to *Table 22: Current characteristics* for the maximum allowed injected current values.
4. Include VREF- pin.

Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)	–160	
I_{VDD}	Maximum current into each V_{DD} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS} ground line (sink)(1)	–100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	–25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	–80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 21: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 70*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 36. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	44.1	7.0	mA
			64 MHz	39.7	6.3	
			48 MHz	30.3	4.9	
			32 MHz	20.5	3.5	
			24 MHz	15.4	2.8	
			16 MHz	10.6	2.0	
			8 MHz	5.4	1.1	
			4 MHz	3.2	1.0	
			2 MHz	2.1	0.9	
			1 MHz	1.5	0.8	
			500 kHz	1.2	0.8	
			125 kHz	1.0	0.8	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.7	238.5	µA
			64 MHz	210.5	209.6	
			48 MHz	155.0	155.6	
			32 MHz	105.3	105.2	
			24 MHz	81.9	81.8	
			16 MHz	58.7	58.6	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

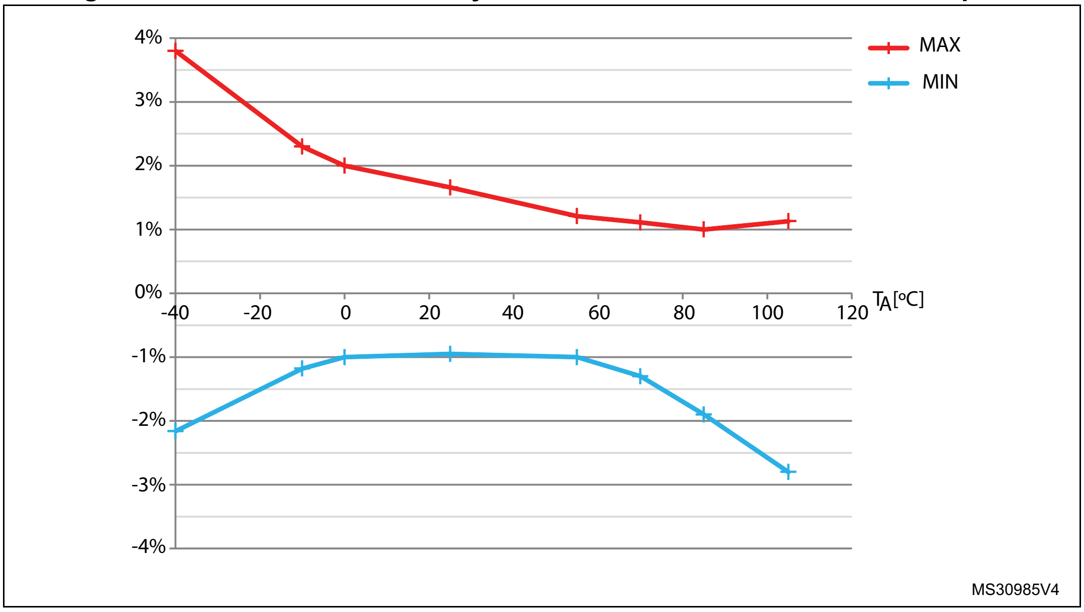
1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 37. Switching output I/O current consumption

Symbol	Parameter	Conditions[(1)]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

Figure 18. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics[(1)]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$[(2)]	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$[(2)]	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 19* and *Figure 20* for standard I/Os.

Figure 19. TC and TTa I/O input characteristics - CMOS port

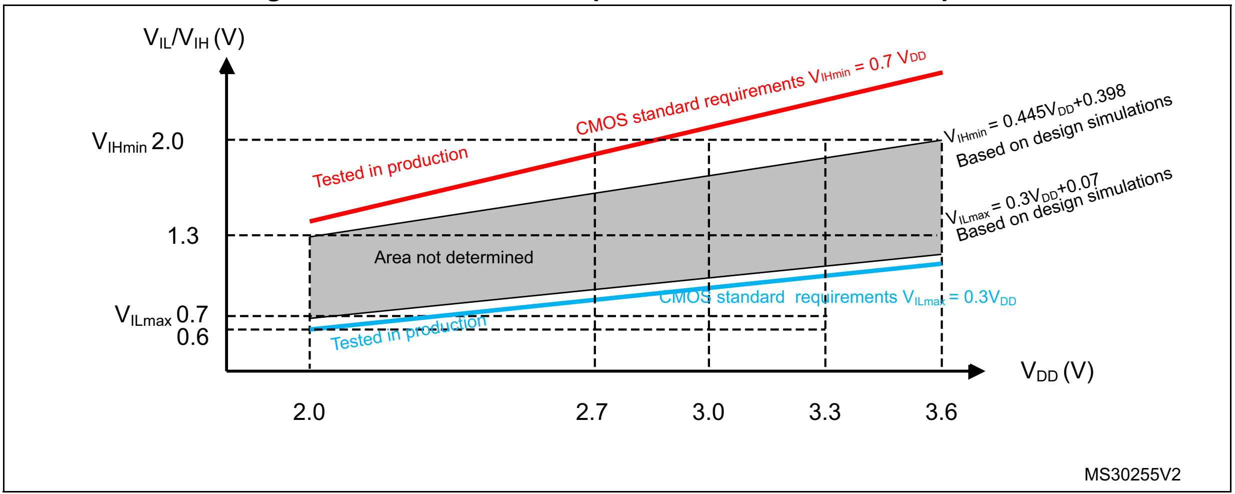


Figure 20. TC and TTa I/O input characteristics - TTL port

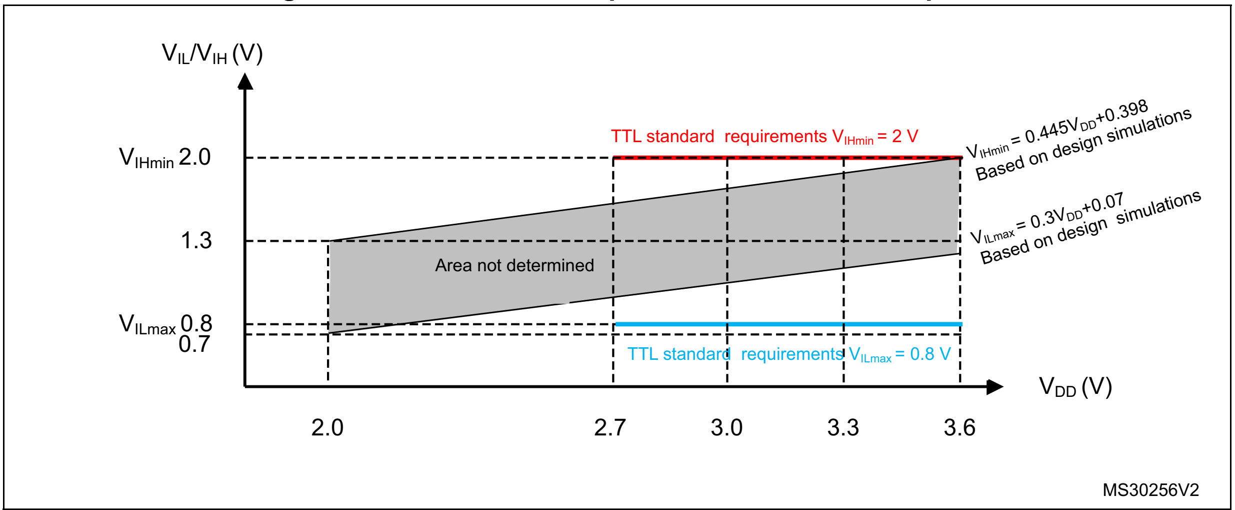


Table 67. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

Table 69. Maximum ADC R_{AIN} (1)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0
10 bits	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
	7.5	104.17	1.20	0.82	0.68
	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Guaranteed by characterization results.
2. All fast channels, expect channels on PA2, PA6, PB1, PB12.

Table 73. ADC accuracy, 64-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
SNR(5)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, 2 V ≤ V_{DDA} ≤ 3.6 V 64-pin package	Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 74. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

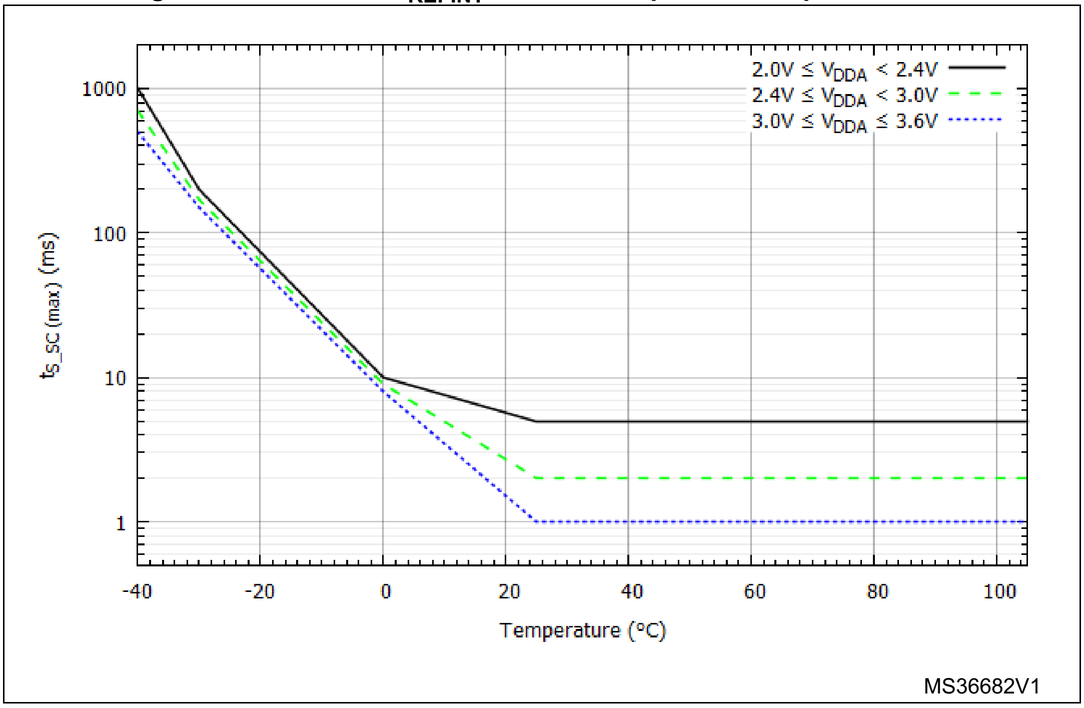
1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.14: I/O port characteristics* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

Table 76. Comparator characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

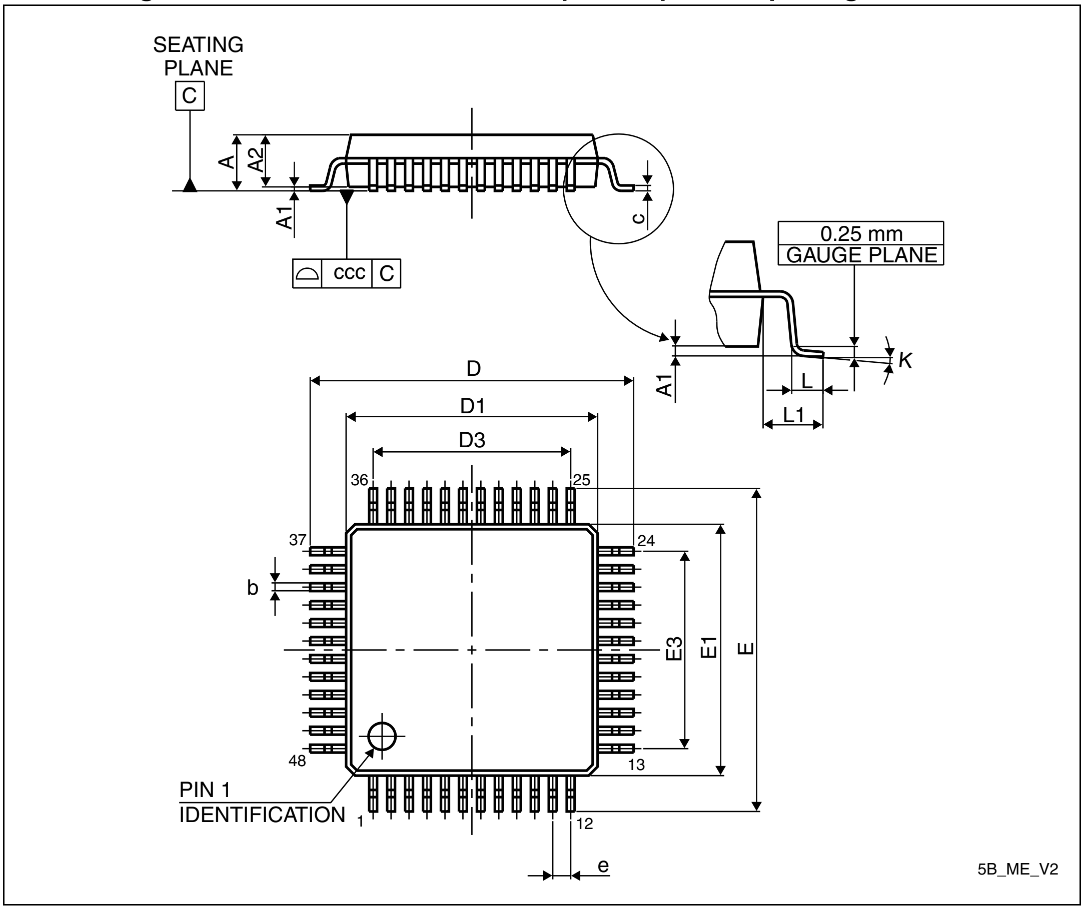
1. Data guaranteed by design.
2. For more details and conditions, see *Figure 37* Maximum V_{REFINT} scaler startup time from power down.

Figure 37. Maximum V_{REFINT} scaler startup time from power down



7.3 LQFP48 – 7 x 7 mm, low-profile quad flat package information

Figure 45. LQFP48 – 7 x 7 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data

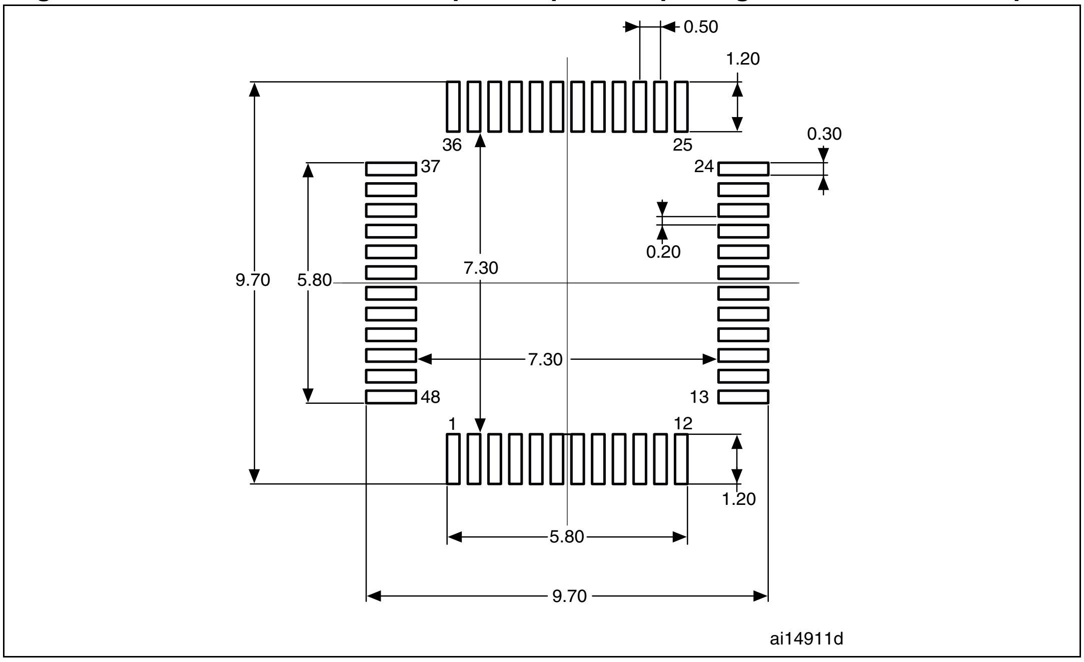
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.0035	-	0.0079
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.80	7.00	7.20	0.2677	0.2756	0.2835
D3	-	5.50	-	-	0.2165	-
E	8.80	9.00	9.20	0.3465	0.3543	0.3622

Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
E1	6.80	7.00	7.20	0.2677	0.2756	0.2835
E3	-	5.50	-	-	0.2165	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. LQFP48 - 7 x 7 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

Table 84. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
Ø b[3]	0.22	0.25	0.28	-	0.0098	0.0110
D	4.166	4.201	4.236	-	0.1654	0.1668
E	4.628	4.663	4.698	-	0.1836	0.1850
e	-	0.4	-	-	0.0157	-
e1	-	3.6	-	-	0.1417	-
e2	-	3.6	-	-	0.1417	-
F	-	0.3005	-	-	0.0118	-
G	-	0.5315	-	-	0.0209	-
N	-	100	-	-	3.9370	-
aaa	-	0.1	-	-	0.0039	-
bbb	-	0.1	-	-	0.0039	-
ccc	-	0.1	-	-	0.0039	-
ddd	-	0.05	-	-	0.0020	-
eee	-	0.05	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 49. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint

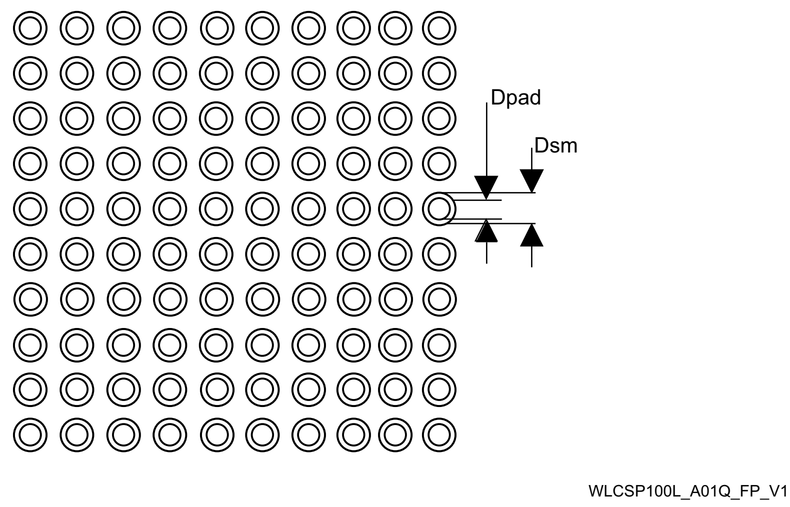


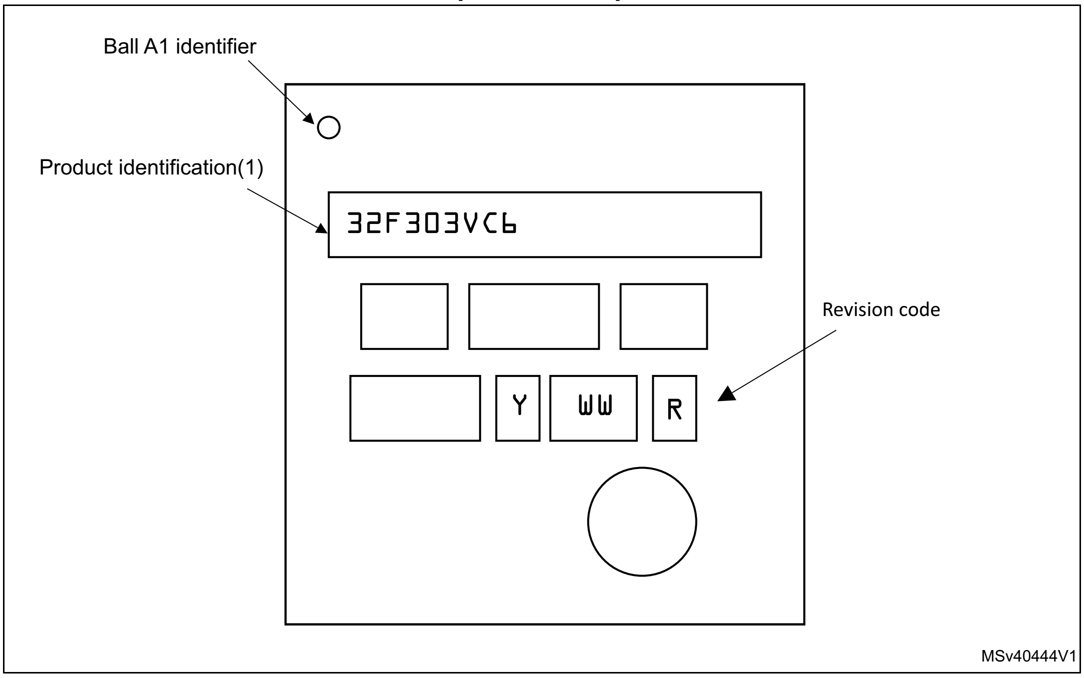
Table 85. WLCSP100 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 50. WLCSP100, 0.4 mm pitch wafer level chip scale package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.