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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f303cct6

List of figures

3.17.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter.It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stopand Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

Figure 6. STM32F303xB/STM32F303xC LQFP100 pinout

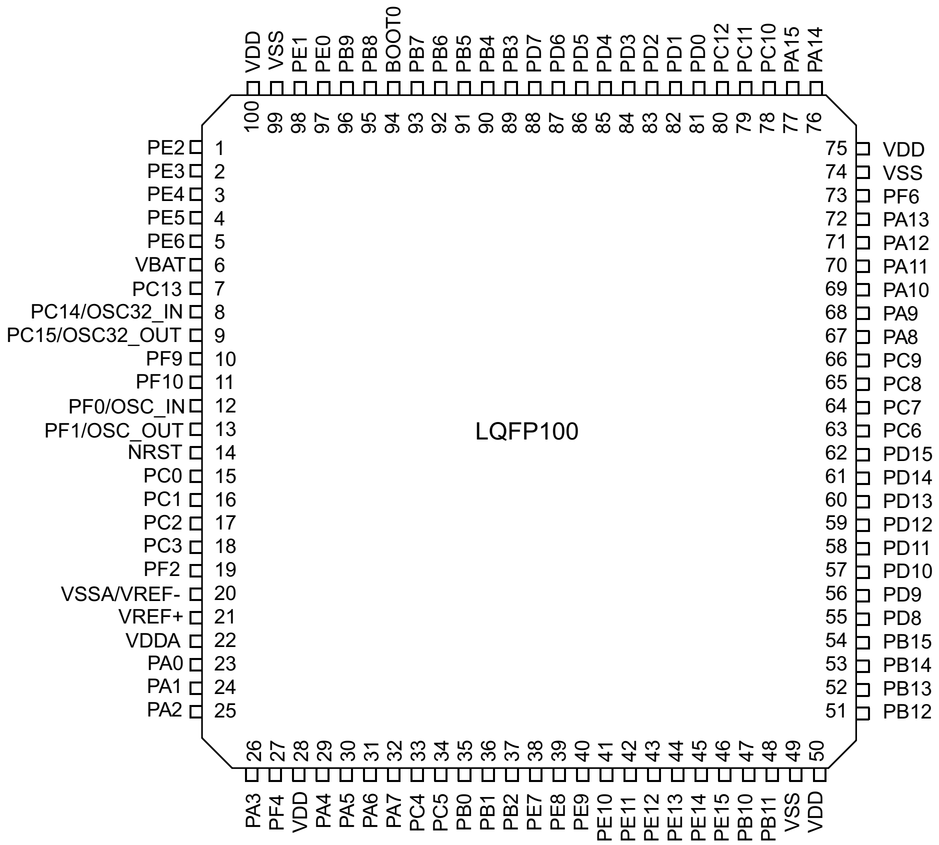


Table 13. STM32F303xB/STM32F303xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
C9	7	2	2	PC13(2)	I/O	TC	-	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
C10	8	3	3	PC14(2) OSC32_IN (PC14)	I/O	TC	-	-	OSC32_IN
D9	9	4	4	PC15(2) OSC32_ OUT (PC15)	I/O	TC	-	-	OSC32_OUT
D10	10	-	-	PF9	I/O	FT	(1)	TIM15_CH1, SPI2_SCK, EVENTOUT	-
E10	11	-	-	PF10	I/O	FT	(1)	TIM15_CH2, SPI2_SCK, EVENTOUT	-
F10	12	5	5	PF0- OSC_IN (PF0)	I/O	FTf	-	TIM1_CH3N, I2C2_SDA,	OSC_IN
F9	13	6	6	PF1- OSC_OUT (PF1)	I/O	FTf	-	I2C2_SCL	OSC_OUT
E9	14	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
G10	15	8	-	PC0	I/O	TTa	(1)	EVENTOUT	ADC12_IN6, COMP7_INM
G9	16	9	-	PC1	I/O	TTa	(1)	EVENTOUT	ADC12_IN7, COMP7_INP
G8	17	10	-	PC2	I/O	TTa	(1)	COMP7_OUT, EVENTOUT	ADC12_IN8
H10	18	11	-	PC3	I/O	TTa	(1)	TIM1_BKIN2, EVENTOUT	ADC12_IN9
E8	19	-	-	PF2	I/O	TTa	(1)	EVENTOUT	ADC12_IN10
H8	20	12	8	VSSA/ VREF-	S	-	-	Analog ground/Negative reference voltage	
J8	21	-	-	VREF+(3)	S	-	-	Positive reference voltage	
J10	22	-	-	VDDA	S	-	-	Analog power supply	
-	-	13	9	VDDA/ VREF+	S	-	-	Analog power supply/Positive reference voltage	
H9	23	14	10	PA0	I/O	TTa	(4)	USART2_CTS, TIM2_CH1_ETR,TIM8_BKIN, TIM8_ETR,TSC_G1_IO1, COMP1_OUT, EVENTOUT	ADC1_IN1, COMP1_INM, RTC_ TAMP2, WKUP1, COMP7_INP

Table 13. STM32F303xB/STM32F303xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
B5	90	56	40	PB4	I/O	FT	-	SPI3_MISO, I2S3ext_SD, SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TIM8_CH2N, TSC_G5_IO2, NJTRST, EVENTOUT	-
A6	91	57	41	PB5	I/O	FT	-	SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM8_CH3N, TIM17_CH1, EVENTOUT	-
B6	92	58	42	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TIM4_CH1, TIM8_CH1,TSC_G5_IO3, TIM8_ETR, TIM8_BKIN2, EVENTOUT	-
C5	93	59	43	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM3_CH4, TIM4_CH2, TIM17_CH1N, TIM8_BKIN, TSC_G5_IO4, EVENTOUT	-
A7	94	60	44	BOOT0	I	B	-	Boot memory selection	
D5	95	61	45	PB8	I/O	FTf	-	I2C1_SCL, CAN_RX, TIM16_CH1, TIM4_CH3, TIM8_CH2, TIM1_BKIN, TSC_SYNC, COMP1_OUT, EVENTOUT	-
C6	96	62	46	PB9	I/O	FTf	-	I2C1_SDA, CAN_TX, TIM17_CH1, TIM4_CH4, TIM8_CH3, IR_OUT, COMP2_OUT, EVENTOUT	-
B7	97	-	-	PE0	I/O	FT	(1)	USART1_TX, TIM4_ETR, TIM16_CH1, EVENTOUT	-
A8	98	-	-	PE1	I/O	FT	(1)	USART1_RX, TIM17_CH1, EVENTOUT	-
C7	99	63	47	VSS	S	-	-	Ground	
A9, A10, B10, B8	100	64	48	VDD	S	-	-	Digital power supply	

Table 20. STM32F303xB/STM32F303xC memory map, peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
	0x4000 8000 - 0x4000 FFFF	32 K	Reserved
APB1	0x4000 7800 - 0x4000 7FFF	2 K	Reserved
	0x4000 7400 - 0x4000 77FF	1 K	DAC (dual)
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	USB SRAM 512 bytes
	0x4000 5C00 - 0x4000 5FFF	1 K	USB device FS
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	TIM7
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

6.3 Operating conditions

6.3.1 General operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	V
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	–0.3	V_{DD}+0.3	V
		TTa I/O	–0.3	V_{DDA}+0.3	
		FT and FTf I/O(1)	–0.3	5.5	
		BOOT0	0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	WLCSP100	-	500	mW
		LQFP100	-	488	
		LQFP64	-	444	
		LQFP48	-	364	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).
3. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 39* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 39. Low-power mode wakeup timings

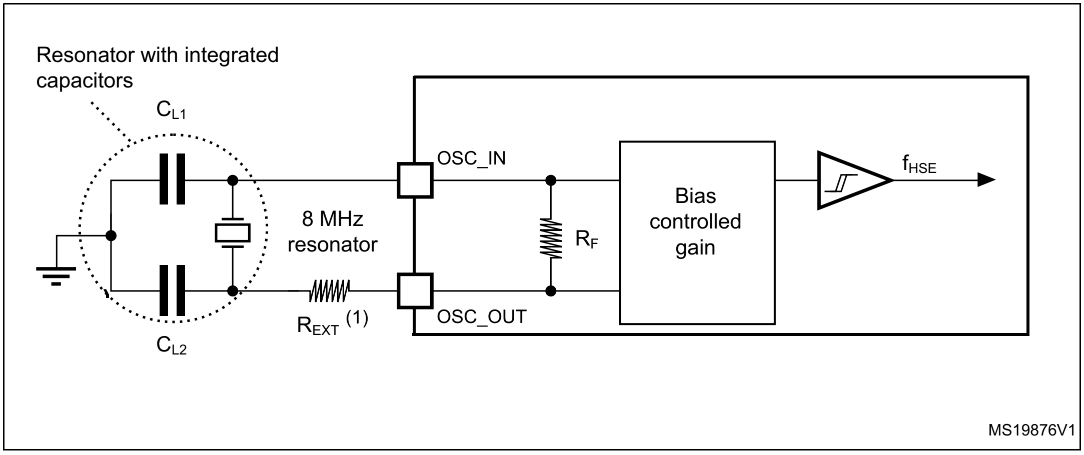
Symbol	Parameter	Conditions	Typ @V_{DD}, V_{DD} = V_{DDA}						Max	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	3.5	4.5	µs
		Regulator in low-power mode	7.9	6.7	6.1	5.7	5.4	5.2	9	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	69.2	60.3	56.4	53.7	51.7	50	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	6						-	CPU clock cycles

1. Guaranteed by characterization results.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 52. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 53*.

Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

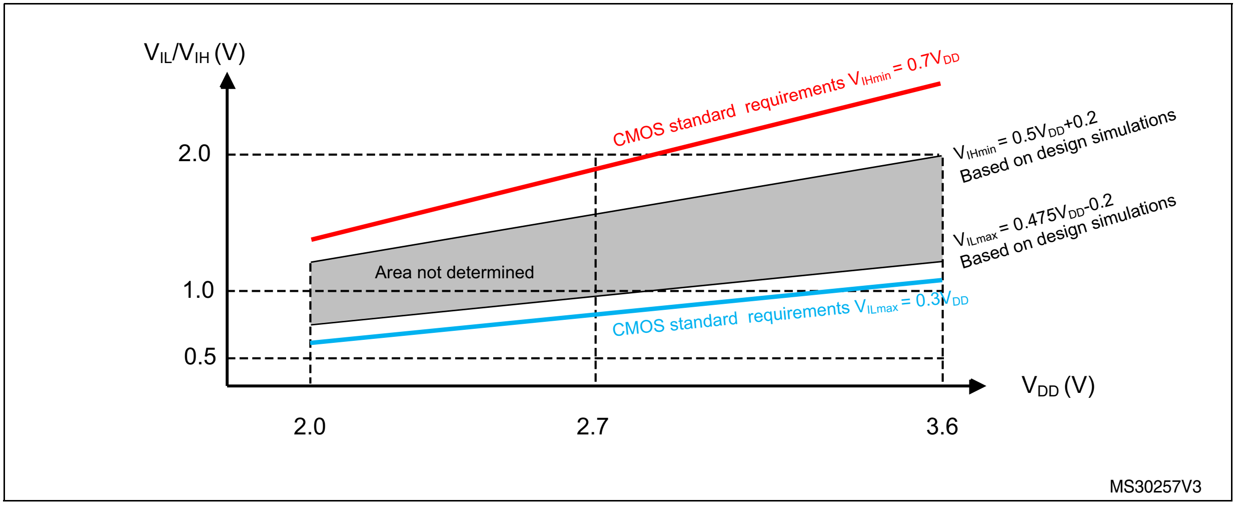
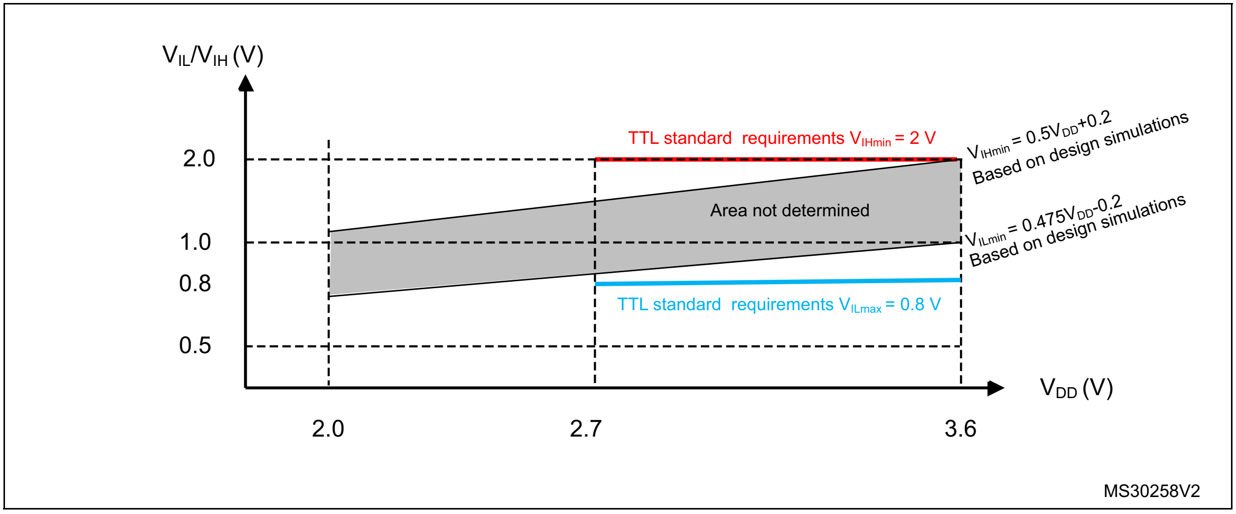


Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 23* and *Table 56*, respectively.

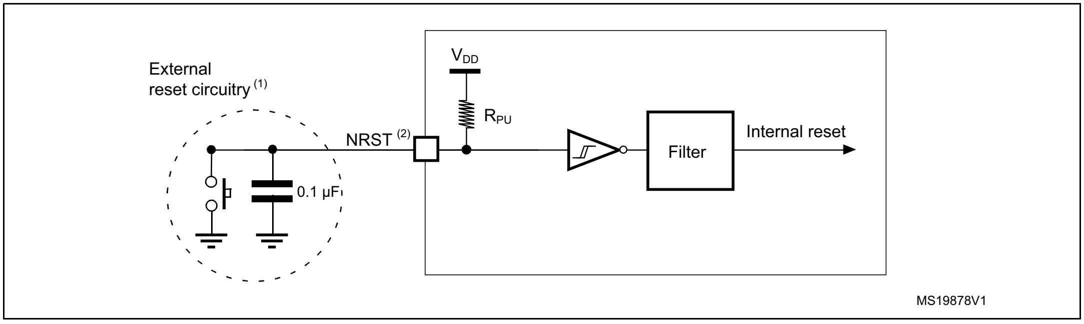
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 56. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50(3)	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30(3)	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(4)	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12(4)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34(4)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10(3)	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0316 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 23*.
3. Guaranteed by design.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F303x STM32F313xx reference manual RM0316 for a description of FM+ I/O mode configuration.

Figure 24. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 57*. Otherwise the reset will not be taken into account by the device.

6.3.16 Timer characteristics

The parameters given in *Table 58* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 58. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIMxCLK}$ = 144 MHz x=1.8	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIMxCLK}$ = 144 MHz x=1.8	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIMxCLK}$ = 144 MHz x=1.8	-	29.825	s

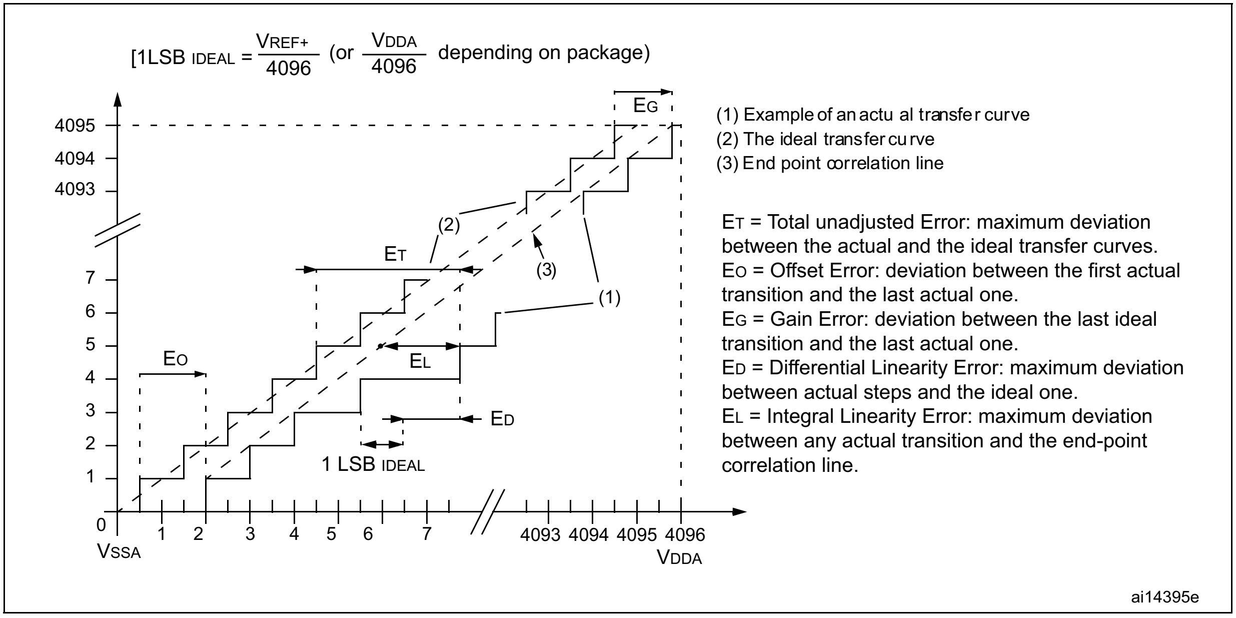
1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM8, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design.

3. Channels available on PA2, PA6, PB1, PB12.

Table 70. ADC accuracy - limited test conditions, 100-pin packages (1)(2)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz Sampling freq. ≤ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin package	Single ended	Fast channel 5.1 Ms	-	±3.5	±4.5	LSB
				Slow channel 4.8 Ms	-	±4	±4.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±2.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2.5	
				Slow channel 4.8 Ms	-	±2	±2.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±3	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
ENOB(4)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.7	10.8	-	bits
				Slow channel 4.8 Ms	10.7	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.1	11.3	-	
SINAD(4)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

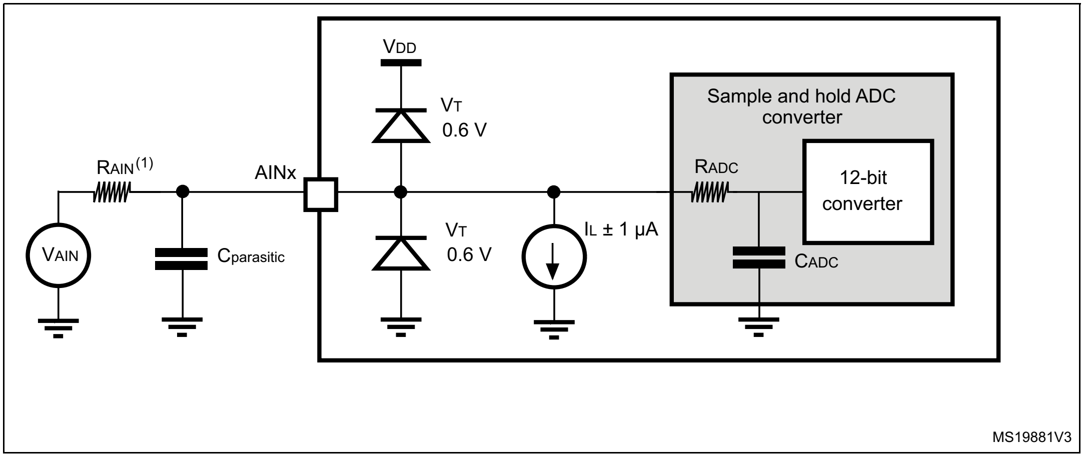
Figure 34. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
E_O = Offset Error: deviation between the first actual transition and the last actual one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end-point correlation line.

Figure 35. Typical connection diagram using the ADC



1. Refer to *Table 68* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

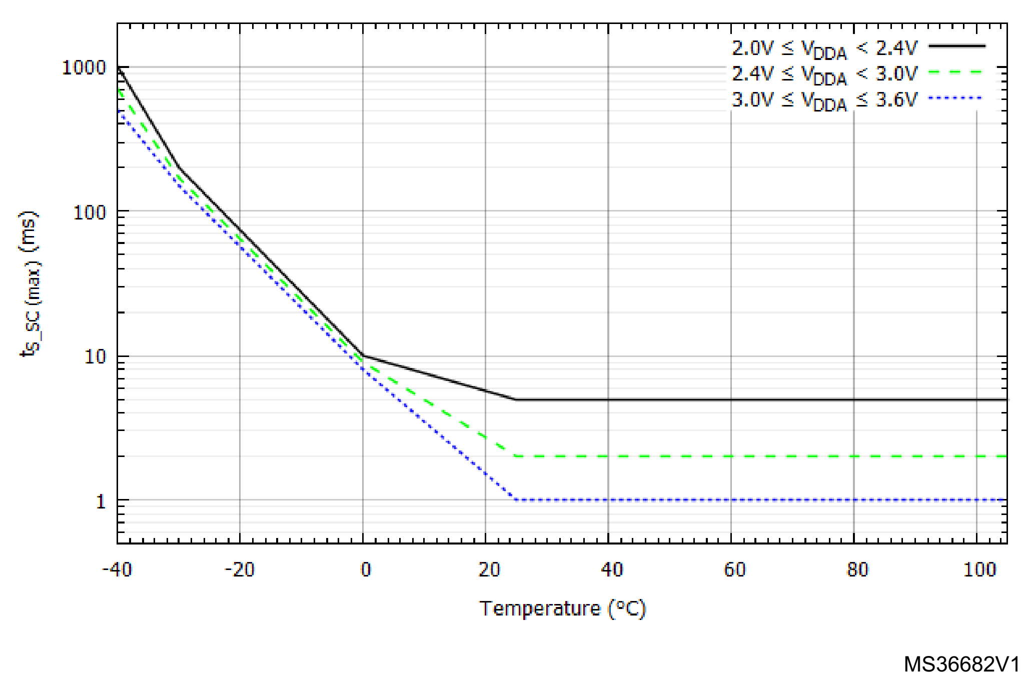
Power supply decoupling should be performed as shown in *Figure 11*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 76. Comparator characteristics[1] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Data guaranteed by design.
2. For more details and conditions, see *Figure 37* Maximum V_{REFINT} scaler startup time from power down.

Figure 37. Maximum V_{REFINT} scaler startup time from power down

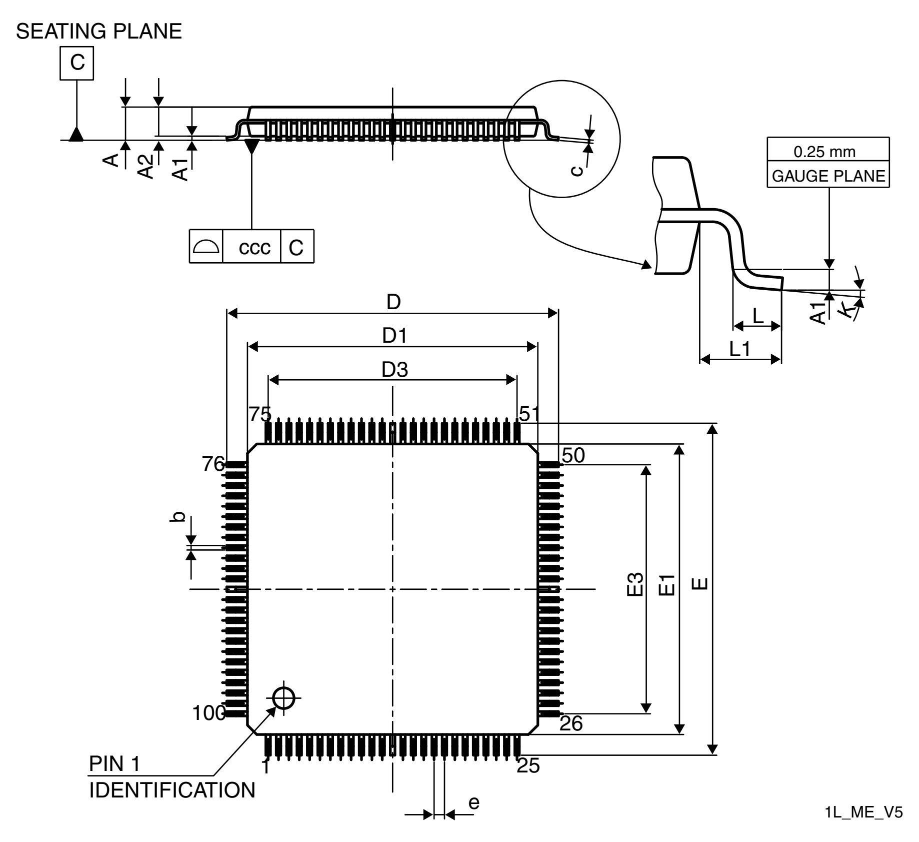


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 – 14 x 14 mm, low-profile quad flat package information

Figure 39. LQFP100 – 14 x 14 mm, low-profile quad flat package outline



1. Drawing is not to scale.

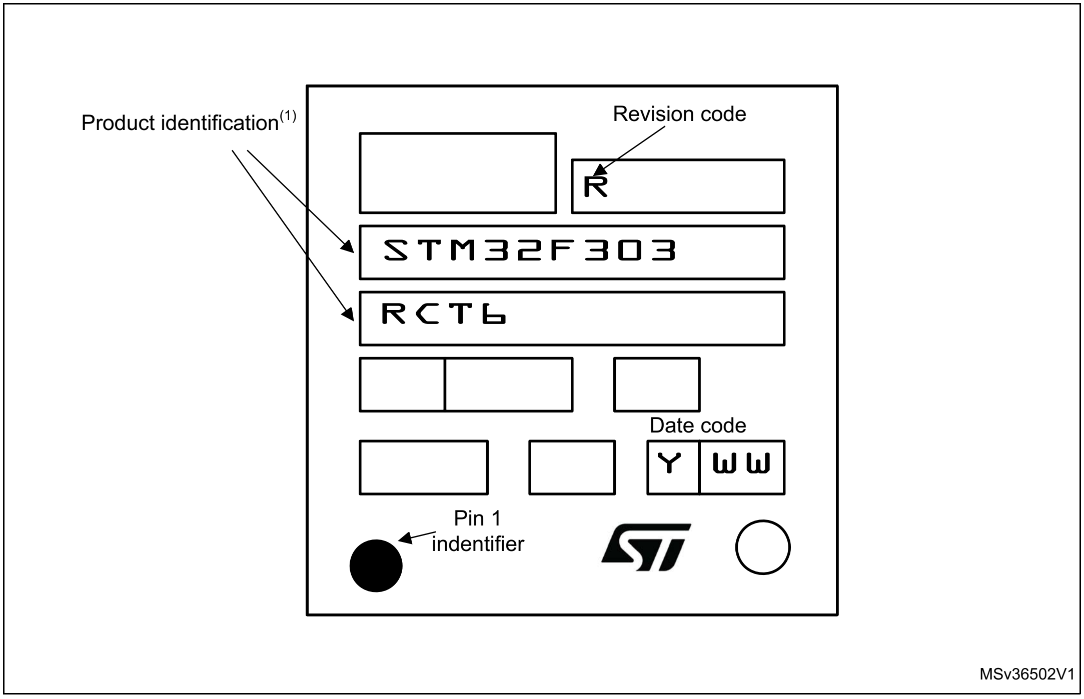
Table 81. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.0059

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 88. Document revision history (continued)

Date	Revision	Changes
05-Dec-2012	4	Updated first page Removed references to VDDSDx and VSSSD Added reference to PM0214 in *Section 1* Moved Temp. sensor calibartion values to*Table 79* and VREF calibration values to *Table 29* Updated *Table 3: STM32F303xx family device features and peripheral counts* Updated*Section 3.4: Embedded SRAM* Updated *Section 3.2: Memory protection unit (MPU)* Updated *Section 3.24: Universal serial bus (USB)* Modified *Section 3.26: Touch sensing controller (TSC)* Updated heading of *Table 11: USART features* Updated *Table 16: STM32F302xB/STM32F302xC pin definitions* Added notes to PC13, PC14 and PC15 in *Table 16: STM32F302xB/STM32F302xC pin definitions* Updated *Figure 11: Power supply scheme* Modified *Table 21: Voltage characteristics* Modified *Table 22: Current characteristics* Modified *Table 24: General operating conditions* Modified *Figure 13: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0] = ’00’)* Updated *Section 6.3.14: I/O port characteristics* Updated *Table 30: Typical and maximum current consumption from VDD supply at VDD = 3.6V* and *Table 31: Typical and maximum current consumption from the VDDA supply* Updated *Table 32: Typical and maximum VDD consumption in Stop and Standby modes* and *Table 33: Typical and maximum VDDA consumption in Stop and Standby modes* Updated *Table 34: Typical and maximum current consumption from VBAT supply* Added *Figure 13: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0] = ’00’)* Updated *Table 35: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 36: Typical current consumption in Sleep mode, code running from Flash or RAM* Added *Table 38: Peripheral current consumption* Added *Table 37: Switching output I/O current consumption* Updated *Section 6.3.6: Wakeup time from low-power mode* Modified *ESD absolute maximum ratings* Modified *Table 55: Output voltage characteristics* Updated *EMI characteristics* Updated *Table 56: I/O AC characteristics* Updated *Table 53: I/O current injection susceptibility* Updated *Table 58: TIMx characteristics* Updated *Section 7.4: WLCSP100 - 0.4 mm pitch wafer level chip scale package information* Added *Table 69: Maximum ADC RAIN* Added *Table 70: ADC accuracy - limited test conditions, 100-pin packages* Updated *Table 64: ADC accuracy - limited test conditions 2)* Updated *Table 75: DAC characteristics* Updated *Table 77: Operational amplifier characteristics* Updated figures and tables in *Section 7: Package information*

Table 88. Document revision history (continued)

Date	Revision	Changes
18-Apr-2014	8	Updated *Table 50: EMI characteristics* conditions :3.3v replaced by 3.6V. Updated *Section 6.3.17: Communications interfaces* I^2C interface. Updated *Table 77: Operational amplifier characteristics* adding TS_OPAMP_VOUT row. Updated *Section 3.13: Fast analog-to-digital converter (ADC)*. updated ARM and Cortex trademark. Updated *Table 32: Typical and maximum VDD consumption in Stop and Standby modes* with Max value at 85°C and 105°C. Updated *Table 70: ADC accuracy - limited test conditions, 100-pin packages* and *Table 71: ADC accuracy, 100-pin packages* for 100-pin package. Added *Table 72: ADC accuracy - limited test conditions, 64-pin packages* and *Table 73: ADC accuracy, 64-pin packages*for 64-pin package. Added *Table 74: ADC accuracy at 1MSPS* for 1MSPS sampling frequency. Updated *Table 63: SPI characteristics*. Updated *Table 75: DAC characteristics*.
09-Dec-2014	9	Updated core description in cover page. Updated HSI characteristics *Table 44: HSI oscillator characteristics* and *Figure 18: HSI oscillator accuracy characterization results for soldered parts*. Updated *Table 58: TIMx characteristics*. Updated *Table 16: STM32F302xB/STM32F302xC pin definitions* adding note for I/Os featuring an analog output function (DAC_OUT,OPAMP_OUT). Updated *Table 68: ADC characteristics* adding IDDA & IREF consumptions. Added *Figure 32: ADC typical current consumption on VDDA pin* and *Figure 33: ADC typical current consumption on VREF+ pin*. Added *Section 3.8: Interconnect matrix*. Updated *Figure 5: Clock tree*. Added note after *Table 32: Typical and maximum VDD consumption in Stop and Standby modes*. Updated *Section : In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.* with new LQFP100, LQFP64, LQFP48 package marking. Updated *Table 16: STM32F302xB/STM32F302xC pin definitions* and alternate functions tables replacing usart_rts by usart_rts_de.
29-Jan-2015	10	Updated *Section 6.3.20: Comparator characteristics* modifying ts_sc characteristics in *Table 76* and adding *Figure 37: Maximum VREFINT scaler startup time from power down*. Updated I_{DD} data in *Table 42: HSE oscillator characteristics*.